**Expert Instructions**

for the ITS surface commissioning (Blg. 167)

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# **IMPORTANT CONTACTS**

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# **DETECTOR AND SERVICES LAYOUT**

## DETECTOR LAYOUT

The **Inner Barrel (IB)** consists of the three innermost layers, also referred to as *Inner Layers* (IL, Layers 0 to 2), while the **Outer Barrel (OB)** contains the four outermost layers, also referred as *Middle Layers* (ML, Layers 3 and 4) and *Outer Layers* (OL, Layers 5 and 6). The ITS layers are azimuthally segmented in units named Staves, which are mechanically independent. Staves are fixed to a support structure, half-wheel shaped, to form the Half-Layers. The Stave of the Outer Barrel is further segmented in azimuth in two halves, named Half-Stave. In total there are: 48 Staves in the IL, 54 Staves in the ML and 90 in the OL.

Following Stave name convention has been defined:

**Inner Barrel** → **L***X***\_***YY***\_C***ZZ*

where:

*X* = 0,1,2 ,

*Y* = 00-11 for L0, Y = 00-15 for L1, Y = 00-19 for L2

*Z* = 00-08 for all the layers

Example: L2\_09\_C07 == Layer 2, Stave 9, Chip 7

**Outer Barrel** → **L***X***\_***YYZ***\_M***W***\_C***QQ*

where:

*X* = 3,4,5,6

*YY* = 00-23 for L3, 00-29 for L4, 00-41 for L5, 00-47 for L6

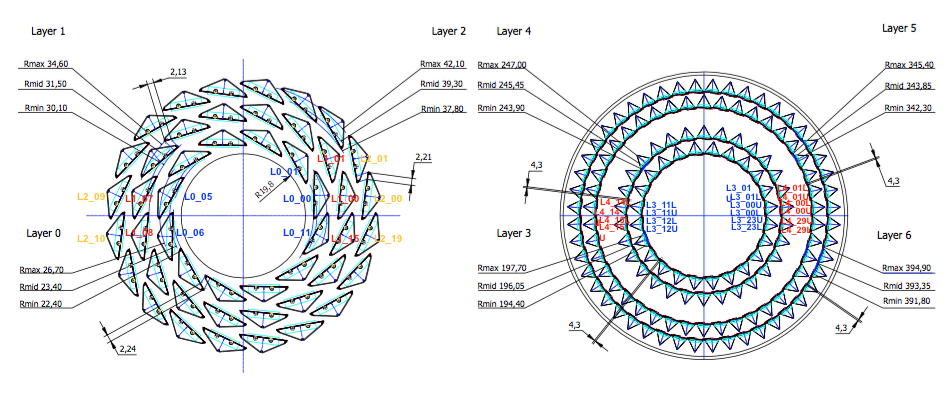
*Z* = U for upper HS and L for lower HS

*W* = 1-4 for L3 and L4, 1-7 for L5 and L6

*QQ* = 00-06 and 08-14

Example: L3\_23L\_M4\_C08 == Layer 3, Stave 23, Half-Stave lower, Module 4, Chip 8

This convention is graphically shown in the picture below and used to identify the pieces of the detector in the DCS panels.



## 

## POWER SYSTEM LAYOUT

Power system can be divided in two parts:

1. CAEN system – located in control room
2. Power units – located in clean room

### CAEN SYSTEM

CAEN system is used to provide powering to the Power Units (48 for the IL, 56 for the ML and 180 for the OL) and to the Readout Units (192). The structure of the CAEN power distribution system is based on EASY3000 system, able to run in magnetic field and radioactive environment. CAEN components of the system are:

* CAEN SY4527 (Mainframe) [1 unit] – Universal multichannel power system supply. The system allows to deal with power supply solutions composed by "branch controllers" (housed in the system mainframe) and on-detector "remote boards" (manufactured in order to be magnetic field and radiation tolerant)
  + Module A4531 [1 unit] – Primary power supply 600 W of the SY4527
  + Module A4528 [1 unit] – CPU control module of the SY4527
  + Module A1676A [3 units] – Branch controller (BC) for LV units
  + Module A2518 [6 units] – 8 independent LV Individual Floating channels board
* CAEN A3486 [12] - Two channel 400 Vac – 48 Vdc converter, which allows to integrate into the EASY channels control also the management of the 48 V power supplies
* CAEN EASY3000 crate [13] - Is a crate designed to house power supply and ADC boards of EASY3000 family; it supports mechanically EASY boards and distributes control signals and power supplies. It is handled by one of the six branches of the A1676A branch controller.
* CAEN A3009B [61] - LV dc-dc converter module with 12 independent channels (2-8V / 9A / 45W)

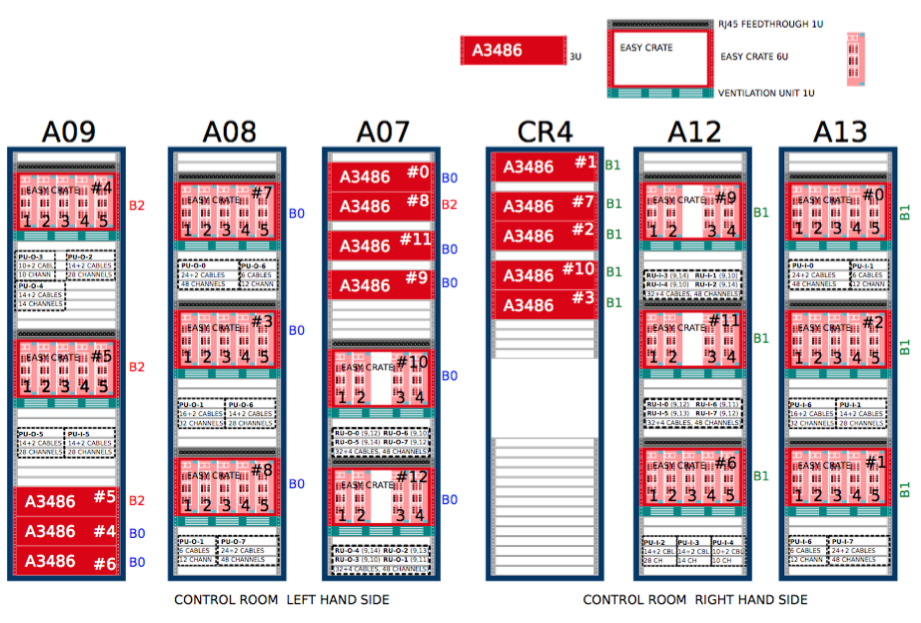
All these components are located in 6 racks located in the control room. A schematic description of their distribution into these 6 racks in shown in the figure below. Follow figure provide the splitting of the EASY3000 crates between the 3 branches (corresponding to the 3 modules A1676A. In the same picture it is also specified what is powered by the channels available in the modules contained in each EASY crate, Readout Unit or Power Unit; and moreover if the Power Unit will power staved in the IL, ML and OL.

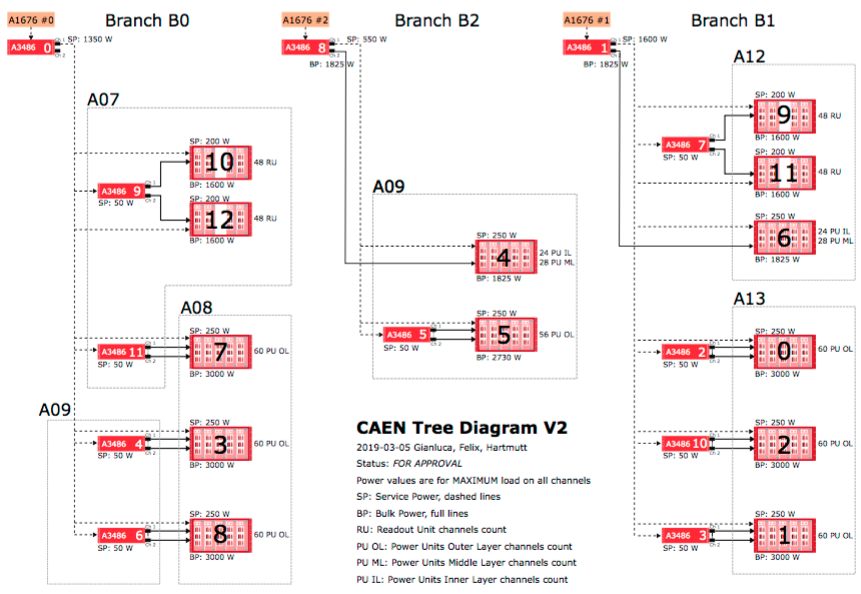
Detailed channels correspondences description is reported in the following file:

<https://espace.cern.ch/alice-project-itsug-electronics/_layouts/15/WopiFrame.aspx?sourcedoc=/alice-project-itsug-electronics/Shared%20Documents/Gianluca/Electronic_Board_Positions.xlsx&action=default>.

Further details on the cabling are available in the following document:

<https://espace.cern.ch/alice-project-itsug-electronics/_layouts/15/WopiFrame.aspx?sourcedoc=/alice-project-itsug-electronics/Shared%20Documents/Hartmut/CAENcablingbldg167.xlsx&action=default>





Further details about the powering infrastructure are shown in the two pictures below (<https://espace.cern.ch/alice-project-itsug-electronics/Shared%20Documents/CAEN/Alice%20ITS%20upgrade%20system%20layout_rev01.pdf>). In particular you can see how the different components are used for the two powering lines: *detector power* and *readout system power*.

*Detector power*

V power  
 IL: 4 A3009B hosted in 1 EASY crate powered by 1 A3486 (+ 1 spare channel)

ML: 9 A3009B hosted in 2 EASY crates powered by 1 A3486

OL: 30 A3009B hosted in 6 EASY crates powered by 3 A3486

V service

1 A1676 (BC) controls 1 A3486 that provides power to all the services, one channel for   
 IL and ML and the second channel for OL.

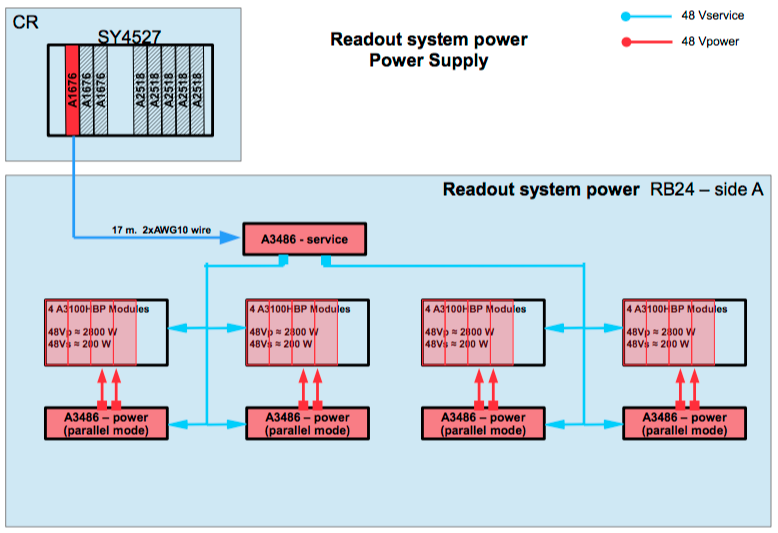
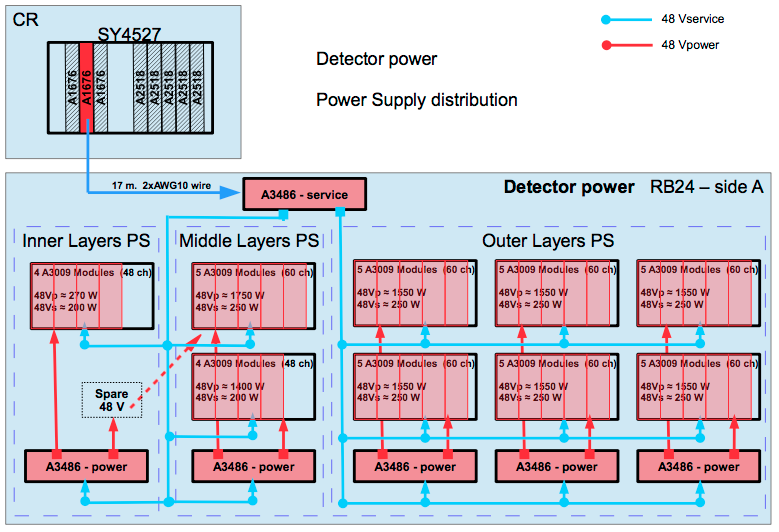
*Readout power*

V power

16 A3009B hosted in 4 EASY crates powered by 4 A3486 (parallel mode)

V service

1 A1676 (BC) controls 1 A3486 that provides power all the services symmetrically in the  
 two channels



**QUESTION**: DESCRIBE HOW THE CHANNELS IN MODULES A2518 ARE USED FOR BACK-BIAS.  
6 units having 8 channels each

### 

### 

### POWER BOARD

Link to the Power Unit operation manual (v1.4):

<https://twiki.cern.ch/twiki/pub/ALICE/DocumentationAndSchematics/2019_07_03_ITS_production_power_board_V14_32-channel_operation_manual.pdf>

The power board (PB) assembly consists of two functionally identical and operationally indistinguishable Power Units referenced to the same ground: Power Unit Right (PUR) and Power Unit Left (PUL). The circuitry on each PU is distributed mainly onto three polyfuse- protected power domains (referenced to the power board common ground): two positive voltage domains (3.3V) and a negative voltage domain (-5V max). Each power unit can operate in two modes: “Inner Barrel” (ILs use) and “Outer Barrel” (MLs and OLs use); the PU operation mode can be selected via a switch located on its top side. Each PU can generate 16 nominally 1.8 V power supply voltages each with a drive strength of 3 A and 4 additional negative voltage outputs with low current strength that can be used as bias connections.   
The main functionalities of the power system, controllable via I2C interfaces, are listed below:

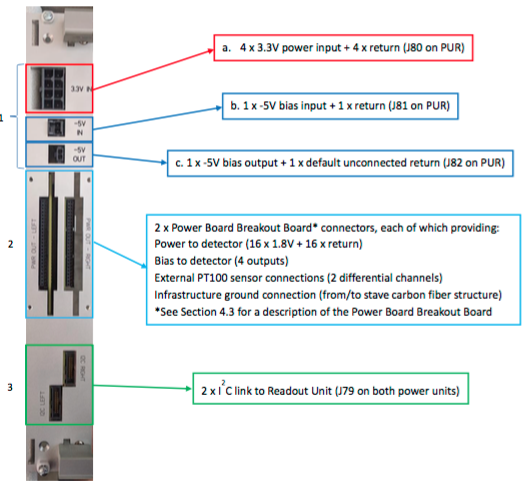
* Individual enabling of supply channels and bias outputs
* Individual adjustment of supply voltages
* Adjustment of bias voltages on power unit basis (2x4 bias outputs with common source)
* Over-current protection circuit with adjustable threshold on each supply channel
* Over-temperature protection circuits on a power unit basis.
* Monitoring of voltages, currents and temperatures

In order to dissipate the heat generated during normal operation, the main power board is equipped with a heat exchanger with inlet/outlet pipes for connection to an external cooling system located on the rear side of the power board assembly.  
The temperature of each PU can also be monitored using a SMD PT100 temperature sensor located on the PCB top of each power unit. Two additional temperature measuring circuits per power unit allow for the readout of up to 2 external PT100 sensors. These are meant to be used to monitor the temperature of the stave inlet/outlet cooling pipes.  
A total of 66 LEDs per PB indicate the status of various parts of the board and can help identifying possible issues, in particular:

* A red LED near each regulator is used to indicate the occurrence of an overcurrent condition. When this happens, the corresponding channel is automatically switched off. At board power on, all these red LEDs are turned on indicating that all supply voltages are grounded.
* A green LED located near each regulator is used to indicate that the corresponding channel is enabled and working properly. Since its brightness grows with the magnitude of the output voltage, it may not be visible for low output voltage values (below 1.8V). A green LED and a red LED belonging to the same channel cannot be simultaneously on. The happening of such condition is an indication that the power board is not working properly.
* A red LED located on the rear side of a power unit is used to indicate the occurrence of an over-temperature condition (threshold temperature is 65°C by design). When this happens all the supply channels of that power unit are simultaneously disabled. Power cycling a power unit will recover it from an over-temperature condition and consequent disabling of the supply channels.

The PB front panel accommodates the following power/control interface connectors:

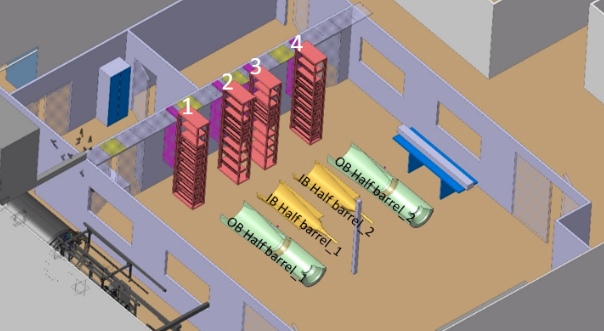
1. A set of input/output power connectors:   
   a) 8-pin 3.3V input power connector that allow for the powering of up to 4 of the power board 3.3V power domains (2 for PUR and 2 for PUL);   
   b) 2-pin -5V input power connector that allow for the powering of all the PB bias-generating circuitry;   
   c) 2-pin -5V output power connector that allows for the daisy-chaining of the -5V input power source.
2. Two PB breakout board connectors
3. Two right-angle 20-pin I2C connectorsfor the control of the two PUs via the ALICE ITS [Readout Unit](#_heading=h.v9ea9kmnbf93); each connector carries the signals for 2 independent I2C interfaces.



Link to the presentation where details on RU and PB distribution in racks is summarized:

<https://espace.cern.ch/alice-project-itsug-electronics/_layouts/15/WopiFrame.aspx?sourcedoc=/alice-project-itsug-electronics/Shared%20Documents/Gianluca/20181019_PP1_Board_Positions.pptx&action=default>.

PBs and RUs are located in the clean room in four racks, as shown in the picture below. The naming of the subracks follow the one that will be used at P2, when all the subracks will actually be hosted in only two racks.



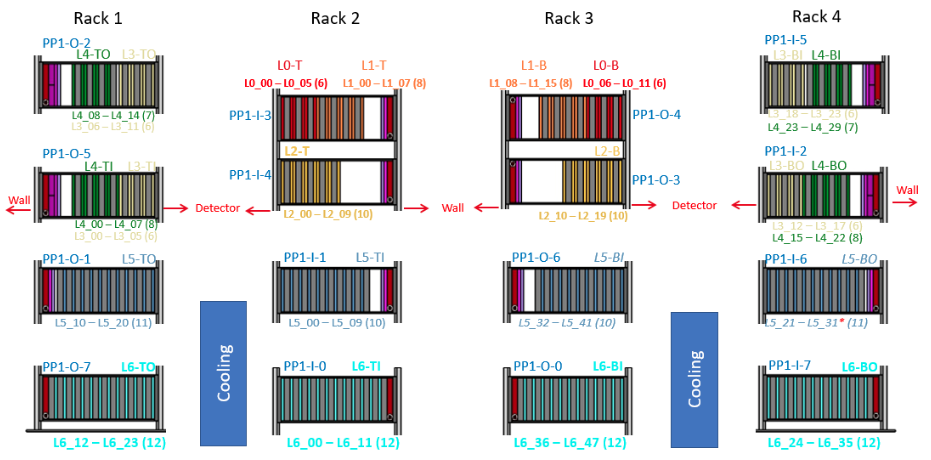
As it will be shown in the [Readout unit paragraph](#_heading=h.v9ea9kmnbf93), each stave is controlled and read-out by one RU. Each RU is able to control up to two PUs; in the ILs and MLs each RU controls only one PU, while in the OLs each RU controls two PUs.

In the *Inner Layers*, each stave is powered by one channel of one PU (remaining channels are not used in this case), giving 12 PUs on 6 PBs for L0, 16 PUs on 8 PBs for L1 and 20 PUs on 10 PBs for L2, for a total of 48 PUs on 24 PBs. These PBs are distributed in four subracks called: PP1-I-3 (L0\_00-L0-05 and L1\_00-L1-07), PP1-I-4 (L2\_00-L2\_09) on rack 2 and PP1-O-4 (L0\_06-L0\_11 and L1\_08-L1\_15), PP1-O-3 (L2\_10-L2-19) on rack 4.

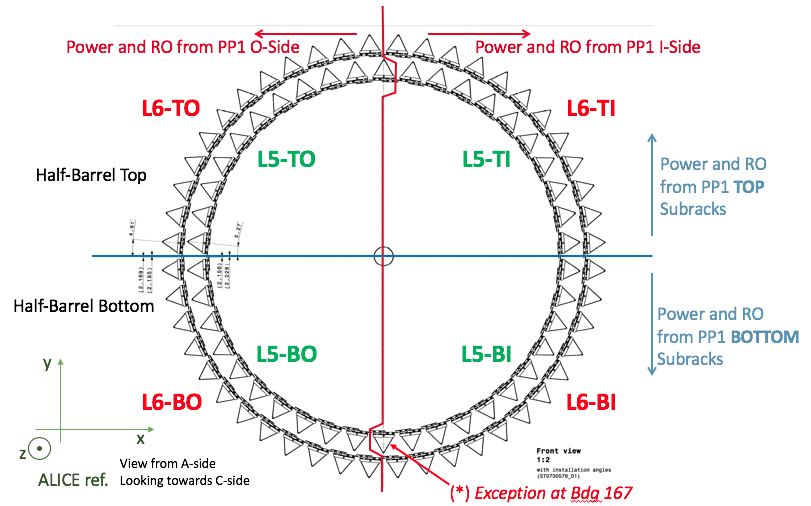
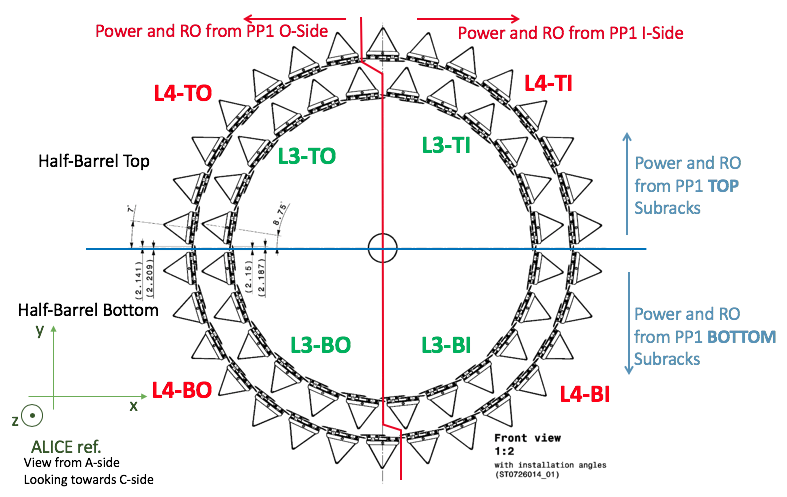
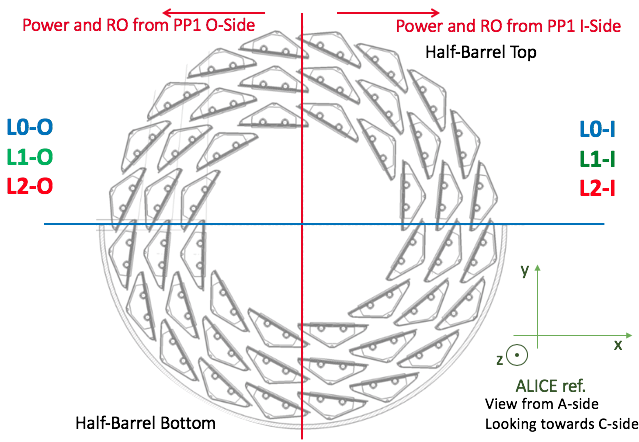
In the *Middle Layers* too, each stave is powered by one PU (all the 8 outputs in use), giving 24 PUs on 12 PBs for L3 and 30 PUs on 16 PBs (two PUs are not used) for L4 distributed in four subracks called: PP1-O-2 (L4\_08-L4\_14 and L3\_06-L3\_11 and hosting one PB with not used PU), PP1-O-5 (L4\_00-L4\_07 and L3\_00-L3\_05) on rack 1 and PP1-I-5 (L3\_18-L3\_23 and L4\_23-L4\_29 hosting the second PB with not used PU), PP1-I-2 (L3\_12-L3\_17 and L4\_15-L4\_22) on rack 4.

In the *Outer Layers*, two PUs are needed to power one full stave (only 28 channels over 32 actually used), giving 84 PUs on 42 PBs for L5 and 96 PUs on 48 PBs for L6 distributed in eight subracks called: PP1-O-1 (L5\_10-L5\_20) and PP1-O-7 (L6\_12-L6\_23) on rack 1, PP1-I-1 (L5\_00-L5\_09) and PP1-I-0 (L6\_00-L6\_11) on rack 2, PP1-O-6 (L5\_32-L5\_41) and PP1-O-0 (L6\_36-L6\_47) on rack 3 and PP1-I-6 (L5\_21-L5\_31) and PP1-I-7 (L6\_24-L6\_35) on rack 4.

How the mentioned subracks are distributed within the four racks is also shown in the following figure.



As can be seen in the above picture PB (in gray) are always alternated with a RU (colored) the usually control the corresponding PU(s) in the close PB.   
As written, at P2 all these subracks will be actually housed in only two big racks within the magnet on the mini-frame at the two sides of the beam pipe, having in this way one rack on the O-side (outer with respect to the LHC ring) and the other on the I-side (inner with respect to the LHC ring). How the different staves in the different layers are split in the two racks is better clarified in the following figure.

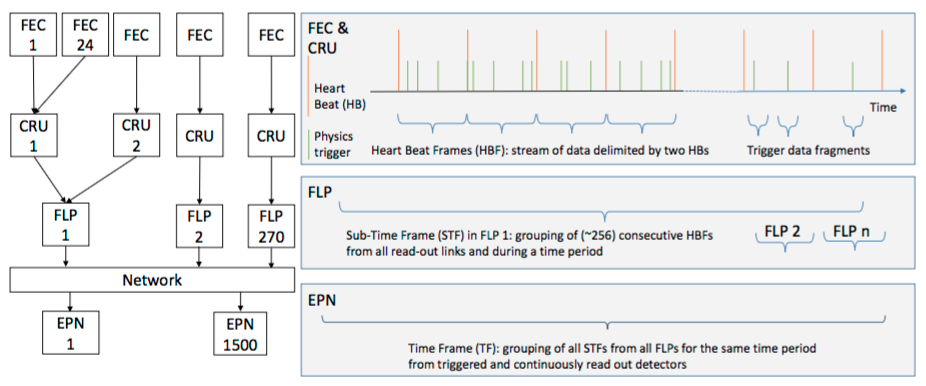


## READOUT SYSTEM LAYOUT

Readout system can be divided in two parts:

1. Readout units
2. CRU/FLP/EPN

A schematic view of the event data assembly procedure, from the detector data collected in each heart beat to the final compressed time frame, is shown in the following picture.



The data produced by the Front-End Cards (FEC) are transferred to the Common Read-out Units (CRU) which are the interfaces to a first farm of computers: the First-Level Processors (FLP) where an initial data volume reduction is performed. The data merging and the final data volume reduction is performed by a second farm of computers: the Event Processing Nodes (EPN). Dedicated time markers, the heartbeat triggers (HB), will be used to chop the data flow to the FLPs into manageable pieces called HB Frames (HBF). The HBFs are assembled in Sub- Time Frames (STF) by the First-Level Processors (FLPs) and then in Time Frames (TF) by the Event Processing Nodes (EPN).

For a complete description of the ALICE Run3 and Run4 data taking architecture have a look at the O2 project Technical Design Report:

<https://cds.cern.ch/record/2011297/files/ALICE-TDR-019.pdf>.

### READOUT UNIT

The readout units are electronic boards that are tasked with controlling and gathering data from the ALPIDE sensor chips on the staves. They will also forward trigger information from the ALICE trigger system to the sensor chips.

It is equipped with several components and ports and is located between the sensor staves and the common readout units in the readout chain. The heart of the board is the main FPGA, a Xilinx Ultrascale, which runs the main firmware that manages the readout process and stream of data. There is also secondary flash-based FPGA, a Microsemi ProAsic3 A3PE600L, referred to as PA3. The PA3 auxiliary FPGA on the RU handles configuration of the Ultrascale, using data from a flash memory chip which it can write to and read from. In addition to initial configuration at power-up, the PA3 will also continuously re-configure the Ultrascale during operation, by overwriting configuration memory without actually resetting or pausing the Ultrascale operation. This technique is known as scrubbing, and it should ensure a reliable operation of the main FPGA as any unwanted error in the configuration caused by single event upsets (SEU) will be cleaned within seconds, without having to shut down the detector and lose valuable experiment time.  
The readout unit includes high-speed Firefly ports for electrically connecting to its designated ALPIDE chip stave. It also contains three GBTx chips and slots for suitable optical transceivers like VTRx’s for connecting to a CRU using the GBT link. Up to three GBT uplinks (from the CRU to the RU) can be used for data. One of the GBT links will also be used for control, and one will be used for trigger information. The GBTx chip used for control is connected to a GBT-SCA ASIC, which can be used for various slow control tasks. The main communication with the PA3 will use an I2C master module on the GBT-SCA.

Each stave is connected to its own readout unit, resulting in a total of 192 readout units as there will be 192 sensor staves in the ITS. These boards are located in Clean Room, close to the detector, distributed in four racks together with the power units, as shown in the picture present in the [power unit section](#_heading=h.tteqjy9o0j3a).

### CRU/FLP/EPN

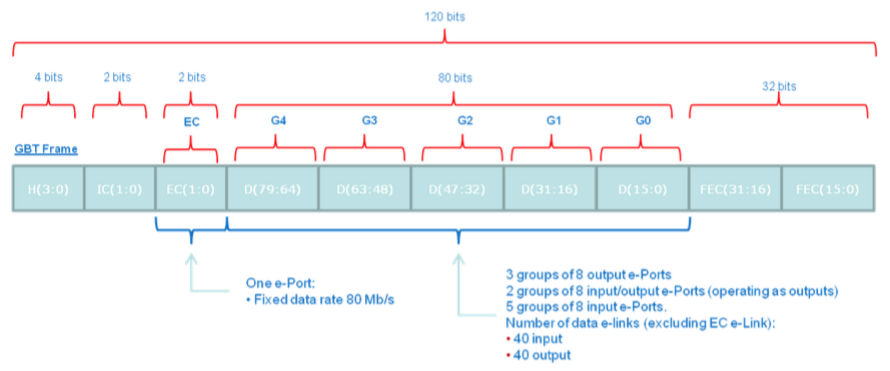
The CRUs act as an interface between the Front Electronics (RUs with ALPIDE sensors), the detector control system, the data computing facilities, and the trigger network. The CRU mainly consists of an FPGA and multiple data links, specifically optical GBT links connected to RUs, TTC-PON carrying trigger and timing information, and a PCI-express interface for communicating with its host computer which is part of the O2 First Level Processing (FLP) system. The CRU will organize (tag and multiplex) and compress (discard useless frames etc.) the data to reduce the bandwidth requirement for the final readout chain steps. The firmware is modular and its base include the necessary modules for the interfaces common to most detectors in ALICE. A user logic module at the heart of the firmware is left to be customized by detector teams if they need additional features or specialized behavior.

Each CRU will have 24 GBT links available. Since each RU uses 3 GBT links, this means that each CRU can be connected to a maximum of 8 RUs. Each FLP node will house one CRU. Consequently the ITS do require 24 CRUs and an equivalent number of FLPs. [TO BE CHECKED]

**QUESTION**: How many CRUs and FLPs do we have in this moment for the surface commissioning? How they are arranged? Do we have any document that do describe this?

### GBT link and Slow Control

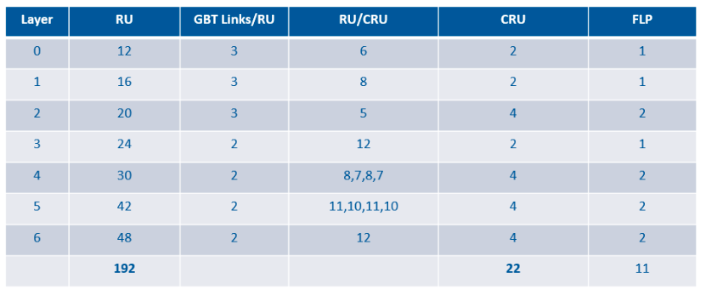
The GigaBit Transceiver (GBT) architecture is an optical serial data link which requires high bandwidth as well as radiation hardening. It is frame based, with one 120-bit frame transmitted continuously at an interval of 25 ns. This results in a raw serial line rate of 4.8 Gb/s. 25 nm corresponds to the LHC bunch crossing interval. The GBT frame is illustrated in the following figure.



It is composed of:

* 4 bit long header: 0b0101 in case of valid frame, 0b0110 otherwise (e.g. transmitter idle or frame contains non-data information, such as Single Word Transactions (SWT))
* 4 bit for slow control information: 2 Internal Control (IC) and 2 External Control (EC)
* main data payload of 80 bits
* 32 bits of error correction

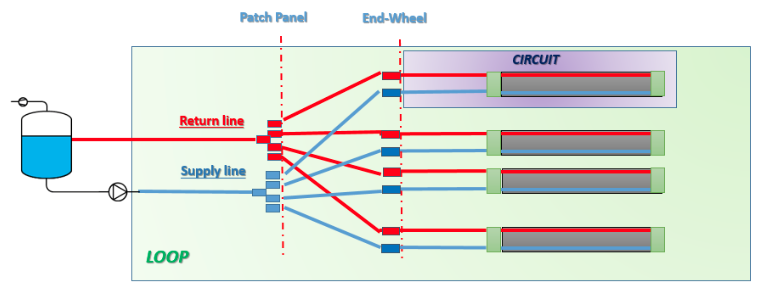
The data field (80-bit) of the GBT frame is used to transmit the data. GBT frames are differentiated into control frames and data frames, with the header specifying data valid for the latter only. Control frames start with a 4 bit identifying header. Four headers are defined: IDLE, SOP (Start Of Packet), EOP (End Of Packet) and SWT (Single Word Transactions). IDLE frames contain no information. SOP and EOP mark the start and end of packets of data from the detectors. SWT frames can contain arbitrary data used for special control or data transfers, these frames may only be sent in between data frames, in other words between EOP and SOP control frames. In the ITS readout electronics, SWT frames are for example used to access the register bus on the readout unit main FPGA.  
Part of the GBT link is the slow control system. The 2 bytes in the EC field of the GBT frame payload is forwarded to a dedicated ASIC for slow control called GBT-SCA (part of the readout unit board). This ASIC contains several communication modules, including a range of GPIO, ADC and DAC pins, as well as I2C, SPI and JTAG masters.



This table has to be verified

## COOLING PLANT

[<https://espace.cern.ch/alice-project-itsug-electronics/_layouts/15/WopiFrame.aspx?sourcedoc=/alice-project-itsug-electronics/Shared%20Documents/Gianluca/20180515_cooling_pipes_name_convention.pptx&action=default>]



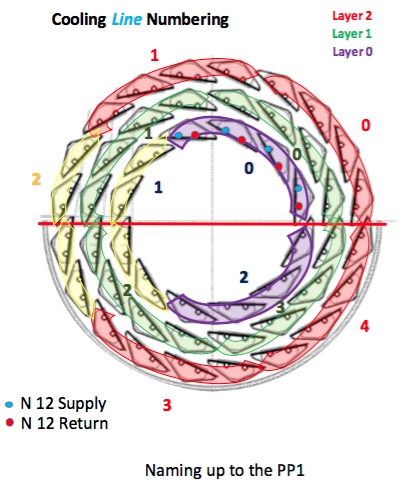
Few definitions:

* **Cooling Circuit** = water routing inside one IB stave/one OB stave/one RU board
* **Supply/return Line** = water routing from the plant to the patch panel
* **Loop** = closed water routing connecting the plant to the patch panel with one supply line and one return line

*EX: 1 IB loop is feeding 4 cooling circuits; 1 OB loop is feeding 6 cooling circuits, 1 RU loop is feeding 12 cooling circuits*

### INNER BARREL LOOPS

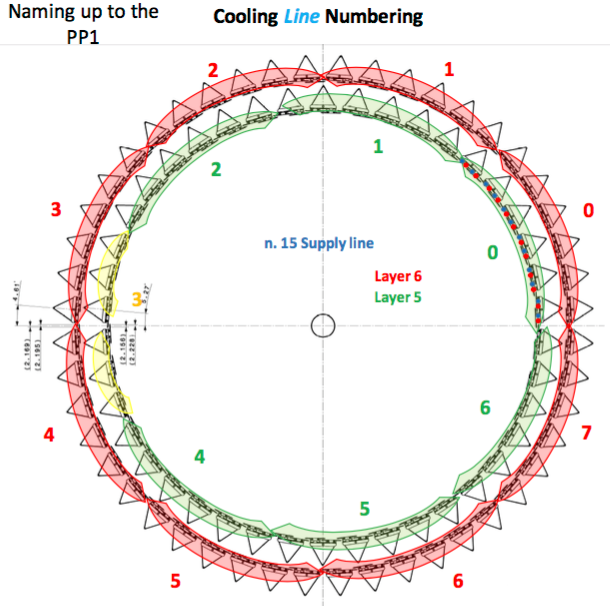
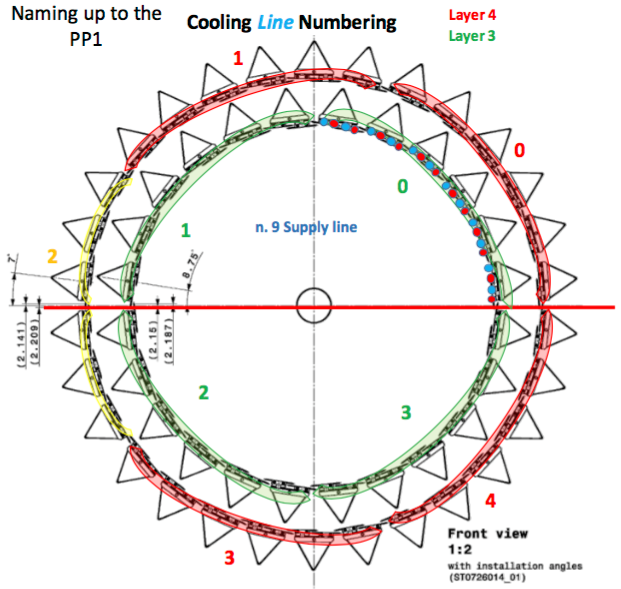
Each loop feed 4 cooling circuits, so we have 3 loops for L0, 4 loops for L1 and 5 loops for L2 grouped and arranged as shown in Figure below. Naming for all the cooling lines of the ILs are reported in Table below. Line name is composed like: IBXYM, where, X = 0,1,2, Y = 0-2 for L0, 0-3 for L1 and 0-4 for L2, M = S (for supply) or R (for return).



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BARREL** | **LAYER** | **COOLING LINES** | **LINE NAME (SUPPLY/RETURN)** | **STAVE** |
| IB | 0 | 0 | IB00S/IB00R | L0\_00, L0\_01, L0\_02, L0\_03 |
| IB | 0 | 1 | IB01S/IB01R | L0\_04, L0\_05, L0\_06, L0\_07 |
| IB | 0 | 2 | IB02S/IB02R | L0\_08, L0\_09, L0\_10, L0\_11 |
| IB | 1 | 0 | IB10S/IB10R | L1\_00, L1\_01, L1\_02, L1\_03 |
| IB | 1 | 1 | IB11S/IB11R | L1\_04, L1\_05, L1\_06, L1\_07 |
| IB | 1 | 2 | IB12S/IB12R | L1\_08, L1\_09, L1\_10, L1\_11 |
| IB | 1 | 3 | IB13S/IB13R | L1\_12, L1\_13, L1\_14, L1\_15 |
| IB | 2 | 0 | IB20S/IB20R | L2\_00, L2\_01, L2\_02, L2\_03 |
| IB | 2 | 1 | IB21S/IB21R | L2\_04, L2\_05, L2\_06, L2\_07 |
| IB | 2 | 2 | IB22S/IB22R | L2\_08, L2\_09, L2\_10, L2\_11 |
| IB | 2 | 3 | IB23S/IB23R | L2\_12, L2\_13, L2\_14, L2\_15 |
| IB | 2 | 4 | IB24S/IB24R | L2\_16, L2\_17, L2\_18, L2\_19 |

### OUTER BARREL LOOPS

Each loop feed 6 cooling circuits, so we have 4 loops for L3, 5 loops for L4, 7 loops for L5 and 8 loops for L6 grouped and arranged as shown in Figure below. Naming for all the cooling lines of the ILs are reported in Table below. Line name is composed like: IBXYM, where, X = 3,4,5,6, Y = 0-3 for L3, 0-4 for L4, 0-6 for L5 and 0-7 for L6, M = S (for supply) or R (for return).



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BARREL** | **LAYER** | **COOLING LINES** | **LINE NAME (SUPPLY/RETURN)** | **STAVE** |
| OB | 3 | 0 | OB30S/OB30R | L3\_00, L3\_01, L3\_02, L3\_03, L3\_04, L3\_05 |
| OB | 3 | 1 | OB31S/OB31R | L3\_06, L3\_07, L3\_08, L3\_09, L3\_10, L3\_11 |
| OB | 3 | 2 | OB32S/OB32R | L3\_12, L3\_13, L3\_14, L3\_15, L3\_16, L3\_17 |
| OB | 3 | 3 | OB33S/OB33R | L3\_18, L3\_19, L3\_20, L3\_21, L3\_22, L3\_23 |
| OB | 4 | 0 | OB40S/OB40R | L4\_00, L4\_01, L4\_02, L4\_03, L4\_04, L4\_05 |
| OB | 4 | 1 | OB41S/OB41R | L4\_06, L4\_07, L4\_08, L4\_09, L4\_10, L4\_11 |
| OB | 4 | 2 | OB42S/OB42R | L4\_12, L4\_13, L4\_14, L4\_15, L4\_16, L4\_17 |
| OB | 4 | 3 | OB43S/OB43R | L4\_18, L4\_19, L4\_20, L4\_21, L4\_22, L4\_23 |
| OB | 4 | 4 | OB44S/OB44R | L4\_24, L4\_25, L4\_26, L4\_27, L4\_28, L4\_29 |
| OB | 5 | 0 | OB50S/OB50R | L5\_00, L5\_01, L5\_02, L5\_03, L5\_04, L5\_05 |
| OB | 5 | 1 | OB51S/OB51R | L5\_06, L5\_07, L5\_08, L5\_09, L5\_10, L5\_11 |
| OB | 5 | 2 | OB52S/OB52R | L5\_12, L5\_13, L5\_14, L5\_15, L5\_16, L5\_17 |
| OB | 5 | 3 | OB53S/OB53R | L5\_18, L5\_19, L5\_20, L5\_21, L5\_22, L5\_23 |
| OB | 5 | 4 | OB54S/OB54R | L5\_24, L5\_25, L5\_26, L5\_27, L5\_28, L5\_29 |
| OB | 5 | 5 | OB55S/OB55R | L5\_30, L5\_31, L5\_32, L5\_33, L5\_34, L5\_35 |
| OB | 5 | 6 | OB56S/OB56R | L5\_36, L5\_37, L5\_38, L5\_39, L5\_40, L5\_41 |
| OB | 6 | 0 | OB60S/OB60R | L6\_00, L5\_01, L5\_02, L5\_03, L5\_04, L5\_05 |
| OB | 6 | 1 | OB61S/OB61R | L6\_06, L6\_07, L6\_08, L6\_09, L6\_10, L6\_11 |
| OB | 6 | 2 | OB62S/OB62R | L6\_12, L6\_13, L6\_14, L6\_15, L6\_16, L6\_17 |
| OB | 6 | 3 | OB63S/OB63R | L6\_18, L6\_19, L6\_20, L6\_21, L6\_22, L6\_23 |
| OB | 6 | 4 | OB64S/OB64R | L6\_24, L6\_25, L6\_26, L6\_27, L6\_28, L6\_29 |
| OB | 6 | 5 | OB65S/OB65R | L6\_30, L6\_31, L6\_32, L6\_33, L6\_34, L6\_35 |
| OB | 6 | 6 | OB66S/OB66R | L6\_36, L6\_37, L6\_38, L6\_39, L6\_40, L6\_41 |
| OB | 6 | 7 | OB67S/OB67R | L6\_42, L6\_43, L6\_44, L6\_45, L6\_46, L6\_47 |

**QUESTION**: description on the plant itself should be added

## INTERLOCK SYSTEM

The In

**QUESTION**: how many PLCs do we have and what they control?

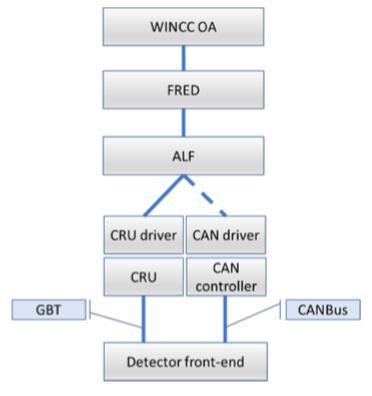
# **DETECTOR CONTROL SYSTEM (DCS)**

## DCS ARCHITECTURE

The Detector Control System is based on commercial SCADA system WINCC OA. It uses a five tier architecture:

1. *Hardware layer*: provides all devices and sensors required for the operation of the experiment.
2. *Hardware abstraction layer*: provides unification of the communication between a large variety of devices and the control system software; it consists of industrial OPC servers.
3. *Control layer*: where the data acquired from the devices are processed; it consists of a farm of servers running a distributed WINCC OA SCADA system. This layer compares parameter values to its limits and take actions if needed. It configures the control devices and sends commands to them. Parameters values and configuration data are stored in an ORACLE database.
4. *Operations layer*: implement all the rules needed to safely operate the detector, representing all devices and channels as finite state machine integrated into a global hierarchy.
5. *User Interface layer*: visualizes all DCS components and their states in a user friendly form, allowing for operation of detector from one workspace by a single operator.

A typical detector front-end module implements the DCS functionality using the CERN developed Slow Control Adapter (SCA) chip interfaced to the GBT link. It provides a wide range of possibilities to access the controlled parameters using multiple busses like JTAG, I2C, parallel I/O bus etc. Although the front-end architectures and DCS requirements of the detectors are largely different, the common SCA-GBT architecture allows for standardization at the software level. The GBT links are controlled by the Common Readout Units (CRU) installed in the FLPs. Here the DCS data is extracted from the data stream and sent to ALF (Alice Low Level Front-end) interface, which publishes the data to the upper layers of the software.



ALF can also receive commands and converts them to data words to be sent to the front-end electronics. To keep the ALF detector neutral, its functionality is restricted to the basic I/O operations. In the current implementation, the ALF can read/write registers implemented on the front-end modules and publish the data using a DIM service. The data published by ALF could be single values, or blocks of data prepared by the electronics modules.

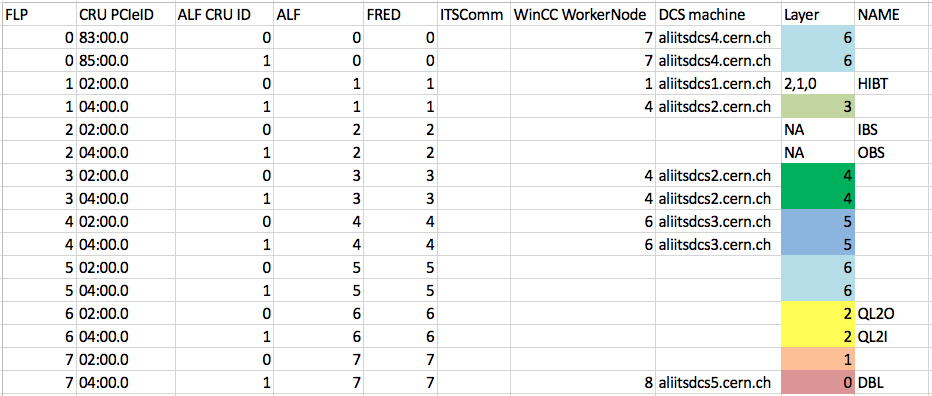
Communication between the WINCC OA systems and the ALFs is managed by the Front-End Device (FRED) module. This layer provides the necessary translation of high level WINCC OA commands to simple ALF transaction and unpacking the ALF data before it is published to the WINCC OA.  
The ALF-FRED architecture decouples the front-end details from the high level SCADA system. Separating this task into 3 layers of software (the drivers, the ALF and the FRED) brings clear advantages:

1. the ALF remains detector independent and can be deployed to all detectors;
2. the FRED layer provides highly customizable detector-specific module which implements all resource intensive calculations, such as data unpacking and first level filtering.

From the WINCC OA perspective, the ALF-FRED behaves as any other standard device.

The present ALF-FRED implementation is based on DIM protocol. It allows for easy integration of complex detector granularity into a coherent system. The ALF modules are installed for each FLP belonging to the same detector and are serviced by a dedicated FRED. The SCADA system recognizes the FRED as a device that recognizes high level commands (such as configure, turn on/off) and publishes its data as single services. It is the task of FRED to translate the high-level commands into a sequence of atomic actions to be carried out by ALF.

The separation of the commands and management of their complexity through the different ALF-FRED layer brings an additional advantage. At the lowest layer, the ALF is interfaced to the CRU through a driver developed in ALICE and takes care of CRU transactions over the GBT link. Replacing this driver allows for use of a different field bus (such as CANbus) without the need of extensive software modifications.



<https://espace.cern.ch/alice-project-itsug-electronics/_layouts/15/WopiFrame2.aspx?sourcedoc=/alice-project-itsug-electronics/Shared%20Documents/Matteo/cru_to_ru_mapping.xlsx&action=default>

Details about FSM and repository for the DCS project:

<https://espace.cern.ch/alicecontrols/projects/_layouts/15/WopiFrame.aspx?sourcedoc=/alicecontrols/projects/Shared%20Documents/ITS%20Workspace/ITS%20DCS%20Description.docx&action=editnew&IsDlg=1>

Monitoring and control notes:

<https://espace.cern.ch/alice-project-itsug-electronics/_layouts/15/WopiFrame.aspx?sourcedoc=/alice-project-itsug-electronics/Shared%20Documents/Gianluca/Monitoring%20and%20Control%20Notes.docx&action=default>

**QUESTION**: probably we need a short description of the DCS structure? Which are the used machines and how they are arranged?

**QUESTION**: how many OPC servers do we have and what they control? CAEN and ...

## DCS PANELS

If your NICE account is recorded in the DCS as an expert user, you can access to the DCS node machines and open all the panel to control and monitor the detector. Control panels are described in the shifter manual. Here will be described the expert panels, used to control the detector.

To open such panels:

1. access to the DCS machine (correct machine depends on the detector layer(s) you want to control, details are reported in paragraph [DCS architecture](#_heading=h.tyjcwt))
2. open “Windows PowerShell”
3. type a command line like: WCCOAui -p panelname.xml -proj its\_wn\_# (where # is the number of **the worker node (not the DCS machine)** that you want to use. Consult the table in [DCS architecture](#_heading=h.tyjcwt) for the layout of the worker nodes.)

where “panelname.xml” is the name of the panel you want to open, as reported in the title of the following paragraphs.

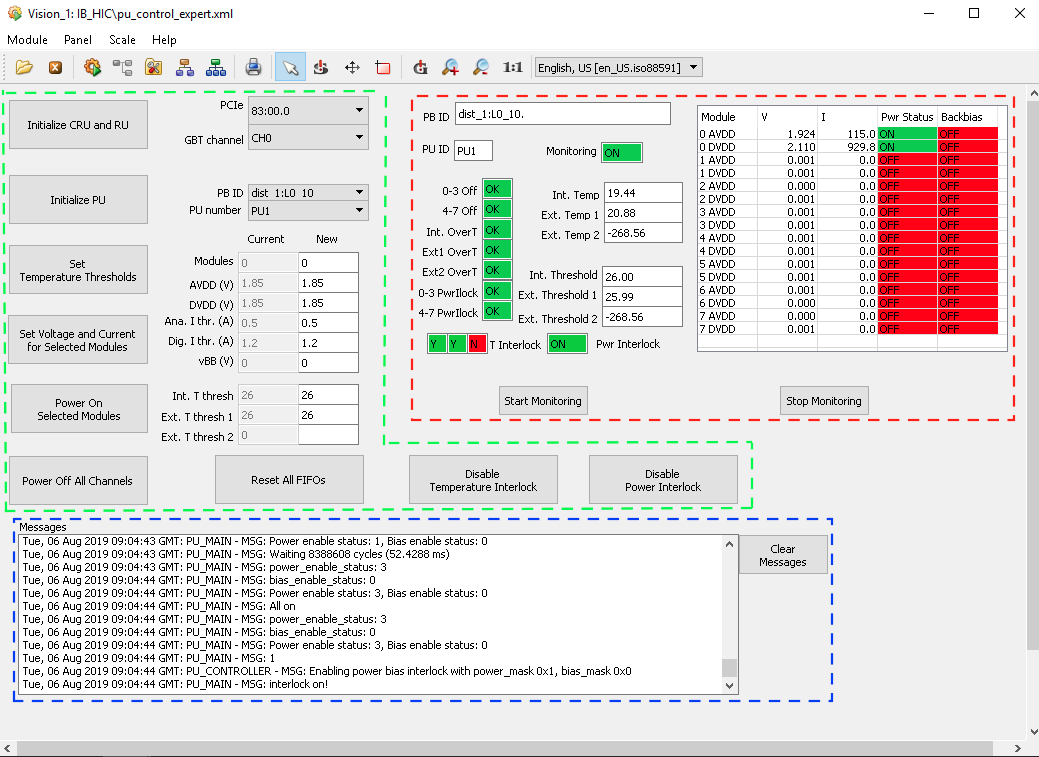
In case there are issues opening a panel using the above method, the more complicated method below will also work:

1. access to the DCS machine (correct machine depends on the detector layer(s) you want to control, details are reported in paragraph [DCS architecture](#_heading=h.tyjcwt))
2. open “Windows PowerShell”
3. type a command line like: # (where # is the number of **the worker node (not the DCS machine)** that you want to use. Consult the table in [DCS architecture](#_heading=h.tyjcwt) for the layout of the worker nodes.)
4. within Gedi, find the panel in the “Project View” pane, right-click, and select “Open in QuickTest Module”. Typically the first place to search is in the green present labeled “its\_wn\_#” (where # means the same as above), and if the panel is not found there, search in “its\_share”. (This is the same search path that WinCC itself uses when running panels directly from the command line. Most of the time, the production panels will only be found in its\_share; they will only be found in its\_wn\_# if there was a modification needed to the panels that has not yet been integrated into the shared repository.) Note that only one panel can be open at a time using this method.

Note: The project ITS\_PowerControl is now deprecated and should not be used for any detector operations. If you have been using this project, please immediately switch to any of the worker nodes described in the table on page paragraph [DCS architecture](#_heading=h.tyjcwt). The panel names below are only accurate for these worker nodes.

### expertPanels\pu\_control\_expert.xml

This is the main panel to be used to switch ON the detector.

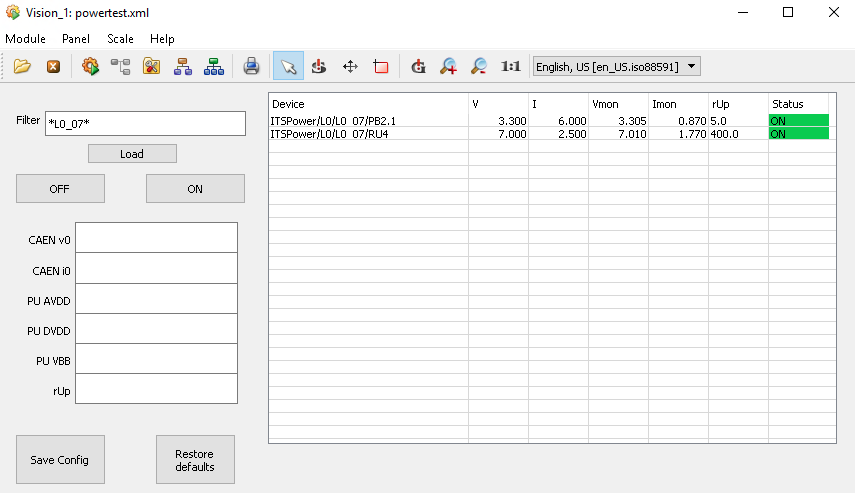


Relevant sections and buttons:

* Control section (highlighted in green)
  + Following buttons are available in this section: “Initialize CRU and RU”, “Initialize PU”, Set Temperature Threshold”, “Set Voltage and Current for Selected Modules”, “Power ON Selected Modules”, Power Off All Channels, “Reset All FIFOs”, “Disable Temperature Interlock”, “Disable Power Interlock”
  + Parameters value can be set in the fields: “Modules”, “AVDD (V)”, “DVDD (V)”, “Ana. I thr. (A)”, “Dig. I thr. (A)”, “vBB (V)”, “Int. T thresh”, “Ext. T thresh 1”, “Ext. T thresh 2”
  + Following dropdown menu are available to select the board on which apply the configuration: “PCIe”, “GBT channel”, “PB ID”, “PU number”
* Monitoring section (highlighted in red)
  + Following display fields are available: “PB ID”, “PU ID”, “Int. Temp”, “Ext. Temp 1”, “Ext. Temp 2”, “Int. Threshold”, “Ext. Threshold 1”, “Ext. Threshold 2”. Furthermore for the 8 channels of the PU, both for digital and analog line, voltage and current value, and two leds “Pwr Status” and “Backbias”
  + Following leds: ”0-3 off”, “4-7 off”, “Int. OverT”, “Ext1 OverT“, “Ext2 OverT“, “0-3 PwrILock”, “4-7 PwrILock”, 3 “T Interlock” leds, “Pwr Interlock”
  + Two buttons: “Start Monitoring” and “Stop Monitoring”
* Messages section (highlighted in blue)
  + Big display field where all the messages related to the actions executed by the DCS are show
  + “Clear Messages” button

### expertPanels\CAEN\_control.xml

This is the main panel to be used to switch ON the RU and PU.

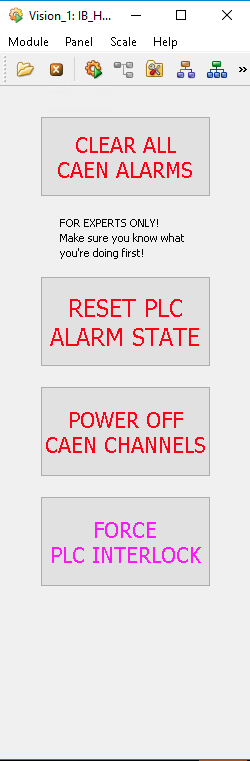


Relevant buttons and fields are:

* “Filter” field connected to the “Load” button to search for needed channel(s). Results of the search will appear in the table on the right side of the panel. Each line in this table contains the following columns: “Device”, “V”, “I”, “Vmon”, “Imon”, “rUP”, “Status”
* “ON” and “OFF” button to switch ON/OFF the channel(s) selected with the filter
* Section to define and save configuration
  + Fields: “CAEN v0”, “CAEN i0”, “PU AVDD”, “PU DVDD”, “PU VBB”, “rUP”
  + Buttons: “Save Config” and “Restore default”

### expertPanels\clear\_alarm.xml

This is the main panel to clear alarms or to apply emergency shutdown.



Relevant buttons and fields are:

* “CLEAR ALL CAEN ALARMS”
* “RESET PLC ALARM STATE”
* “POWER OFF CAEN CHANNELS”
* “FORCE PLC INTERLOCK”

DEBUG IN CASE OF PROBLEM

Relevant butt

Two are the log files that could be checked looking for the reason of a strange behaviour of the detector system:

1. ALF log on the itsflp# machine

ALF server is stored in each flp machine in the folder:

**/opt/ALFServer-ITS**

To verify the status of the server:

**systemctl status alf**

The log of the alf activities is stored in the following folder:

**/data/alf.service.log**

1. ITSComm log on the aliitsdcs0 machine

ITSComm server is stored in each dcs machine in the folder:

**/opt/ITSCommLayer-ITS**

To verify the status of the server:

**systemctl status ITSCommLayer@{0..7}**

To restart the server:

**systemctl start ITSCommLayer@#**

where # is the number of the server that want to be re-started.

The log of the ITSCOmm activities is stored in the following folder:

**/data/ITSCommLogs**

# **DATA ACQUISITION – RUN MANAGER (DAQ)**

## DAQ ARCHITECTURE

**Following are notes provided by Miko and are mainly true for HIB-T through itsflp1**

To use the Run Control panel in the DCS, one has to activate the corresponding server in each flp. The python script that activate the server is located in the folder:

**/home/its/shifts/ib-commissioning-tools**

and is called:

**run\_control\_server.py**

The server is expected to run in a dedicated tmux session; usually this is the tab 0 in tmux, that is called “rcs”. To connect directly to this dedicated tmux session: **tmux a -t rcs**

To check the list of the tmux sessions open in the flp: **tmux ls**

In case the flp shut down, the command to open a new “rcs” session in tmux is: **tmux new -s rcs**

Before starting the server it is needed to launch in the terminal the command:

**rc**

To start the run control server the command is:

**./run\_control\_server.py IBT --expert --dry**

where:

* IBT = define the configuration and is related to the fraction of detector available; IBT and HL2 are the two options available in the itsflp1
* --expert = add a prefix in the logbook entry created for each run and include more details in the report
* --dry = allow to perform a run that do not expect any data from the staves and that can be performed having the staves not powered

There exist a configuration file for the run control server:

**/home/its/shifts/ib-commissioning-tools/config/setup.cfg**

The only interesting part, in case a fraction of the detector needs to be excluded, is in the two parameters:

* *crtl\_and\_data\_link\_list*

This parameter is used to specify the list of the links to be configured; in the case of the HIB-T goes from 0 to 23. Correspondence to the staves is: 0 —> L2\_00, …, 9 —> L2\_09, 10 —> L1\_00, …, 17 —> L1\_07, 18 —> L0\_00, …, 23 —> L0\_05.

List of staves to be included can be provided also in this way: 0-11,13,17-21,23

Note that when a stave is excluded in this list, it has to be excluded also in the readout, as we will see below.

* *exclude\_gth\_dict*

This parameter can be used to exclude a chip, using the sintax: **{"L0\_03":[3]}** to exclude chip 3 in the stave L0\_03.

As anticipated, there is a second configuration file containing the list of the links included in the readout. This file has to be modified if a stave is excluded from the configuration list. The file is:

**/home/its/shifts/ib-commissioning-tools/config/readout\_ibt\_1gbtlink\_lz4.cfg**

or

**/home/its/shifts/ib-commissioning-tools/config/readout\_hl2\_1gbtlink\_lz4.cfg**

depending of the fraction of the detector is going to be used. Actually the second file is filled with values good to run only the staves in the HL2-T.

In this file the interesting part is the parameter *linkMask*. Actually there are two of these parameters, one for each RORC within the CRU. For the HIB-T the division of the staves between the two RORCs is the following:

- RORC1

channels 0-9 —> L2\_00 to L2\_09

channels 10-11 —> L1\_00, L1\_01

- RORC2

channels 0-6 —> L1\_02 to L1\_07

channels 7-11 —> L0\_00 to L0\_05

If the removal of the link is not properly done a readout.exe error is reported in the run control messages.

There exist also a python script to avoid to use the run control panel in the DCS; it is locate in folder:

**/home/its/shifts/ib-commissioning-tools**

and can be launched with the following command and options:

**./run\_test\_rc.py <det> <scan> <option>**

where:

* <det> = IBT or HL2
* <scan> = Threshold, FakeHitRate, ReadoutTest
* <option> = --skip or a configuration file

## DAQ PANEL

## SCANS

and Digital current

# PROCEDURES

## RESET INTERLOCK ALARM

This requires that the cause that triggered the interlock has been solved.

In [expertPanels/clear\_alarm.xml panel](#_heading=h.6cbsld1ai9ip) following sequence of actions have to be executed:

1. RESET PLC ALARM STATE
2. CLEAR ALL CAEN ALARMS

**QUESTION:** how to check if there is an active interlock?

ANSWER: a panel will be implemented in the DCS to allow a fast check on this; for the time being one has to look at the PLC leds in the back of the DCS PCs rack and at the front of the CAEN modules.

**QUESTION**: is there a way to visually check that the command has been actually propagated and that the alarms are actually cleaned?

ANSWER: this will become possible once the DCS panel for the interlock status will be available

## SWITCHING ON/OFF RUs AND PUs

This requires that no interlocks are active and that the CAEN system is ON.

In [expertPanels\CAEN\_control.xml panel](#_heading=h.8lju3ybd4yhm), the following sequence of actions have to be executed to power the needed RUs and PUs:

1. Power reverse-bias channels
   1. Type in the Filter a string like “\*vBB\*” and click on “Load” button   
      → a list of channels corresponding to the -5V supply for the PU will be shown
   2. Click “ON” button, to switch ON all the channels listed   
      → Status will become GREEN with “ON” text
      1. Typical current values are: Imon = 0.4 mA (value to be checked)
2. Power RU and PU
   1. Type in the Filter a string like “\*L0/L0\_06/\*” and click on “Load” button   
      → a list containing for each stave one line for the PU and one for the RU will be shown
      1. you can choose the best string to select the list of channels you need
   2. Click “ON” button, to switch ON all the channels listed   
      → Status will become GREEN with “ON” text
      1. Typical current values for PB are: Imon = 1.4 mA (value to be checked)
      2. Typical current values for RU are: Imon = 1.8 mA (value to be checked)

The same panel can be used to switch OFF RUs and PUs.  
Before doing so, be sure that the corresponding staves are OFF.  
As done in powering ON procedure, select the channel using the Filter field and click on “OFF” button.  
As in the previous case, the “OFF” action will be execute over all the channels listed in the panel.

## CONFIGURE AND SWITCHING ON/OFF Staves

This requires the RUs/PUs and BB channels are ON for the staves that is going to be powered.

In [expertPanels/pu\_control\_expert.xml panel](#_heading=h.ru2k1sjkuikm), the following sequence of actions have to be executed to switch ON a stave:

1. Initialize CRU and RU
   1. Select the correct group of CRUs/RUs from the dropdown menu
   2. Click on the “Initialize CRU and RU” button

This action can be done just once for all the staves belonging to this group of CRUs/RUs

1. Switch ON Monitoring on all the channels (repeat the below sequence for all the staves)
   1. Select the Stave to be powered in the dropdown menu “PB ID”
   2. Click the “Initialize PU”
   3. Insert the following values for Modules = 0, AVDD (V) = 1.8, DVDD (V) = 1.8, Ana. I thr. (A) = 0.5, Dig. I thr. (A) = 1.2, vBB = 0 (or -3), Int. T thresh = 26, Ext. T thresh 1 = 26, Ext. T thresh 2 = empty
   4. Click on “Set Temperature Thresholds”
   5. Click on “Start monitoring”
2. Switch ON staves (repeat the below sequence for all the staves)
   1. Click on “Power On Selected Modules”

To be sure that the PU initialization succeeded, the following string must appear in the Messages panel: Command cruinit pp1o4\_hl0 exited with code 0 (the name of the stave can change).

In the Messages panel, the following string must appear in case of successful powering:

“” (to be defined)  
In case of failure, repeat again step f) in point 2).

Typical values for currents, just after the switching ON, are: analog channel ~100 mA, digital channel ~400 mA.  
The same panel can be used to switch OFF the staves.  
As done in powering ON procedure, select the stave in the dropdown menu “PB ID” and click on “Power OFF All Channels” button.

In some cases you could also need to disable the Monitoring: click on “Stop Monitoring” button. Do not perform this action when the stave is powered ON.

## SWITCHING ON THE DETECTOR FROM SCRATCH

Only Expert user can switch ON the detector.

PC: the dcs machine depends on the layer to be switched ON (DBL: aliitsdcs5.cern.ch)   
User: aliceits

Password: ask Felix/Domenico

The sequence to be followed is:

→ [RESET ALARMS](#_heading=h.2s8eyo1)

→ [SWITCH ON RU AND PU](#_heading=h.bgwbgabczsxc)

→ [CONFIGURE AND SWITCH ON STAVES](#_heading=h.8ax0o93yebtr)

## RE-INITIALIZE CRU

Be sure that all the CAEN channels related to the CRU you want to r-initialize are ON!

~~~only for DBL~~~

ssh its@flpits7

cd /shareFS/its/shifts/CRU\_ITS/software/py

aliswmod enter ReadoutCard/v0.11.4-1

./testbench\_pp1o4\_hl0.py cru initialize

~~~FOR THE OTHER LAYERS~~~

cd

commands are the same, but the last line:

./testbench\_<subrack>.py cru initialize

where <subrack> identify the subrack where the layer is located and has to be identified.

## LIST OF RECORDED RUN

To have a full list of runs taken, ordered by start of run time:

>> ssh its@flpits7

>> cd /home/its/shifts/ib-commissioning-tools

>> rc

>> ./list\_runs\_.py DBL

## LIST LAST ERRORS IN A RUN

To have the list of the last errors during a run:

>> ssh its@flpits7

>> cd /data/shifts/logs

>> tail -f rcs\_DBL\_debug.log

## CLEANUP DISK SPACE ON THE FLP

In the FLP the data are collected in folder:

/data/shifts/runs

At the moment, an rsync process is copying the run folders to EOS in the following path:

/eos/project/a/alice-its/Commissioning/flpits7\_DBL (for the DBL)

The user to access to EOS to check the list of the transferred files has to be:  
 ssh -Y [aliceits@lxplus.cern.ch](mailto:aliceits@lxplus.cern.ch)

**QUESTION**: How to access to the CAEN to check if the powering is actually on? (GEKO)

# **QUALITY CONTROL (QC)**

QC ARCHITECTURE

A

**BACKUP**