sPHENIX Prototype Hadronic Calorimeter Preamp

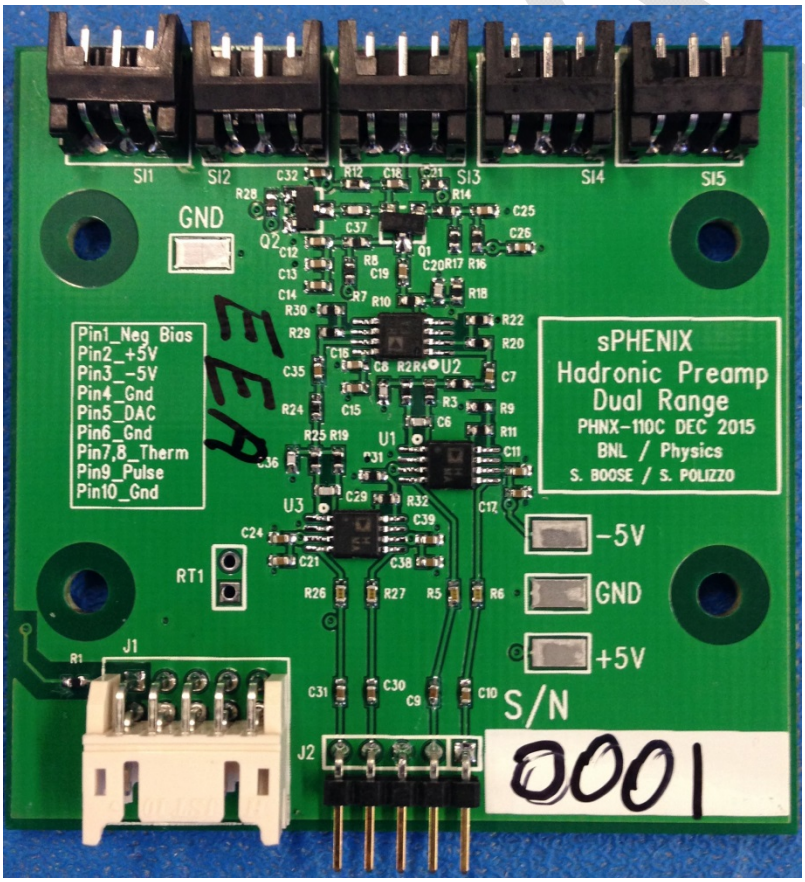
PHNX-110C "Prototype C"

Revised 6/16/16

Introduction

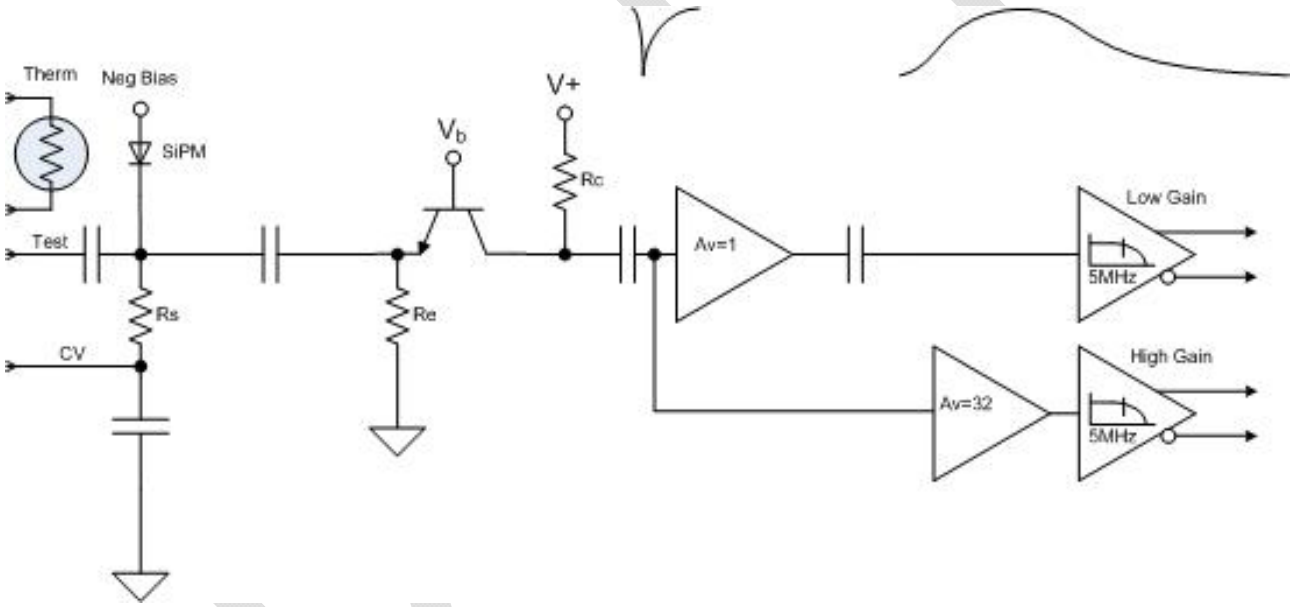
The PHNX-110 preamp board is a common-base amplifier with added voltage gain stages and multipole-filter differential output drivers to appropriately shape and drive signals to the Nevis ADC module. Two gain ranges, each with its own differential signal output are provided. Revision C differs from Revision A in that the supplies are now +-5V, the I/O connectors are now parallel to the board and the SiPM connectors have been changed to a type that is easier to use. Low voltage and negative bias supplies, DAC control input, Test Pulse input and Thermistor output are all connected to the board through J1. Up to five SiPMs are connected in parallel to the input via Hirose DF3 2mm connectors. Output connector J2 is a 2mm header which conforms to the pin assignment for the Nevis ADC allowing output polarity reversal by simply rotating the connector. A single Meritec cable is normally connected to this header.

PHNX-110-C Preamp



Functional Description

The first stage amplifier utilizes a common-base (CB) configuration which provides characteristics appropriate for amplifying SiPM sources such as low input impedance across a broad frequency range and good stability. The output of the CB is amplified and sent to two separate output drivers, one with 32 times the voltage gain of the other. SiPM bias is returned through a load resistor whose return node is set to a positive voltage of 0-5V from J1-5 to allow remote bias trimming. Leads from the thermistor are passed through the cable on J1-7 and J1-8. A cascode-driven 1pF capacitor is also connected to the input node for functional testing purposes and is triggered by a positive TTL pulse J1-9. For general use as a preamp for bench testing one can just short all wires from J1-5 to J1-10 to ground.



Connectors

(The color code of the enclosed cable is shown)

J1 Power and Control Connector B10B-PHDSS mates with PHDR-10VS

J1-1 Negative Bias	(RED/ BLK Stripe)
J1-2 +5V @ 38mA (typ)	(BLK/RED Stripe)
J1-3 -5V @ -38mA (typ)	(WHI/BLK Stripe)
J1-4 Gnd	(BLK/WHI Stripe)
J1-5 DAC Input	(GRN/BLK Stripe)
J1-6 Gnd	(BLK/GRN Stripe)
J1-7 Thermistor_1	(BLU/BLK Stripe)
J1-8 Thermistor_2	(BLK/BLU Stripe)
J1-9 Pulse In	(YEL/BLK Stripe)
J1-10 Gnd	(BLK/YEL Stripe)

J2 Output 2mm Header mates with 2mm HardMetric connector

J2-1 Low Gain Negative Output

J2-2 Low Gain Positive Output

J2-3 Shield Gnd

J2-4 High Gain Negative Output

J2-5 High Gain Positive Output

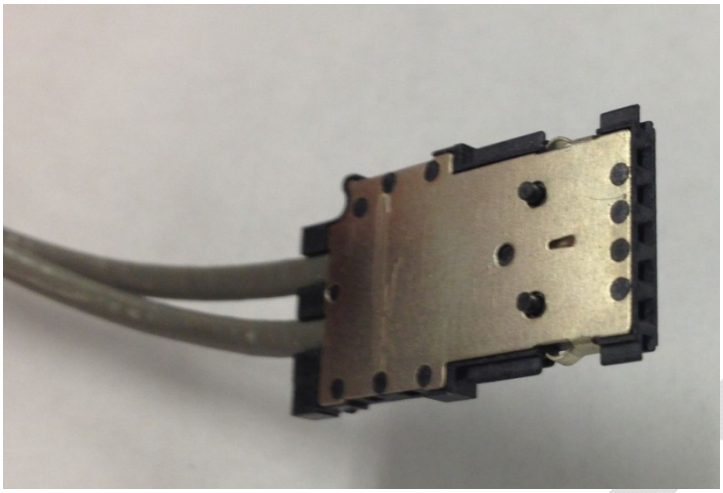
Si1 – 5 Connectors

1 SiPM Anode

2 SiPM Cathode

3 Shield

Meritec Cable



Example Test Pulse (High Gain Channel)