Open the project in vivado HLx 2019.1: Base_system_0227 → infer_whole_sys → infer_whole_sys.xpr (shown in Figure 1)

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🍌 infer_whole_sys.xpr	2/28/2020 10:16 AM	Vivado Project File	12 KB

Figure1. Vivado project.

After opening the project, the vivado window looks like the Figure 2.

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Figure 2. Window after opening the project.

2. Generating bitstream:

Click "Generate Bitstream" under PROGRAM AND DEBUG

3. After generating the bitstream successfully, export the hardware as shown in Figure 3.



Figure 3. Export Hardware.

4. Launch SDK:

Launching the SDK as shown in Figure 4.

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Figure 4. Launch SDK.

After launching the SDK, the window looks like Figure 5.



Figure 5. SDK workspace.

5. Import SDK project:

Importing the SDK project as shown in Figure 6.

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					 Select root directory: Select archive file: 	E:\Base_system_0227\infer_whole_sys\sdk	-	Browse
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Figure 6. SDK project importing.

6. Project C code:

We then can modify the C code in "helloworld.c", and this C code will run on the soft CPU IP core (Microblaze) on the FPGA. The "helloworld.c" is shown in Figure 7.

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🎦 Project Explorer 🐹 📄 🔄 🔽 🗆	🗊 system.hdf 🛛 🔂 helloworld.c 🐹
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Figure 7. C code run on the FPGA soft CPU IP core.

- Modify the "helloworld.c" code. Replace the code in "helloworld.c" with the code in the "helloworld_mod.c", "helloworld_mod.c" Is located under Base_system_0227.
- 8. Replace the content in "lscript" under SW→src with the content in the "lscript_mod.c", "lscript_mod.c" Is located under Base_system_0227.
- Clean project:
 Saving the modified C code and cleaning the project as shown in Figure 8.

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Figure 8. Project cleaning.

10. Open the Tera Term for data transferring between Computer and FPGA: Opening the Tera Term and set it up ad shown in Figure 9 by clicking setup→Serial port.

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Tera Term - [disconnecte	ed] VT Window Hala				×	Port:	СОМ4	•	ОК	
Tera Tern	m: New connection		×	-	^ 0	Baud rate: Data:	115200 8 bit	•	Cancel	
С тс	CP/IP Host:	myhost.mydomain ☑ Telnet TCP port#;	- 23		-	Parity: Stop:	none 1 bit	•	Help	
© Se	erial Port:	COM4 -				Flow control:	none	•		
	ОК	Cancel Help			t T	Transmit delay	/char 0	mse	c/line	

Figure 9. Tera Term setup.

11. Configure FPGA:

Configuring the FPGA as shown in Figure 10. SDK Program FPGA × Program FPG/ Search Debug ~ Ō Specify the bit: • • New folder Hardware Con Hardware Platfweight Name Date modified Туре Size Connection: ume (E:) 2/28/2020 10:16 PM File folder Device: SW.elf 2/28/2020 10:16 PM ELF File 279 KB Bitstream: Partial Bitstr infer_sys_wrapper.mmi BMM/MMI File: rch... Browse.. Software Configuration ELF/MEM File to Initialize i ock RAM Processor E:\infer_whole_sys\infer_whole_sys.sdk\SW\Debug\S.. microblaze_0 < > ? Program Cancel

Figure 10. FPGA configuring.

12. Sending data (in binary format) in the LeNet7_weight folder from computer to FPGA based on the information appeared on Tera Term.