CERN, May 12th, 2020

Towards ITS3 sensor development

G. Aglieri Rinella and W. Snoeys

Discussion with foundry still ongoing

- Several 65 nm flavors
  - high density logic
  - RF
  - imaging (ISC).

- ISC preferred : 2D stitching experience, special sensor features, lower defect densities, etc, but limited to 5 metal layers (4 thin + 1 thick), no MPWs available.

Proposal:

start in ISC with Multiple Layers per Reticle with standard metal stack

- Avoid not representative results, more and thicker metals later
- Multiple Layer per Reticle 1 x 1.5 cm^2
    - cost in between MPW and engineering run
    - minimizes Tower's burden for gds/MLR assembly (using template)
- Several starting materials (can use same readout) among which:
    - one more conventional for Alpide-like,
    - (stacked or not) photodiode for increased radiation tolerance
- 2 MLRs instead of MPWs + engineering runs, first MLR ~ September to efficiently use the area

- Still need final proposal validation/endorsement by the foundry
    - needs balance with support resources

Status at CERN

- Rudimentary design environment in place at CERN
- Working on:
  - Simple test structures (transistors, small pixel matrices…)
  - Need to define standard interfaces/test setups…
- Target MLR in the fall including also a demonstrator to use large available area efficiently
- After proposal validation provide access to other groups.

Transistor test structures (Geun Hee Hong and Wenjing Deng)

- First layout finished. Found relatively large gate leakage currents in 1.2 V devices for ISC, have now recently added a structure including 3.3 V devices.

- Compatible with standard probe card at CERN. Testing probably at CERN.

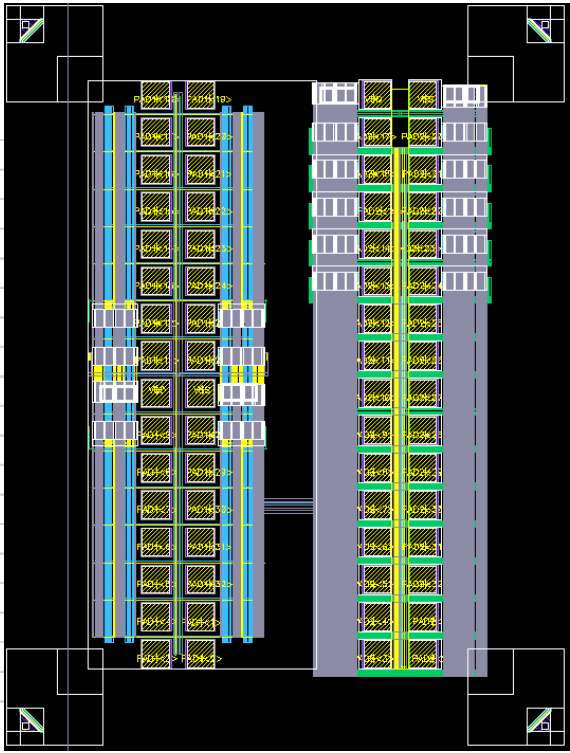
- ISC: 2 sets of probe pads, foot print ~ 1.8 by 2.5 mm^2 (2 x, 1.2 and 3.3 V)

- Also prepared test structure in RF (3 by 2.5 mm^2).
  - Very different process with more transistor flavors => larger test structure for logic/rf.

Transistor test structures (Geun Hee Hong and Wenjing Deng)

		1	SLVt/ W&L Array		
SLVt	gate oxide	18	pMOS SLVt 5.0x6.0	nMOS SLVt 5.0x6.0	19
	STI	17	pMOS SLVt 0.20x6.0	nMOS SLVt 0.20x6.0	20
	Min. Size	16	pMOS SLVt 0.20x0.10	nMOS SLVt 0.20x0.10	21
LVt	gate oxide	15	pMOS 5.0x6.0	nMOS 5.0x6.0	22
	STI	14	pMOS 0.20x6.0	nMOS 0.20x6.0	23
	Min. Size	13	pMOS 0.20x0.10	nMOS 0.20x0.10	24
		12	gate1 P	gate1 N	25
		11	pSOURCE	nSOURCE	26
		10	VDD	VSS	27
		9	gate2 P	gate2 N	28
LVt	Diff. W	8	pMOS 0.40x0.10	nMOS 0.40x0.10	29
		7	pMOS 0.60x0.10	nMOS 0.60x0.10	30
		6	pMOS 1.00x0.10	nMOS 1.00x0.10	31
	Diff. L	5	pMOS 1.00x0.20	nMOS 1.00x0.20	32
		4	pMOS 1.00x0.50	nMOS 1.00x0.50	1
		3	pMOS 1.00x1.00	nMOS 1.00x1.00	2

	2	Diff. Bias (LVt)		
	18	VDD	VSS	19
	17	pSOURCE	nSOURCE	20
	16	pGATE1_diff_bias	nGATE1_diff_bias	21
	15	pGATE2_diff_bias	nGATE2_diff_bias	22
	14	pGATE3_diff_bias	nGATE3_diff_bias	23
	13	pGATE4_diff_bias	nGATE4_diff_bias	24
Min. Size	12	pDRAIN1_0.20x0.10	nDRAIN1_0.20x0.10	25
Narrow/Long	11	pDRAIN1_0.20x10.0	nDRAIN1_0.20x10.0	26
Wide/Short	10	pDRAIN1_1.0x0.10	nDRAIN1_1.0x0.10	27
Min. Size	9	pDRAIN2_0.20x0.10	nDRAIN2_0.20x0.10	28
Narrow/Long	8	pDRAIN2_0.20x10.0	nDRAIN2_0.20x10.0	29
Wide/Short	7	pDRAIN2_1.0x0.10	nDRAIN2_1.0x0.10	30
Narrow/Long	6	pDRAIN3_0.20x10.0	nDRAIN3_0.20x10.0	31
Wide/Short	5	pDRAIN3_1.0x0.10	nDRAIN3_1.0x0.10	32
Narrow/Long	4	pDRAIN4_0.20x10.0	nDRAIN4_0.20x10.0	1
Wide/Short	3	pDRAIN4_1.0x0.10	nDRAIN4_1.0x0.10	2



- 3.3 V device structure similar

Pixel sensor test structures

- Analog readout (Francesco Piro, Wenjing Deng and Geun Hee Hong)
  - Limited to a smaller number of pixels

- Digital readout (Leonardo Cecconi)
  - More practical for larger sensitive areas with many pixels
  - Can be vehicle to prototype a possible architecture (among several)
  - Need comparator (ultimately need compact and low power, not immediately)

MLR submission (“September”)

- Transistor test structures, likely to be tested at CERN
- Elementary analog pixel test structure
- Possibly digital pixel test structure/small demonstrator, requires comparator
- Ring oscillators
- Possibly SEU chip (need elementary digital flow)
- Opportunity for early IP and front end validation
    - Desirable : bandgap, DACs
    - Possibly PLL + built-in regulator

Further activities this year

- Draft full plan and start regular meetings with other groups sharing work
- Improve design environment, digital libraries, special DRC checks
- Architecture studies (some activity in 180 nm for the back up solution ?)
- Need to go through the submission process to understand turn-around time
- After positive feedback of first results: (may run into next year)
  - Put full digital flow in place (outsource ?)+ frame contract
  - More general access to the technology
- If negative revert to 180 nm as back up solution

Conclusions

- Proposal for ISC 65 nm waiting for foundry validation
- After proposal validation work on access for other groups.
- MLR is larger submission, some delay to use area more efficiently.
- Will re-contact groups and start regular meetings soon