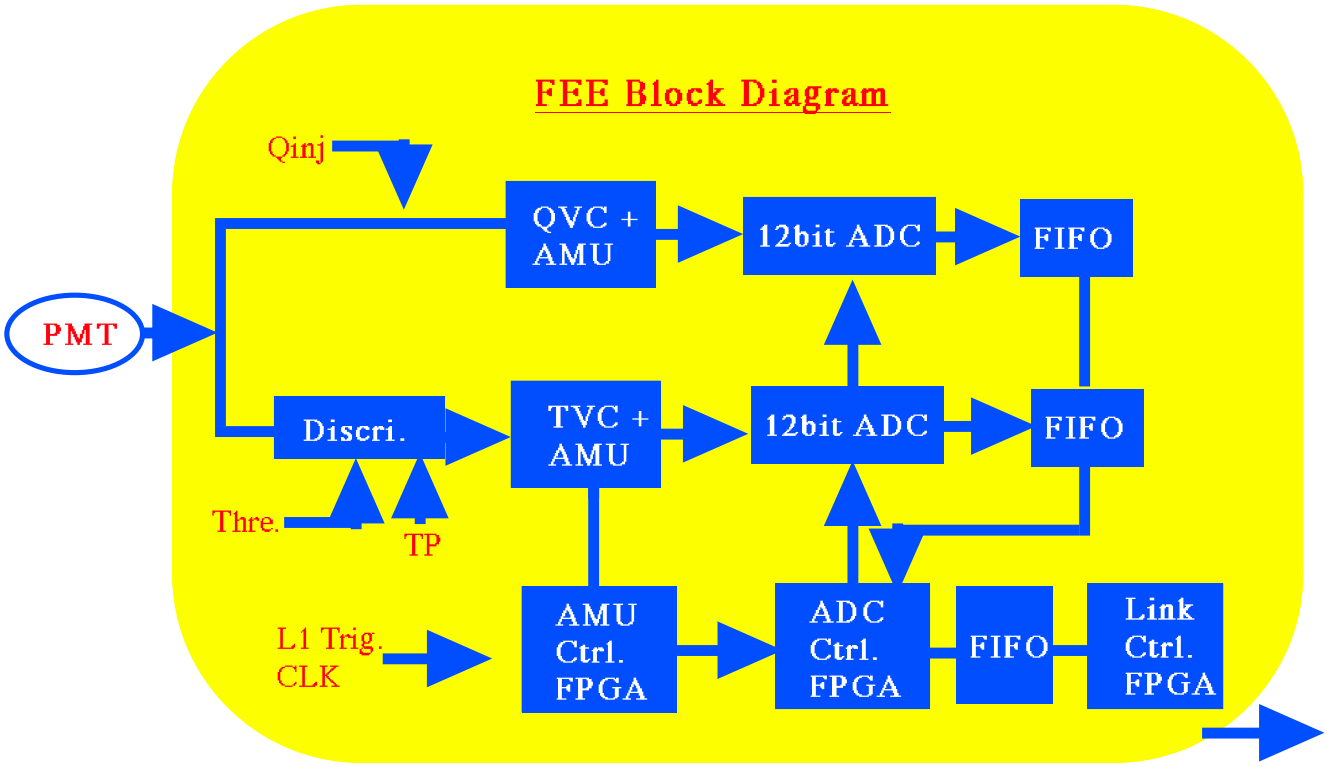
PHENIX TOF FEE overview

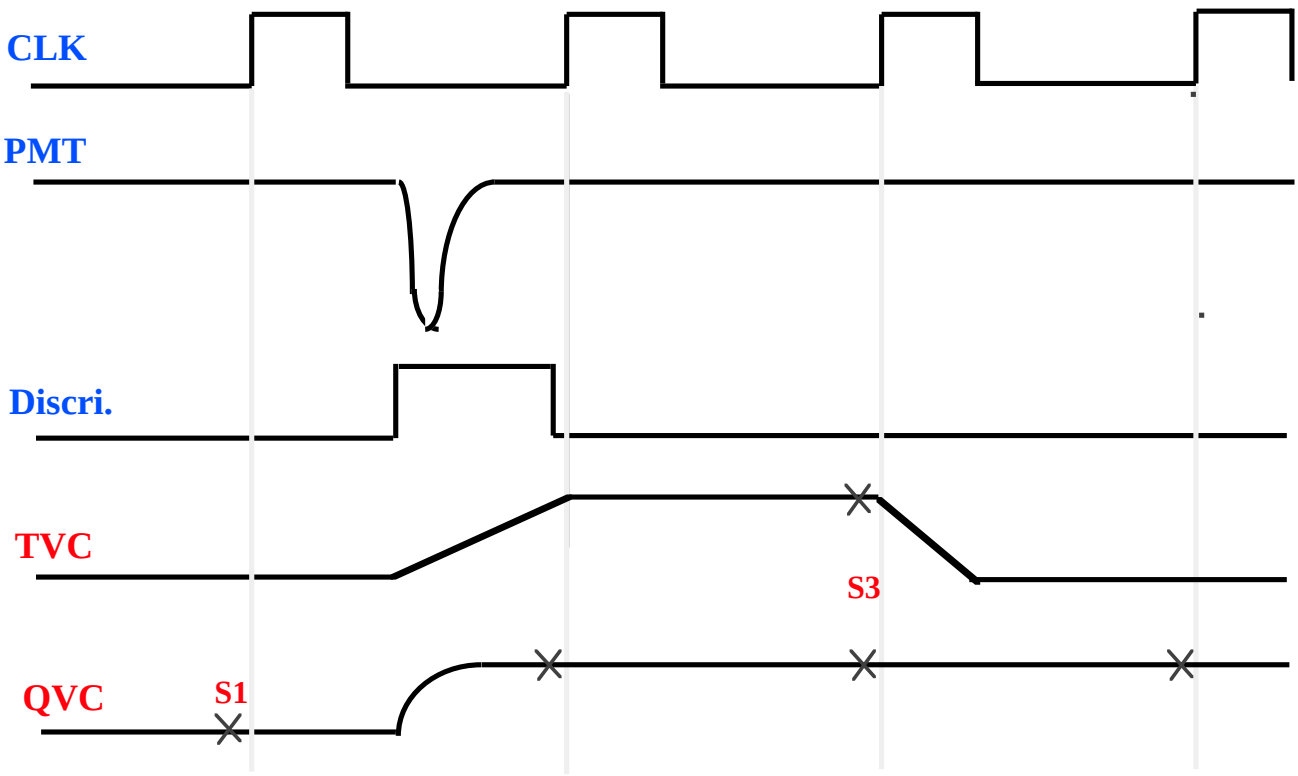
- FEE introduction
- What we learned on test bench + test beam
- WA98 setup
- Time resolution of WA98 Start counter
- FEE revision history and mass production
- Conclusion

PHENIX TOF FEE Block Diagram



- **Pipeline TVC/QVC system (custom chips)**
- **Use of Analog Memory Unit**
- **programmable delay up to 4 micro sec**
- **sample up to 4 consecutive AMU cells per event**
- **Overall timing resolution < 25ps**
- **1000 ch in operation in WA98 (till Nov. 25)**

AMU Sampling



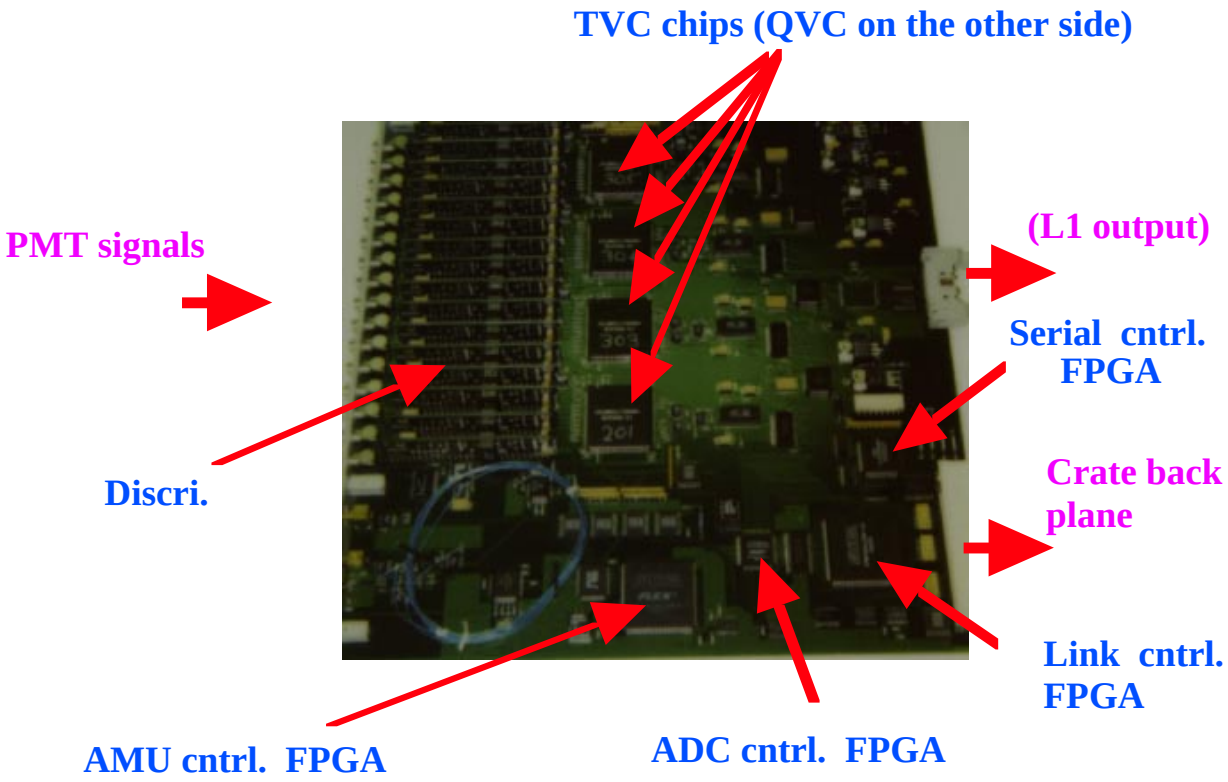
1, TVC takes 3 CLK cycles (charge up, sample, reset) per valid hit --> rate limited by this fact

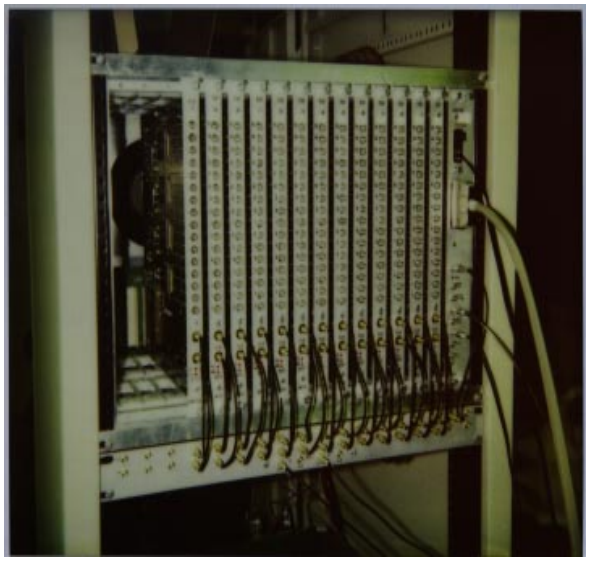
2, QVC samples each CLK cycles

3, In this example, TVC s3 <-> QVC s3 - QVC s1

4, External QVC reset NIM pulse is sent regularly

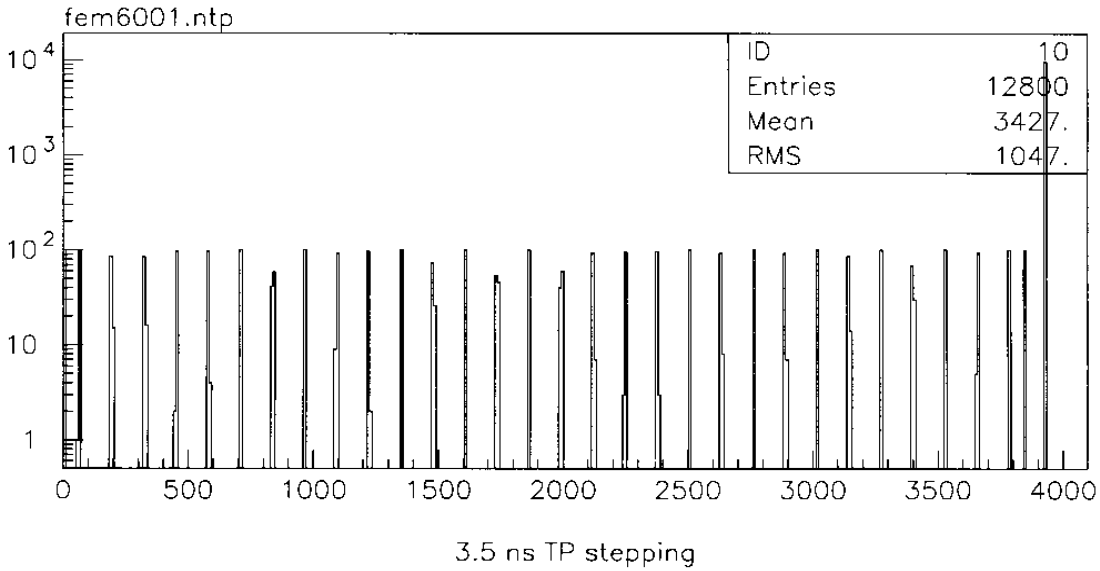
PHENIX/WA98 FEE





Crate filled with FEE boards

TVC Test Pulse results



3.5 ns step Test Pulse

1, 3.5 ns TP is generated by system clock module

2, Number of steps from the edge of the system clock can be specified

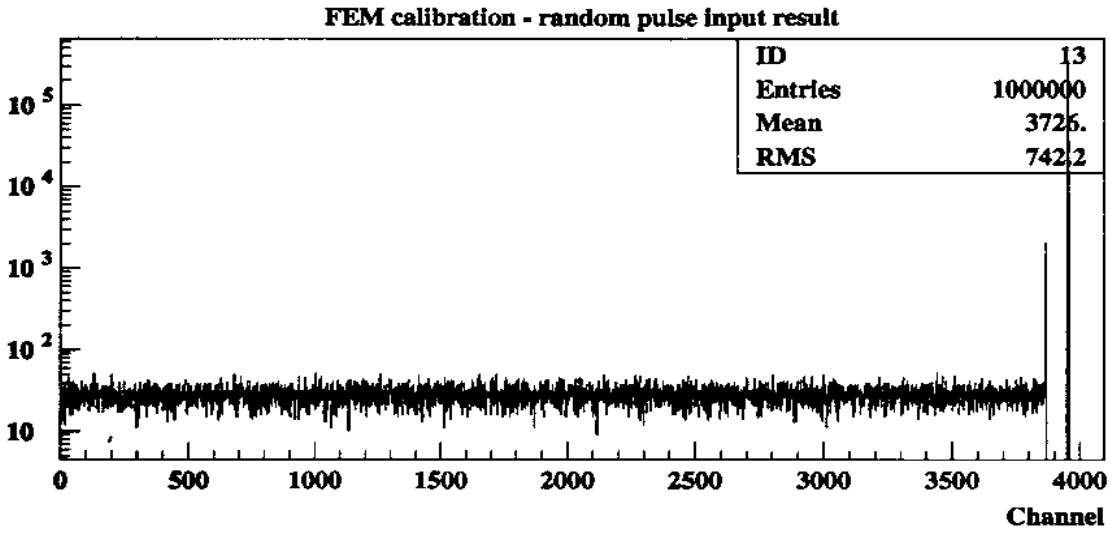
3, TVC value distinct from pedestal when there's a hit -----> efficiency 100%

4, Used to get the time constant + linearity check

5, AMU cell dependence was not seen

6, Peak width < 1ch ---> time resolution ~ 25 ps
cross talk negligible

TVC Random Pulse Input



Random pulse input to TP

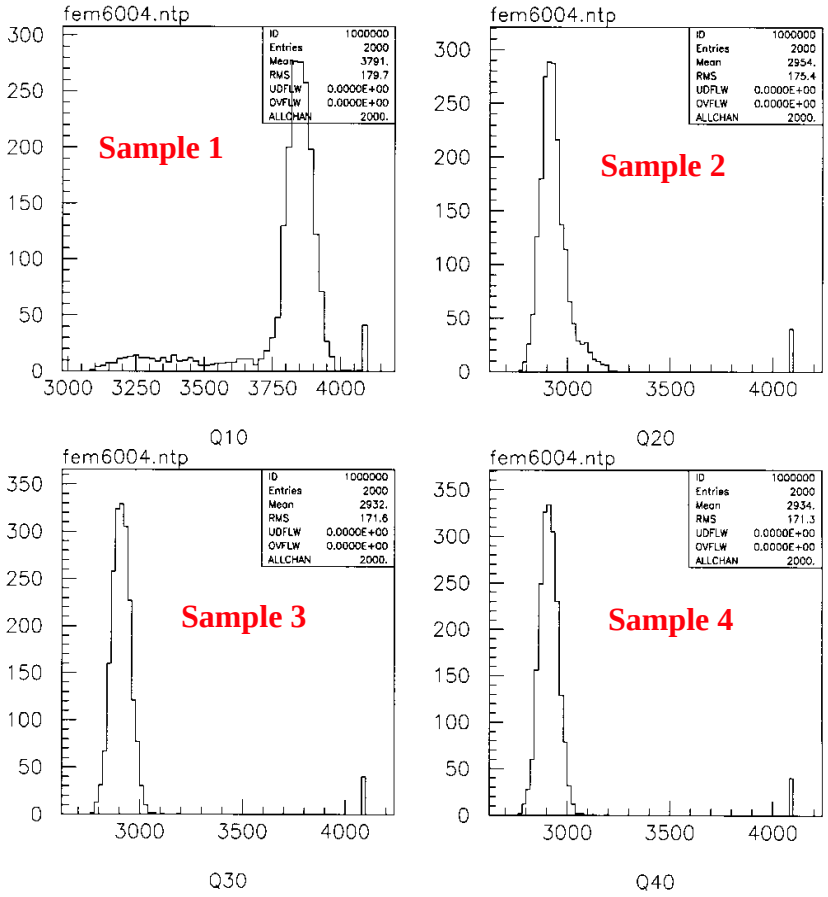
1, Fills 3.5 ns gaps --> No dead region in active range

2, Flat distribution --> another linearity check

3, Clear separation from pedestal

4, Hits in dead region pile up around 3900

QVC Qinj Results

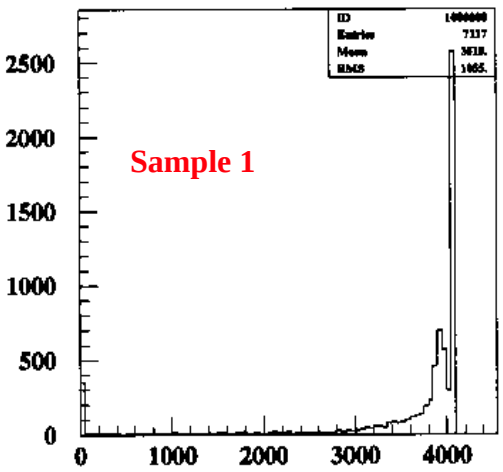


1) Charge to be injected adjustable by DAC

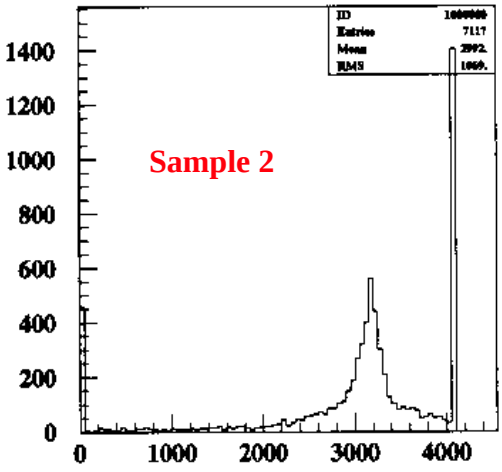
2) Injection timing determined by external NIM pulse

3) Q Injected in 2nd sample in this example

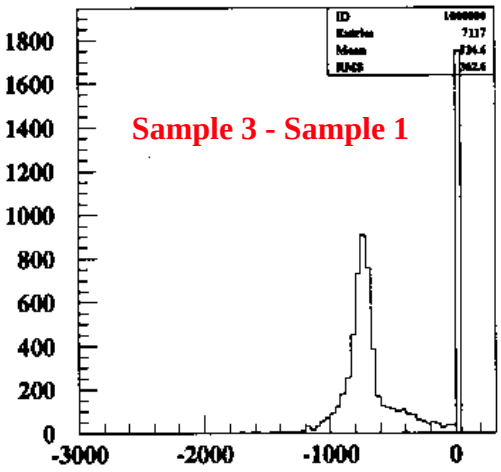
QVC Measurement



Q16



Q36



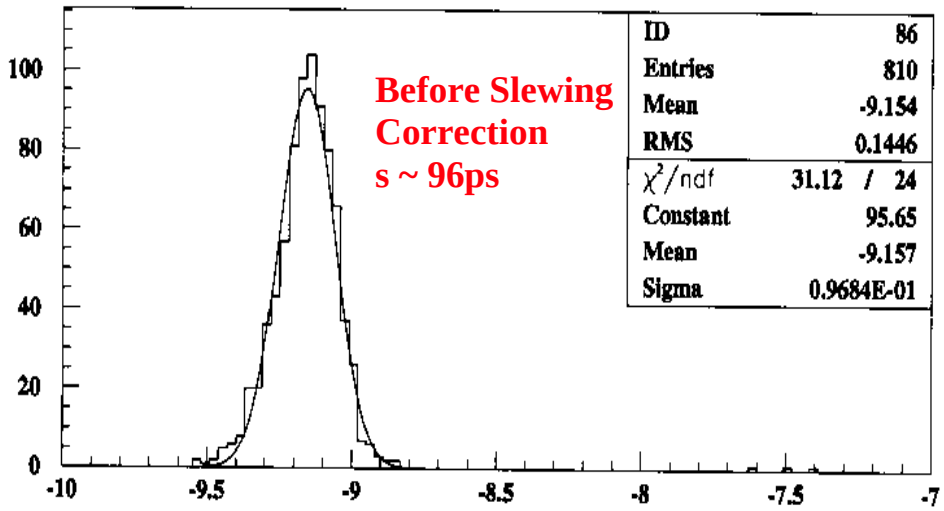
(Q36-Q16)

MIP in second sample

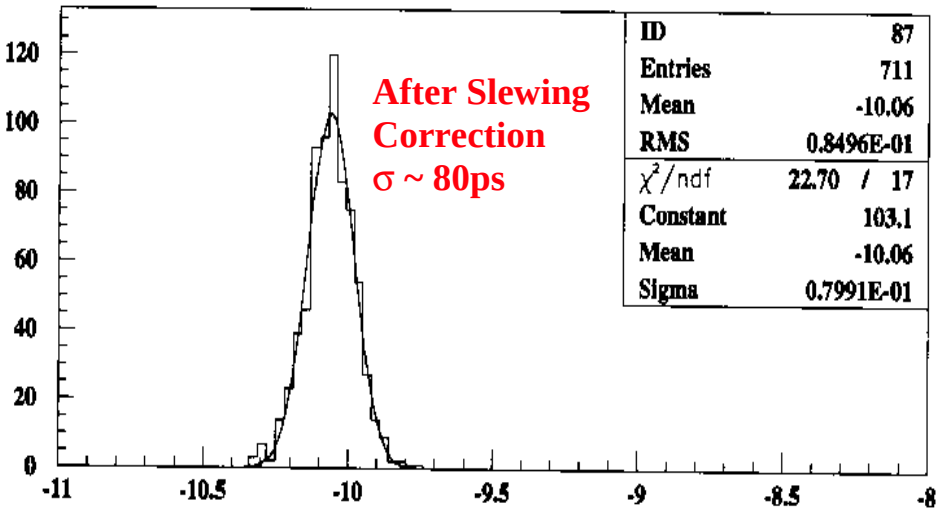
net charge = sample3 - sample1

MIP peak clearly separated from pedestal

TVC time resolution



TOF before Slewing Correction



TOF after Slewing Correction

TOF resolution 80ps achieved !

Bench test and test exp. at KEK

- TVC

  1, time resolution < 1ch ~ 25ps

  2, AMU cell dependence negligible

  3, linearity is good enough

  4, range > 90ns ===> more than we need

  5, no holes in the range

  6, TOF resolution from test beam ~ 80ps

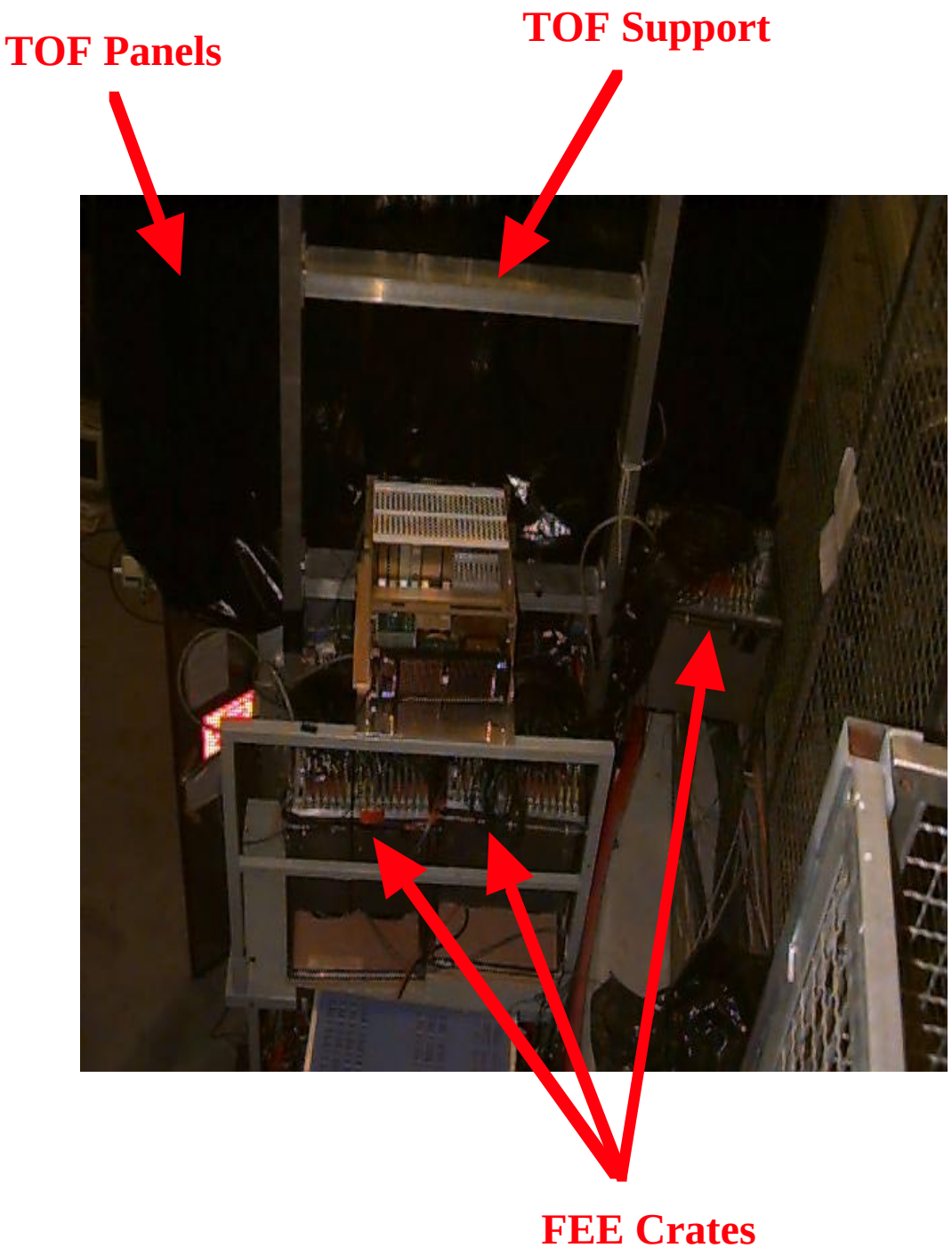
- QVC

  1, pedestal width ~ 1.5 ch

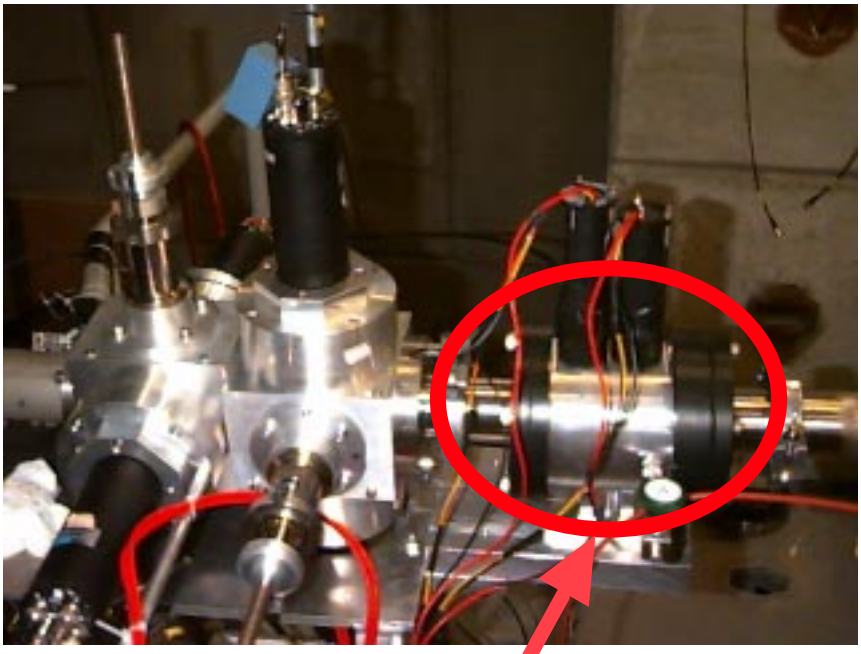
  ===> much better than we need

  2, MIP peak clearly separated from pedestal

WA98 FEE setup



WA98 Start Counter



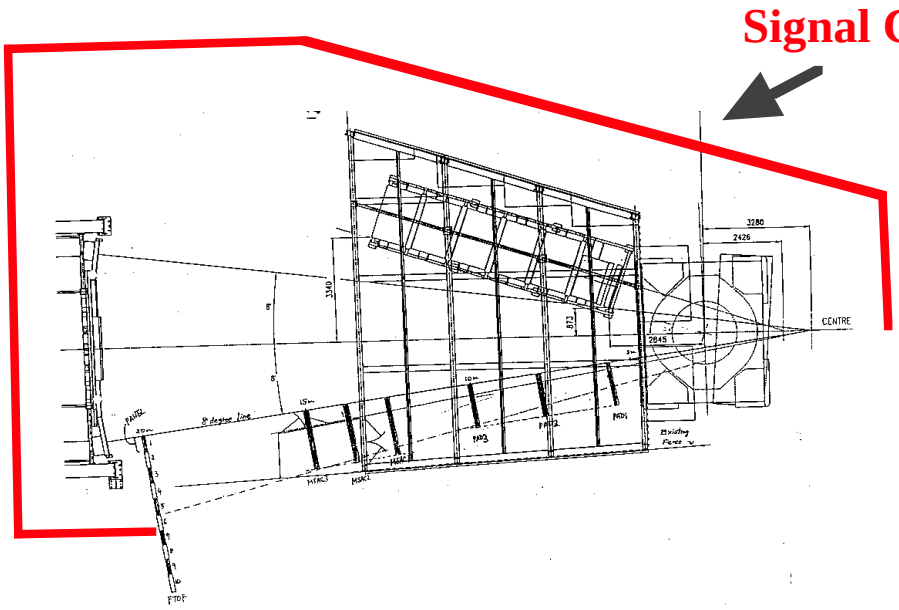
1, Nitrogen Gas Cherenkov Counter

2, Two PMT's are used

3, Too much light with 160GeV/c Pb beam --> we use filter !

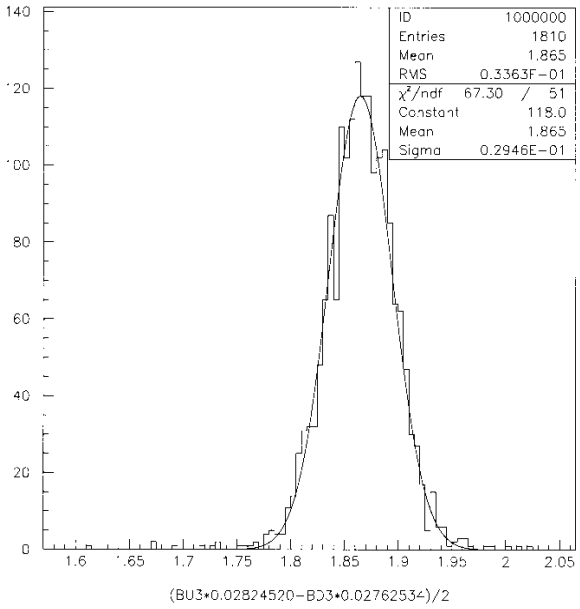
4, Time resolution obtained by CAMAC TDC ~ 30ps

Time Resolution of WA98 Start Counter



Time Resolution

σ < 30 ps



Difference Between Two PMT's

Revision History

- **Man Power**

  C.Y. Chi, K. Kurita, K. Enosawa (Physicists)

  W. Sippach, H. Cunitz, L. Zhang (Elec. Engineers)

  N. Bishop, P. Maytan, J. Capone (Technicians)

Jan. '95 **Started Design of TOF FEE**

Nov. '95 **WA98 Pb run - without FEM**

Postponed KEK test a few times

Feb. '96 **KEK Test Beam - 1 FEM Prototype**

Sucessful test beam

Revision of the board (Booting via ARCNET, regulators)

May '96 **WA98 pA run - 7 FEM's (Ver. 2)**

Another revision (added a regulator, lowered discri. subboard)

Assembler started assembling in early Sep.

Oct. '96 **WA98 Pb run - 60 FEM's (Ver. 3)**

Mass Production Experience

Key Issues

1) Get all parts as soon as the design is finished

Some parts have 6 months delivery time and some even disappear

2) Make money available in time

3) Add at least one more month to the delivery time they claim ==> continuous push is necessary

4) Chip yield was ~ 90%

5) Ended up with $200/ch

PHENIX TOF FEE Spec Sheet

Board size	29.27 cm x 28.73 cm
Board spacing in crate	2.54 cm
# of board in crate	(8 + 1 controller card) x 2
Cooling Air flow	back to front
# of ch	2048
PMT type	Hamamatsu R3478
Pulse Width	~10ns
Pulse Height	500mV - 2V
Total Charge	50-200 pC
Au-Au occupancy	<10%
Timing resolution	<25ps
Charge resolution	several % of MIP
Time range	>70ns
Cross Talk	<25ps
Threshold range	20mV - 100mV
connector	LEMO
System clock input	50% duty cycle bunch crossing clock Sealectro Connector
L1 input	NIM with clock cycle width, LEMO
Q reset	NIM pulse >10ns, ~10 times of the signal frequency, LEMO input
FEE reset	NIM pulse ~100ns, LEMO input
Qinj	NIM pulse >200, LEMO input
Test Pulse	ECL input <5ns, Sealectro connector
Clock/TP fan out	External ECL fan out (18 output)

Conclusion

- **Status**

  1, we understand the system

  2, The system performance is all satisfactory

  3, WA98 start counter resolution < 30ps obtained with the FEE after a long cable ==> no surprise was found

  4, TOF resolution ~ 80ps is achievable

  5, FEE revision and mass production experience

  6, More detailed TOF study will come out from WA98

- **Future**

  1, TOF FEE final design review

  2, L1 output parts to be mounted

  3, Rest of the boards will be fabricated by the end of 1997

  4, TOF FEE documentations