EICAC Meeting

DAQ/Electronic Systems at High Luminosity w/CW Beams

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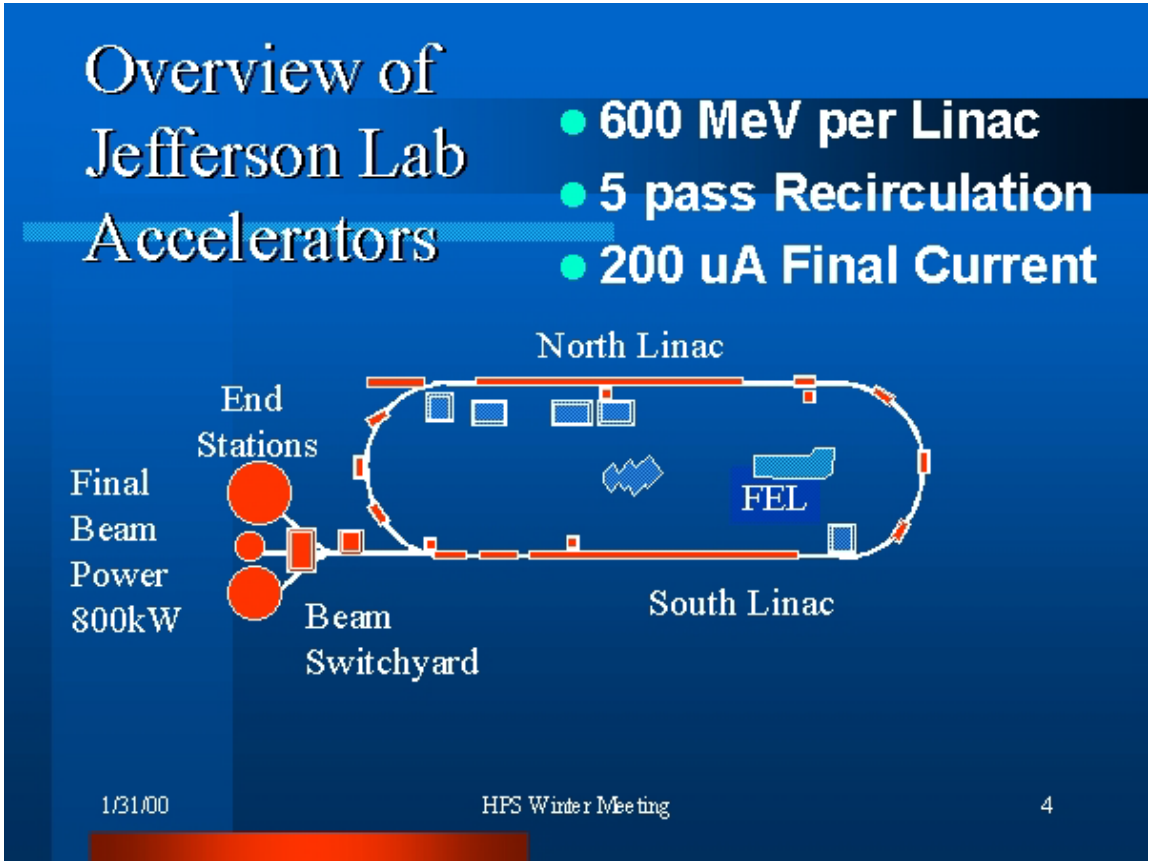
Experimental Nuclear Physics Division

- Experiment experience using CEBAF beam
- **C**ebaf's **L**arge **A**cceptance **S**pectrometer
  CLAS DAQ/Trigger design parameters
  Performance Notes -- 1996 to 2008
- 12 GeV Upgrade –
  Trigger Requirements & Solutions
- EIC Trigger requirements – New challenges
- Summary

Background

CEBAF

- Two recirculating Linacs operating at 1497MHz
- Three beams produced at the injector with 120 degrees of phase separation
- Beams delivered to three experimental halls at 499MHz
- Continuous Wave (CW) bunches at ~2ns on fixed targets



An old story,

- Long ago, a young theoretical physicist couldn't find a girlfriend for a long time …
- He then complained about it to Hans Bethe
- Hans's advice:

"Young man, if the cross section is so low, increase the luminosity !"

$$\text{Rate} = \sigma \mathcal{L}$$

σ - cross-section

probability that an interaction will occur.

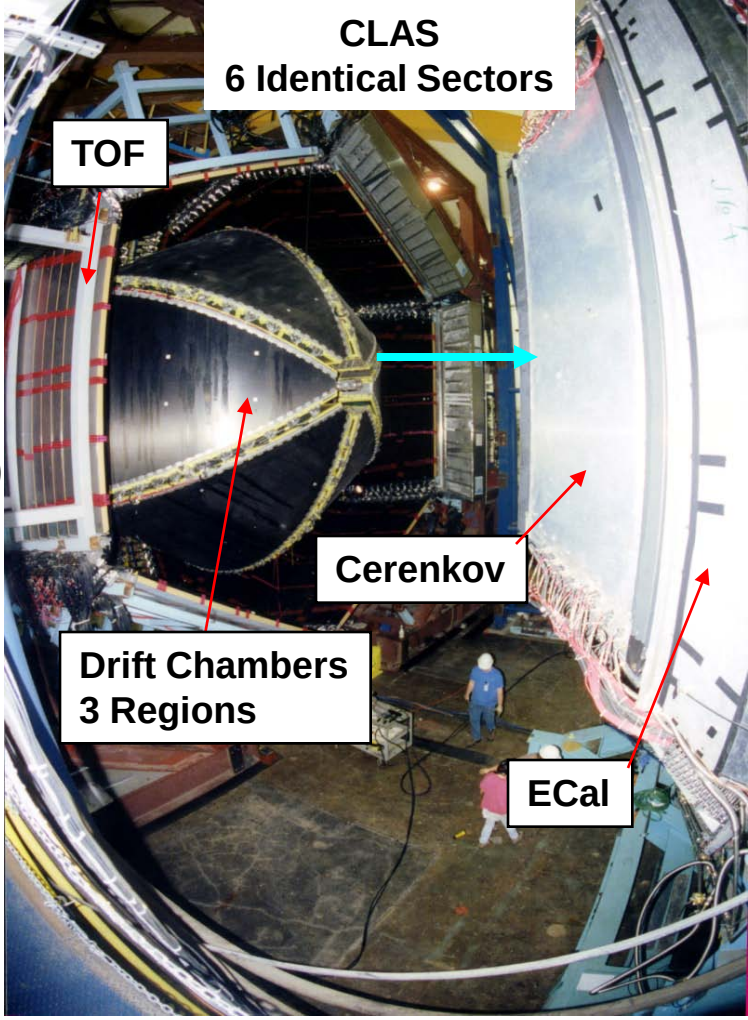
For Jefferson Lab experiments:

- 'Collision' Rate 499MHz
- Event Rate in the MHz
- e- Trigger Rates >10KHz

"Every collision does not produce an event, and every event does not produce a trigger"

CLAS DAQ/Trigger Design Parameters

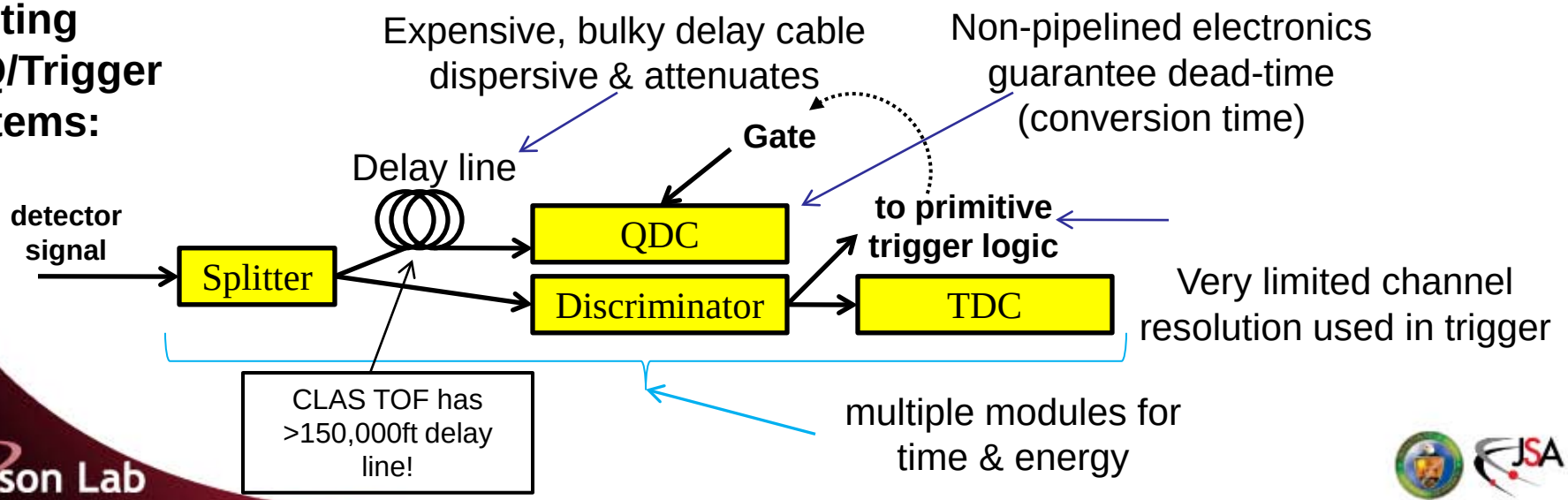
- Photon & Electron Experiments with polarized targets, polarized beam
- High Luminosities $10^{34}cm^{-2}s^{-1}$:
- DAQ event rate designed to >10KHz
- Custom Level 1 Hardware
  - Pipeline design, Dead-timeless, (15ns pipeline clock)
  - Low latency, ECLps technology
  - Event Processor combines sector coincidences
- Fast Level 1 for ADC Gate, TDC Start
  - TOF, Cerenkov, Electromagnetic Calorimeter
  - Pattern recognition programming
  - Sector based logic for L1 trigger 'equations'
- Level 2 (Drift Chambers)
  - Majority Logic Pass/Fail per sector
- Trigger Supervisor manages trigger signals and interrupts the front end crate **R**ead**O**ut **C**ontrollers (ROC)
- Up to 32 Front End ROCs
  - Fastbus, VME, [TDC; ADC; Scalers]



CLAS Trigger Performance Notes (1996 → Present)

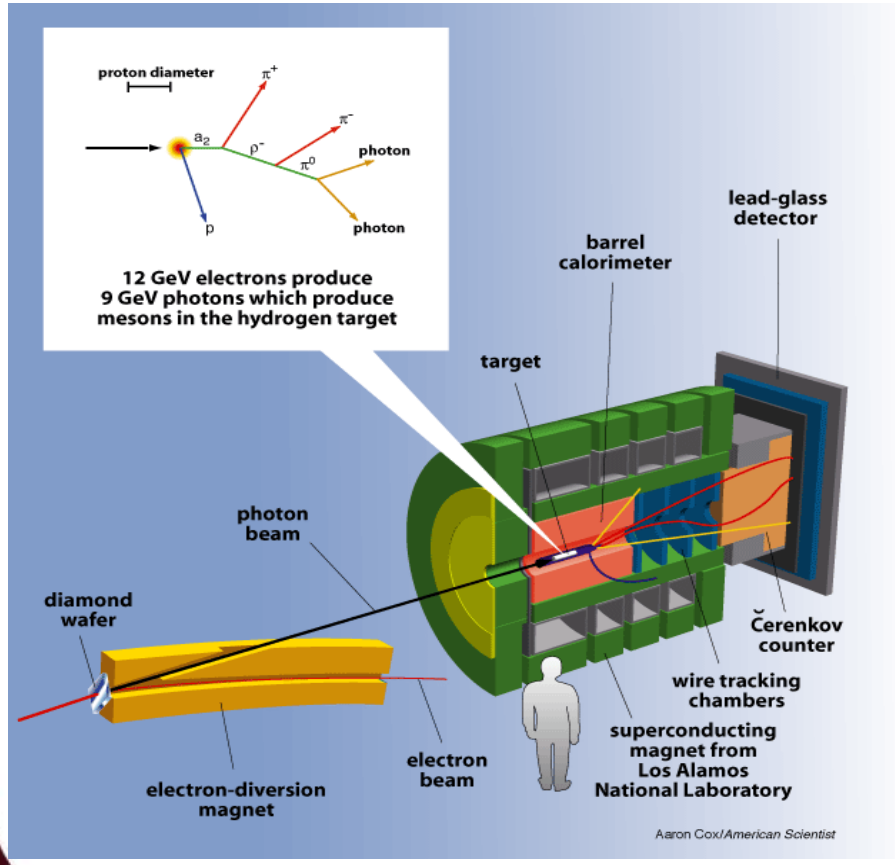
- Relatively low failure rate of FastBus instrumentation
- Nine (9) aging BiRa FastBus crate power supplies have been replaced with Wiener product for 1877 TDC crates only
- Virtually no hardware failures for custom Level 1 Trigger System
  *VXI crate and power supply converted to Wiener product
- Virtually no hardware failures for custom Level 2 Trigger modules
  - 360 Level 2 boards
  - Each board uses 6 Xilinx FPGA (1990 Technology ☺)
- Very recent implementation of VME CAEN 1495 programmable (FPGA) logic modules for the g12 photon beam experiment. Photon trigger hardware is coupled to original Level 1 modules to create triggers for CLAS. In use since April 2008, with excellent results and new trigger GUI.

Existing DAQ/Trigger Systems:

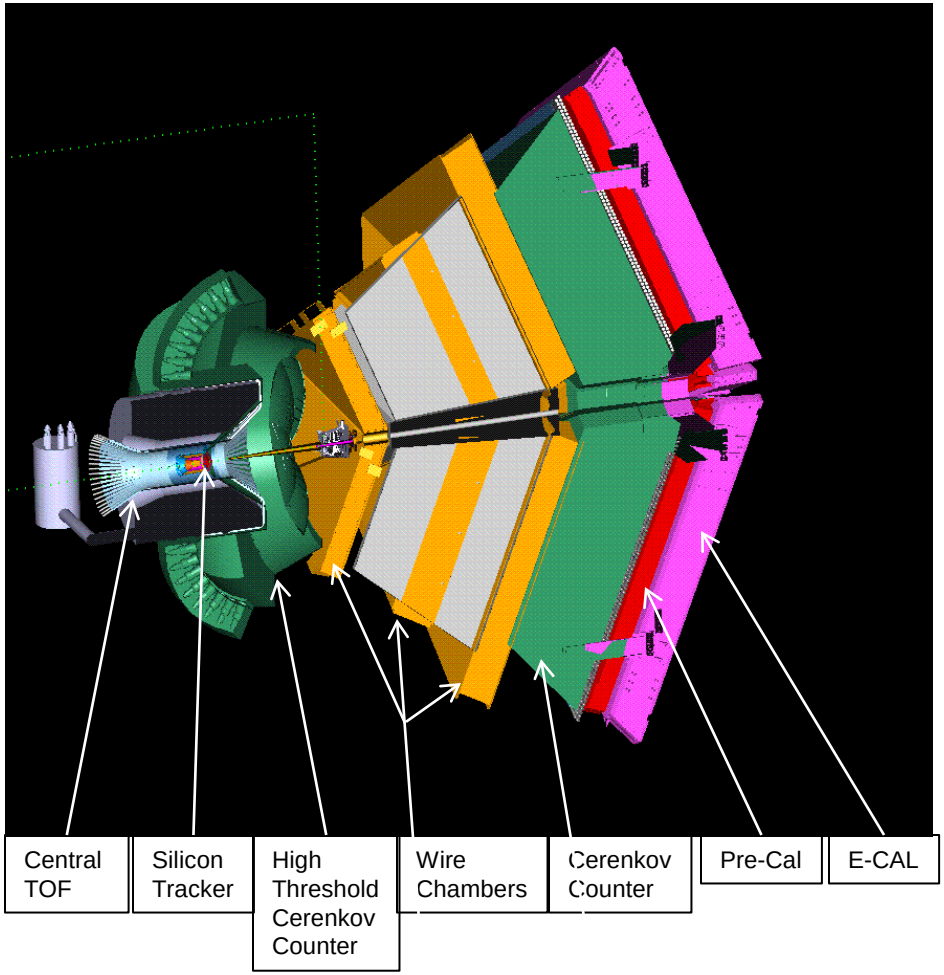


Two examples of 12 GeV Experiments

GlueX



CLAS12



12 GeV Trigger Requirements

- 200kHz average L1 Trigger Rate, Dead-timeless, Pipelined, 2ns bunch crossing (CW Beam)
- L1 trigger supporting streaming subsystem hit patterns and energy summing with low threshold suppression
- Scalable trigger distribution scheme (GlueX: ~30 L1 crates, ~50 total readout crates)
- Low cost front-end & trigger electronics solution
- ***Reconfigurable firmware*** – CLAS12 (Hall B) will use different programmable features than Hall D

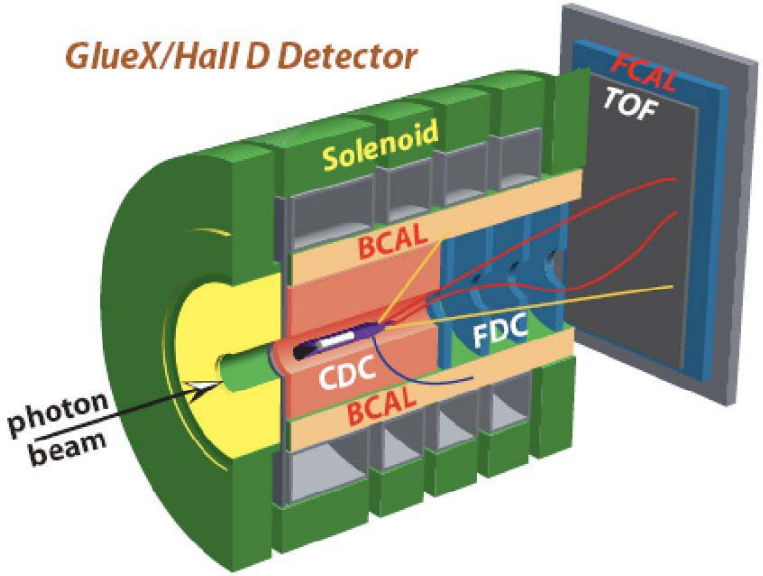
12 GeV Trigger Requirements

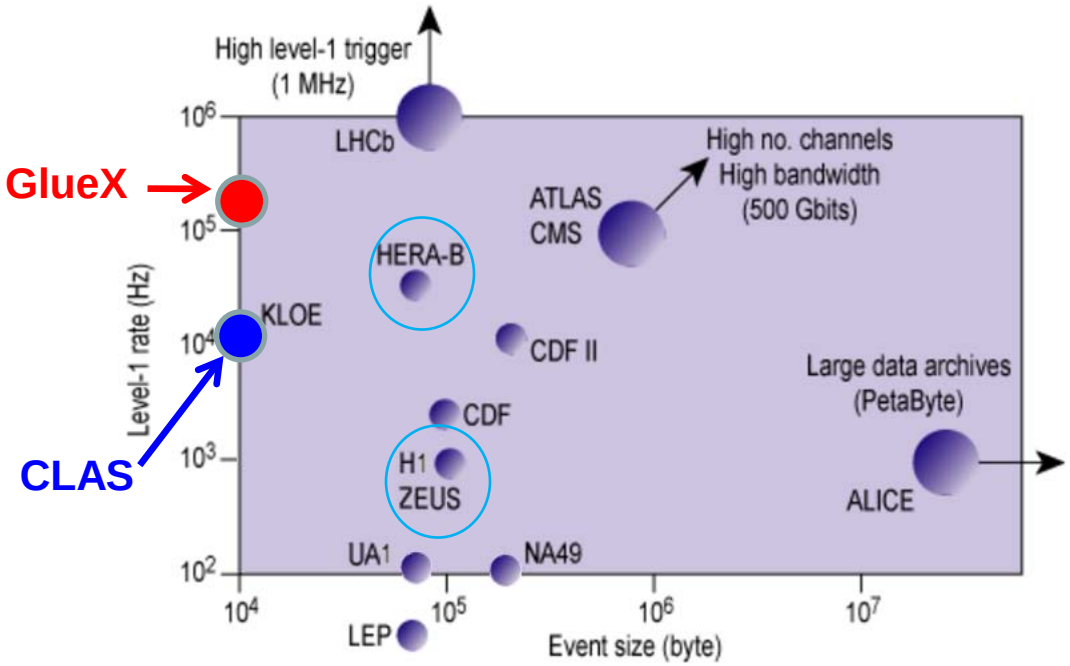
Specific to Hall D

- Reduce total hadronic rate from 350KHz to true tagged hadronic rate of ~14KHz
- Use Level1 hardware trigger and Level 3 farm to achieve this 25:1 reduction
- Level 1 hardware trigger efficiently cuts low energy photon interactions
- Level 1 trigger hardware design goal is 200KHz
- Level 1 includes:
    - Energy Sum from Barrel Calorimeter
    - Energy Sum from Forward Calorimeter
    - Charged track counts (Hits) from TOF
    - Charged track counts (Hits) from Start Counter

- Simulations show that this Level1 cut method achieves ~150KHz trigger rate
- Relatively ‘open’ Level 1 trigger

Compare GlueX to CLAS in Hall B

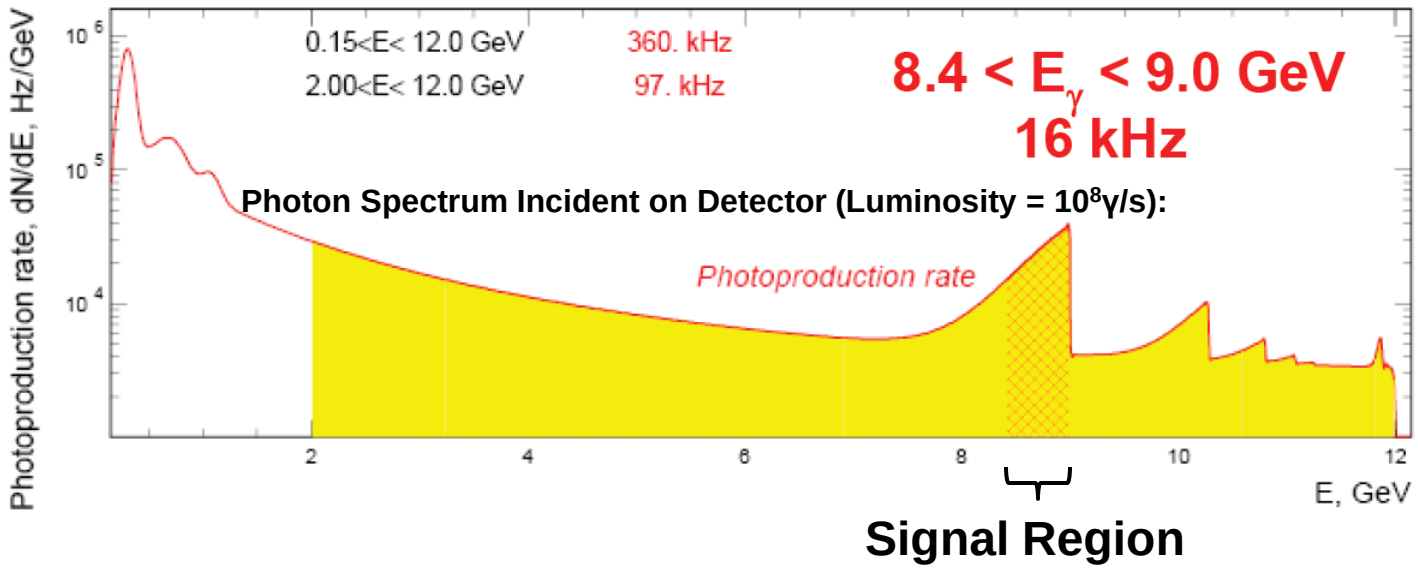




	Hall D-GlueX	Hall B-CLAS
Channel Count:	~20k	~40k
Event Size:	~15kB	~6kB
L1 Rate:	**200kHz**	**10kHz**
L1 Data:	**3GB/s**	**60MB/s**
To Disk:	**L3, 20kHz, 300MB/s**	**L2, 10kHz, 60MB/s**

* Expected Level 1 rates at a luminosity of a 'few' x 10^{34} are expected to be in the 100 kHz range for EIC

Example L1 Trigger (GlueX)

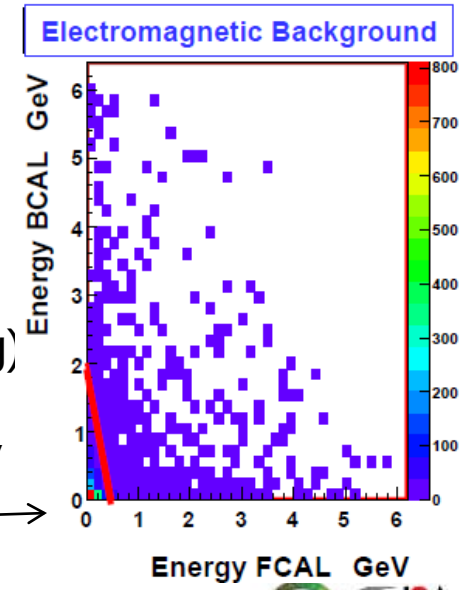


L1 Trigger Requirements:

- Reduce 360kHz hadronic & 200MHz electromagnetic interaction to <200kHz L1 trigger rate
- High acceptance in signal region (8.4-9.0GeV)

L1 Trigger:

- Process Trigger Data in 100ns time windows (4ns stepping)
- Start Counter Hits > 0
- L1 Energy sum suppresses BCAL & FCAL pulses <30MeV
- $BCAL_{energy} + 4 * FCAL_{energy} > 2GeV$

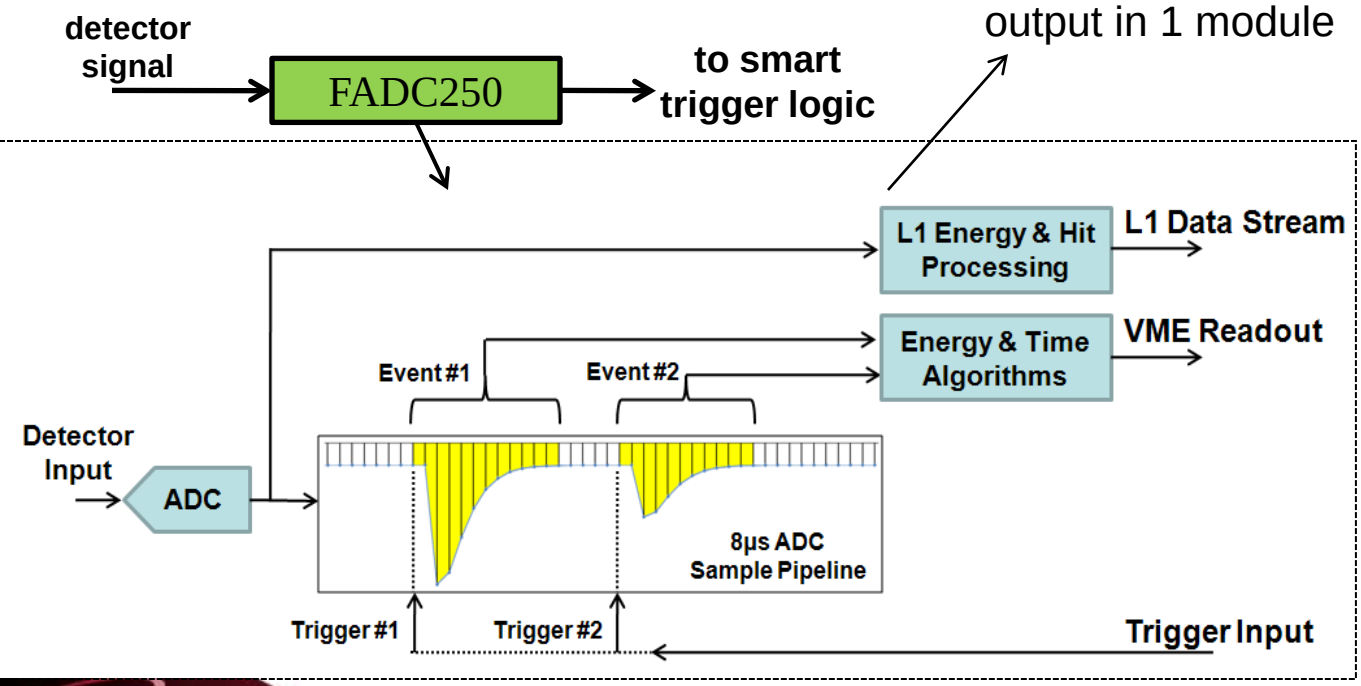


12 GeV Trigger Hardware

Hall D – "How do you perform this Level1 cut with hardware?

- Use FLASH ADC for detector signals that are included in the Level 1 trigger
- Detector signals are stored in front end boards
- Energy Sum is computed at the board, crate, and subsystem (BCAL,FCAL)
- Synchronous system and Trigger Supervisor performs event blocking at the ROC level
- 8us buffer on front end boards allows for trigger decision (latency)
- Use high speed fiber optic/serial data transfer from front end crates to global processors
- Easily supports 64 readout crates and is easily expandable

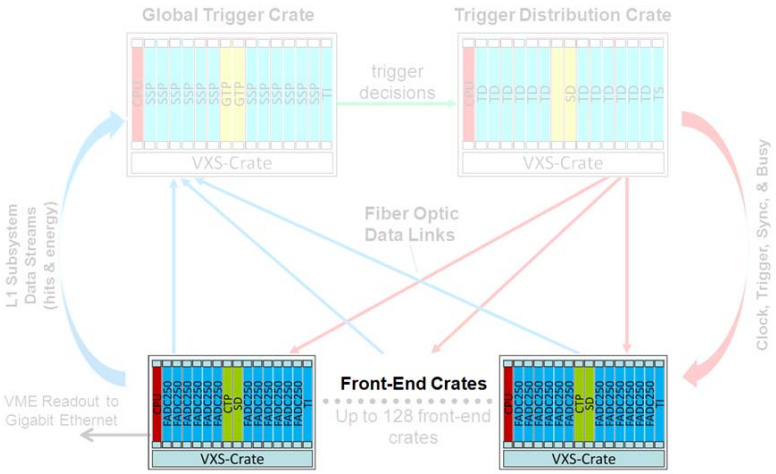
New System: (for timing >500ps)



- **Pipelined sampling, readout, & trigger -> no dead-time**
- **Digitization retains original signal integrity**
- **Long pipeline allow more time for complex triggers**

Front-End Electronics
Flash ADC 250Msps

- 16 Channel 12bit, 250Msps Flash ADC
- 8µs raw sample pipeline, >300kHz sustained trigger rate (bursts @ ~15MHz)
- Post-processing in customizable firmware to extract time, charge, and other parameters minimizing event size
- Module supports 2eSST VME transfers at 200MB/s transfer rate
- Large event block sizes (>100) to minimize CPU interrupt handling
- ***<u>USE VITA_41 (VXS)</u>*** P0/J0 outputs 5Gbps L1 data stream (hit patterns & board sum)
- Used in existing 6GeV program:
  - Hall A BigBite
  - Upgraded Hall A Moller Polarimeter



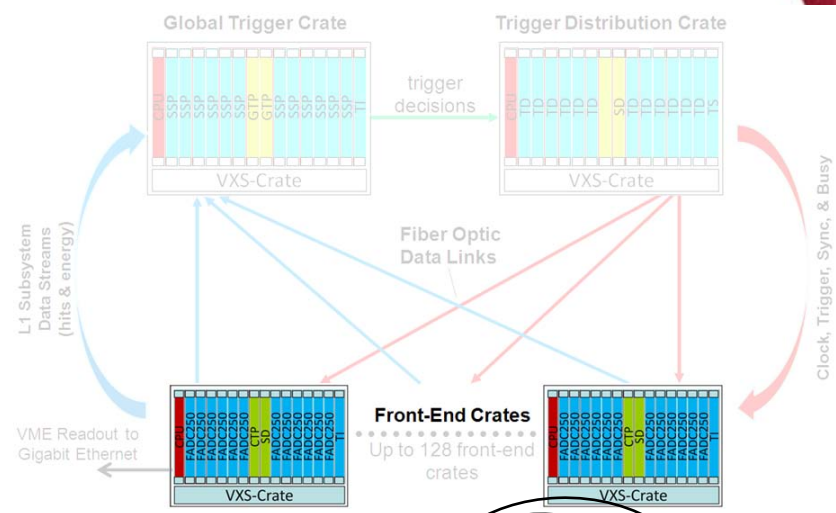
JLab-FADC250:

Front-end Crates: Level 1 Trigger

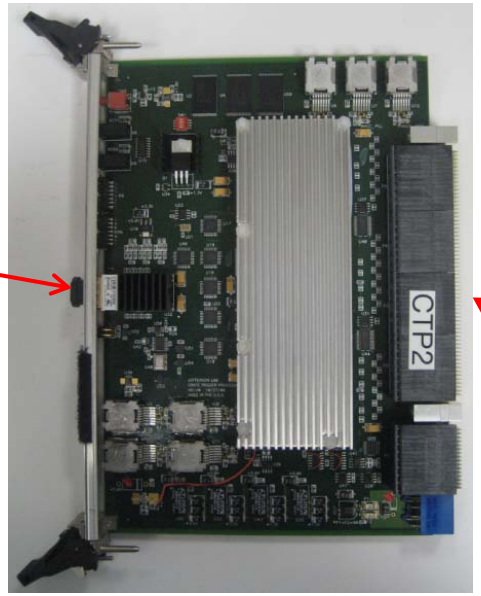
- Each FADC250 stream L1 board energy sum/hit to **C**rate **T**rigger **P**rocessor (CTP) residing in VXS switch slot A

- Crate Trigger Processor computes a crate-level energy sum (or hit pattern)

- Computed crate-level value sent via 10Gbps fiber optics to Global Trigger Crate (32bits every 4ns)



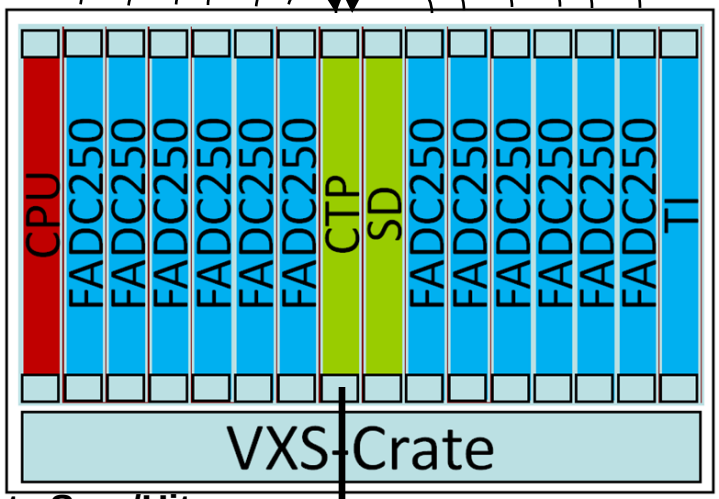
CTP Prototype:



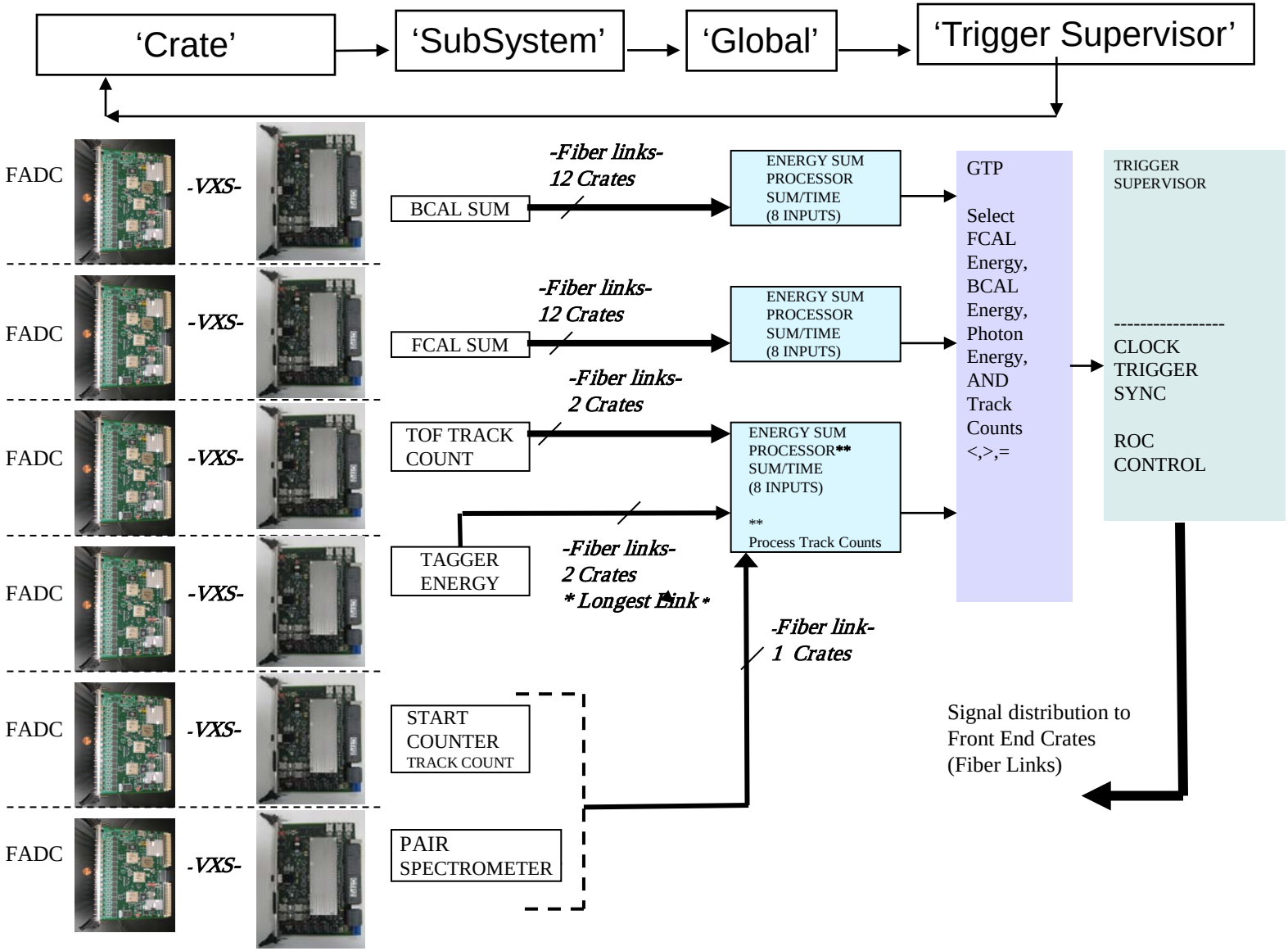
Fiber Optics Transceiver

VXS Switch Connector

Board Energy/Hits 5Gbps to CTP



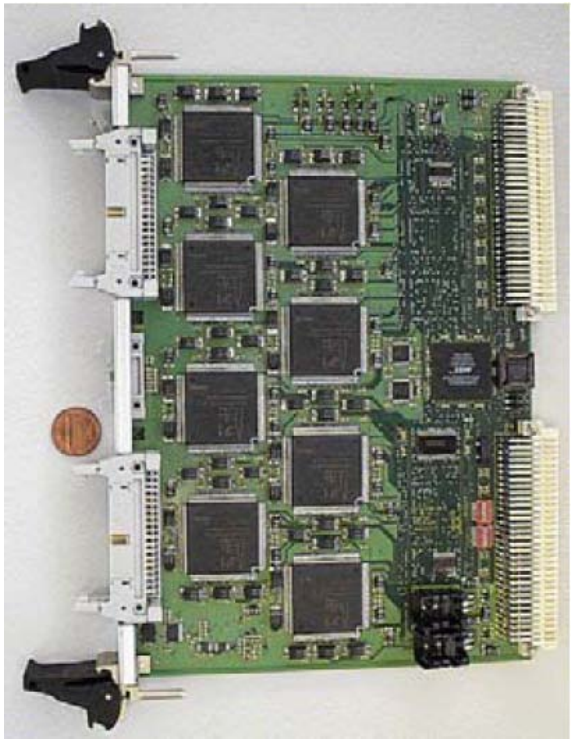
Crate Sum/Hits 10Gbps Fiber to Global Trigger Crate



Block Diagram: Hall D Level 1 Trigger

Front-End Electronics: F1TDC

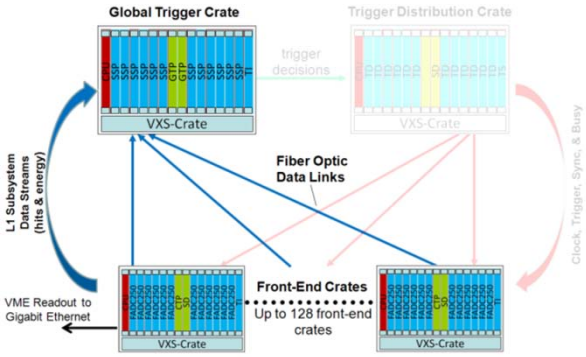
JLab-F1TDC



Sets maximum trigger latency

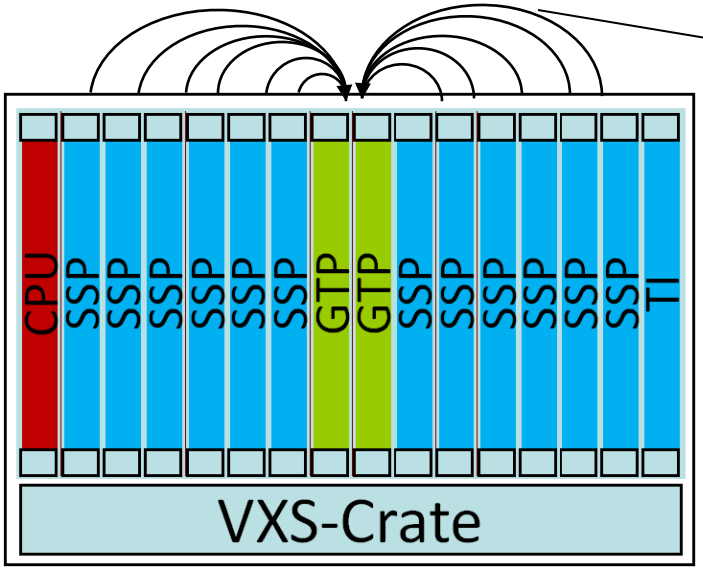
- **High resolution - 60ps/32 channel**
- **Normal resolution – 120ps/64 channel**
- **3.7μs sample pipeline**
- **Used in all subsystems except CDC & FCAL**
- **<u>Not used in L1 trigger</u>**
- **Uses VXS for clock, synchronization, and trigger input signaling**
- **CLAS12 has selected CAEN High resolution TDC module**

Subsystem Processor: L1



Global Trigger Crate:

Subsystem Energy Sum & Hit Pattern (10Gbps to GTP)

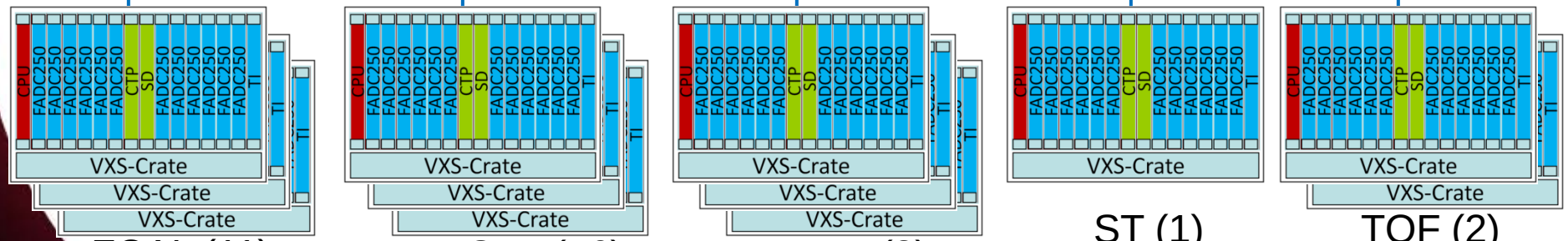


- Sub-System-Processor (SSP) consolidates multiple crate subsystems & report final subsystem quantity to Global-Trigger-Processor (GTP)
- 32bit quantity every 4ns

Hit Pattern

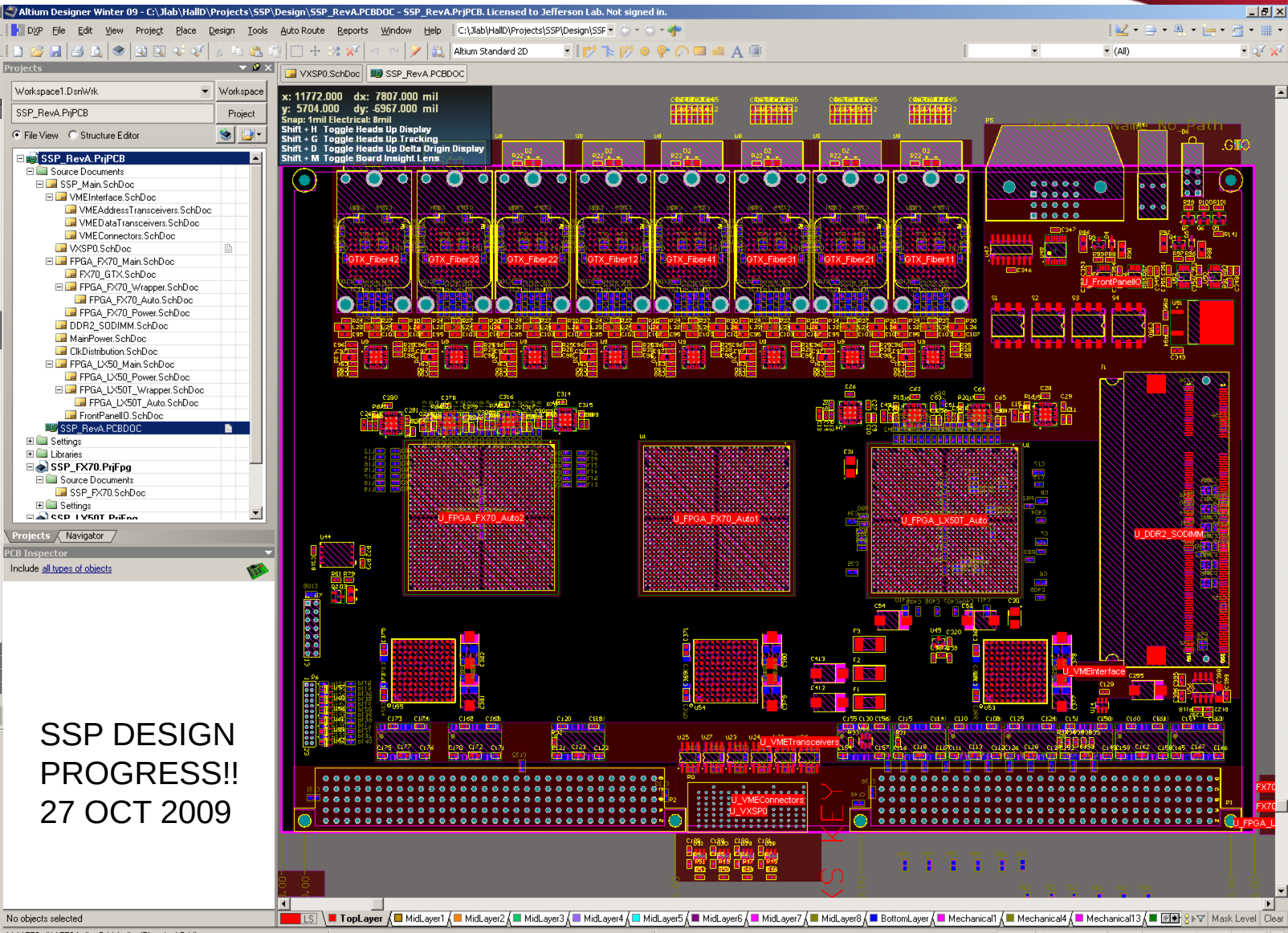
10Gbps fiber optics

Energy



FCAL (11) BCAL (16) Tagger (3) ST (1) TOF (2)

L1 Subsystems (# Crates)

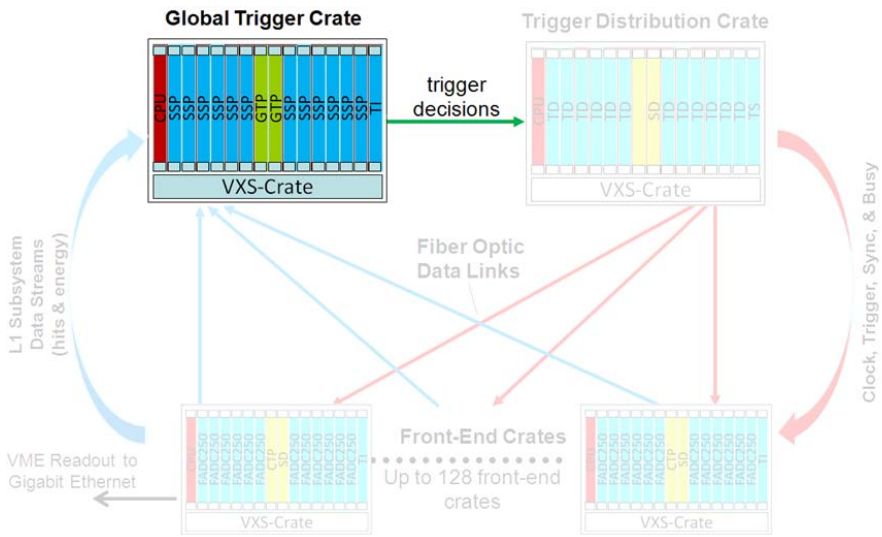


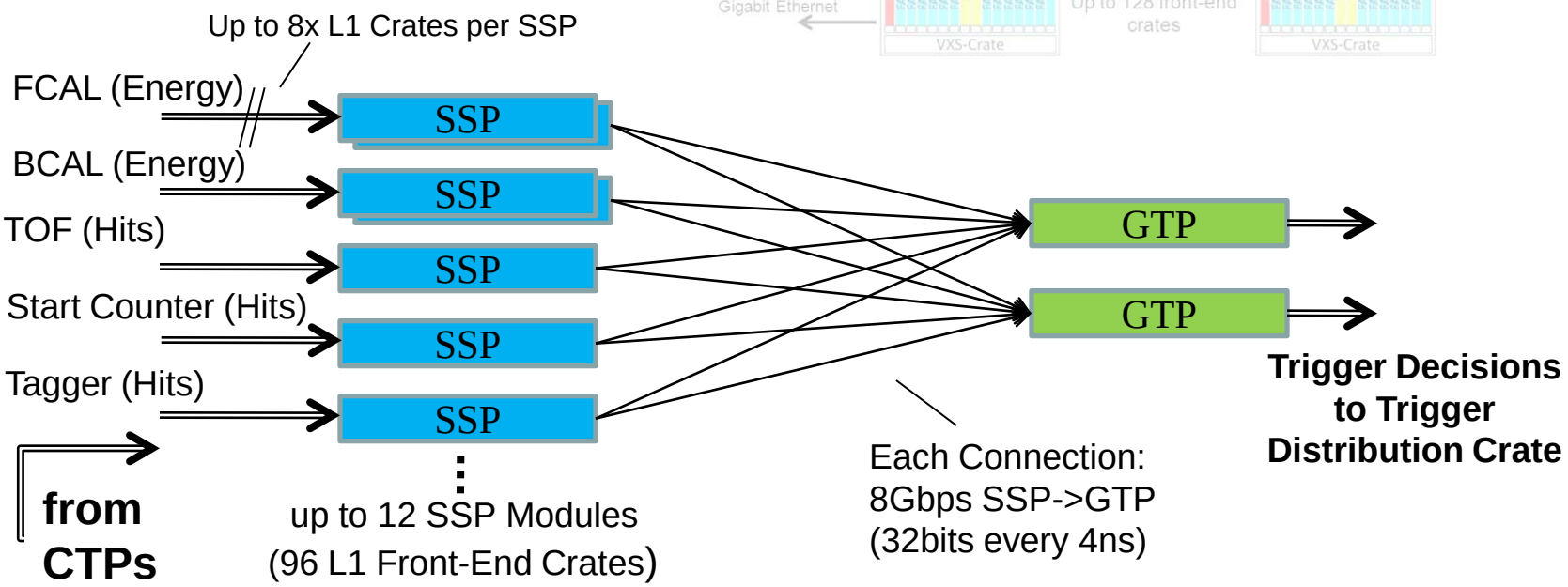
SSP DESIGN PROGRESS!!
27 OCT 2009

Global Trigger Processor: L1

- Global Trigger Processor (GTP) receives all subsystem L1 data streams

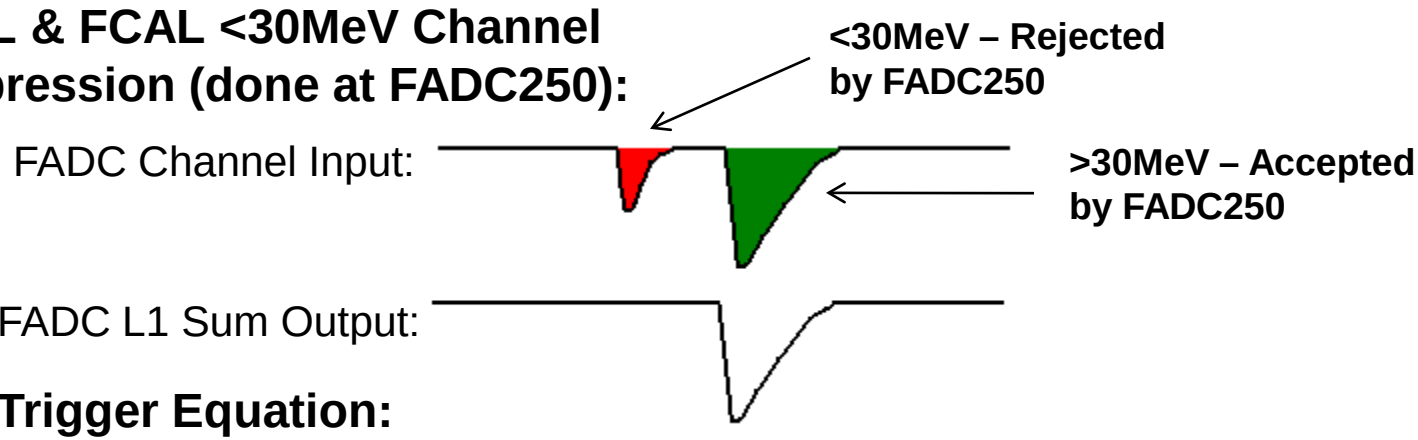
- Trigger decisions made in GTP and distributed to all crates at the Trigger Distribution Crate





Example L1 Trigger cont…

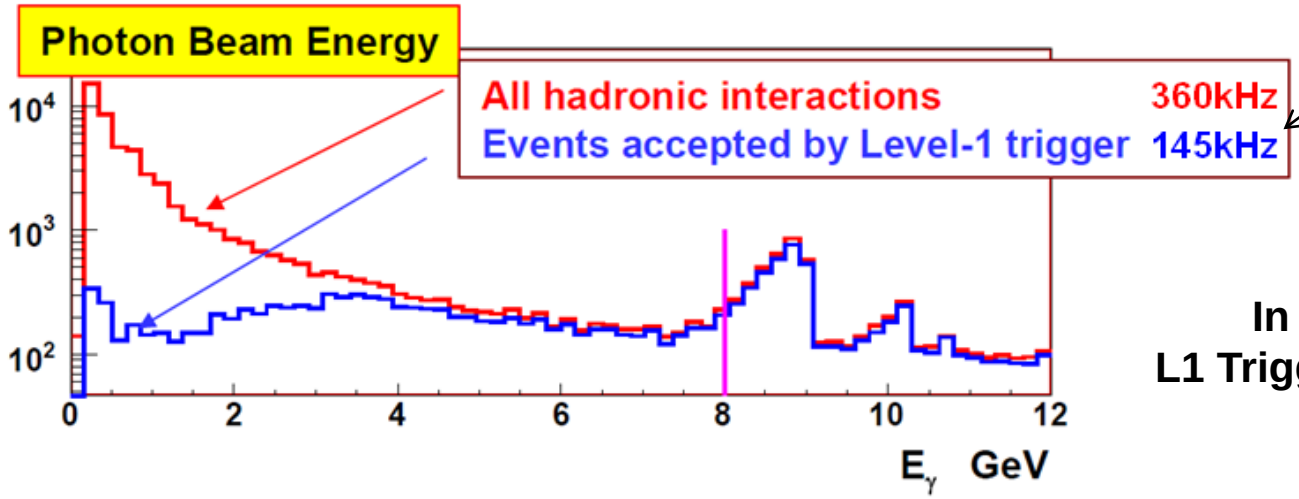
BCAL & FCAL <30MeV Channel Suppression (done at FADC250):



GTP Trigger Equation:

$$\sum_{t}^{t+100ns} ST_{hits} > 0 \;\; \&\& \;\; \sum_{t}^{t+100ns} BCAL_{energy} + 4 * FCAL_{energy} > 2GeV$$

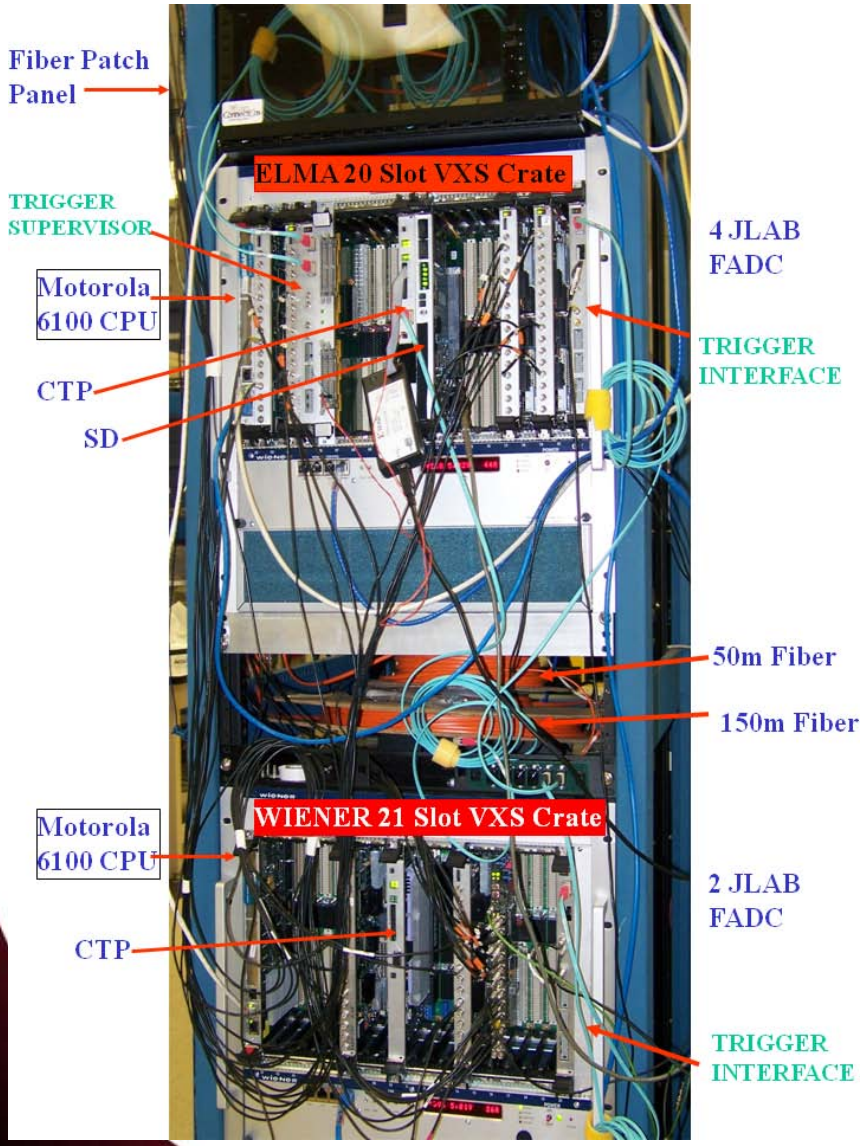
Resulting L1 Acceptance Spectrum:

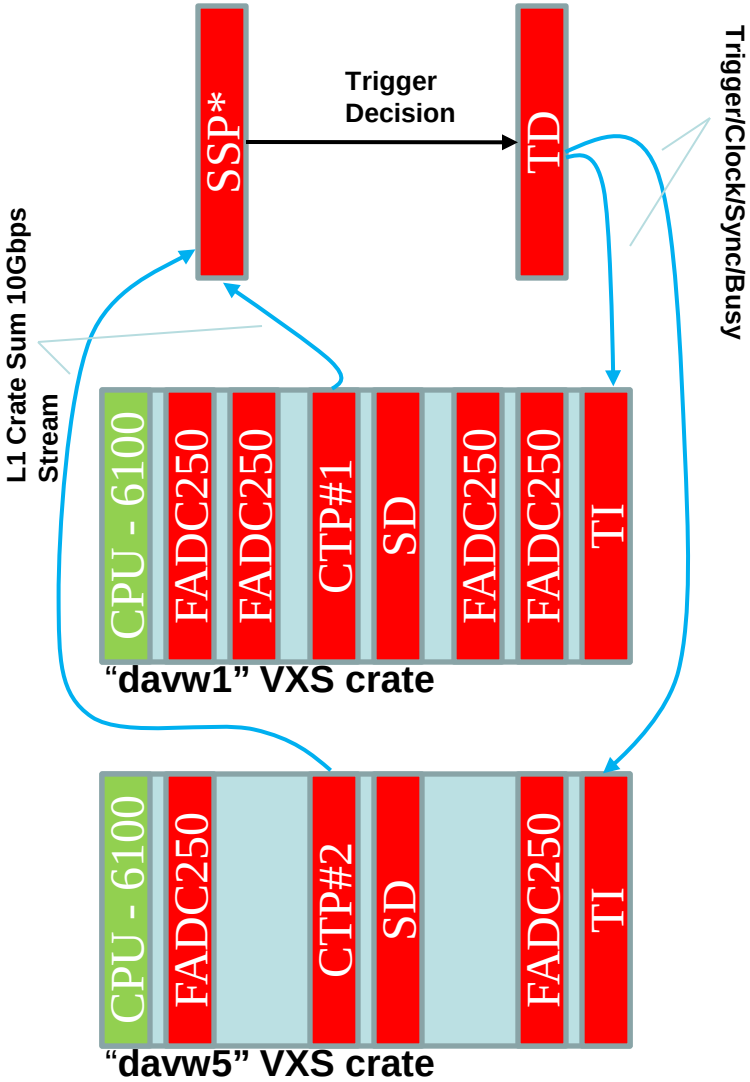


L1 Rate < 200kHz

In Signal Region:
L1 Trigger Efficiency > 92%

2 Fully Prototyped Front-End Crates

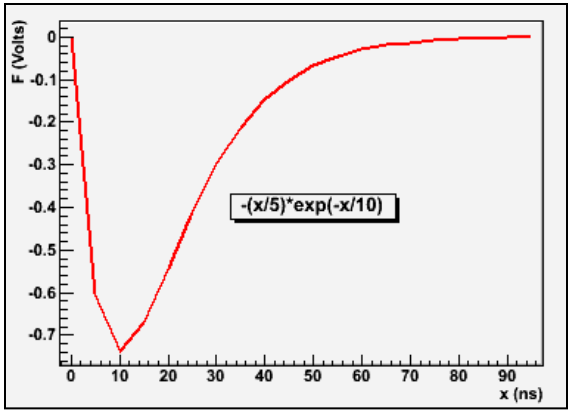




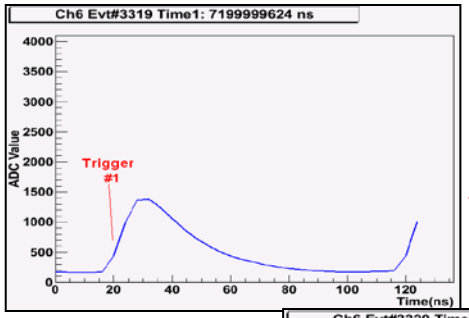
*SSP function embedded inside 2nd CTP

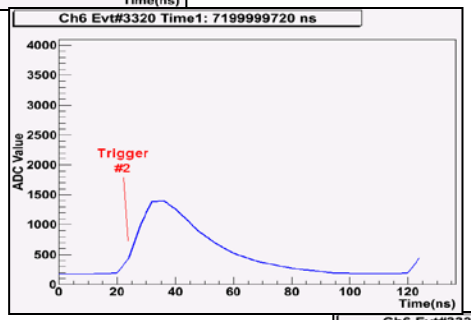
2 Crate Energy Sum Testing

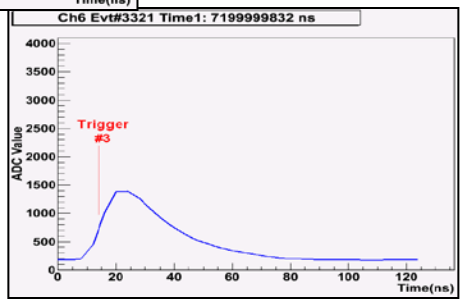
Input Signal(to 16 FADC250 Channels):



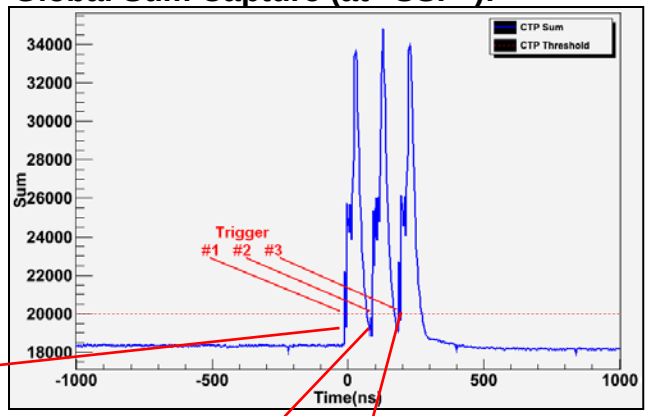
Raw Mode Triggered Data (single channel shown only):







Global Sum Capture (at "SSP"):



- **Threshold applied to global sum (80 digitized channels) produces 3 triggers.**
- **Raw channel samples extracted from pipeline shown for 1 channel.**
- **Runs at 250kHz in charge mode**
- **Latency: 2.3μs(measured) + 660ns(GTP estimate) < 3μs**

EIC Trigger Hardware Goals

(Copied Slides)

Detector R&D topics

- DAQ / Trigger System (I)
  - Goal:

    Multi-level trigger system including development of trigger algorithms for efficient rare process and DIS-e trigger selection (In particular for very low electron energies)

  - Issue:

    To efficiently select rare processes next to minimum-bias trigger may require the use of tracking at the trigger level.

Detector R&D topics

- DAQ / Trigger System (II - ELIC only)
  - Goal:

    Development of high-speed DAQ/Trigger system for very small bunch crossing time.

  - Issue:

    Need to i) prove that one can pipeline data to handle 0.5 GHz RF frequency; ii) Prove >2,000 rejection of hadronic background capability at trigger level; iii) develop GHz level ultra-fast digitization capabilities and verify timing; iv) Develop multi-processing data acquisition to achieve 5 kHz, 150 MB/s (CLAS achieved 8 kHz, 30 MB/s); v) Simulate data rates in detectors and electronics; vi) Study how to further improve to 1.5 GHz RF frequency.

Summary

- Experience with CEBAF at 2ns beam structure and electron trigger techniques has been very reliable and at relatively high trigger and data readout rates.
- The 12 GeV upgrade's new experiment (GlueX) requires significant performance improvements for both trigger and data acquisition.
  - Prototype hardware has been built and test results exceed trigger rate requirements. **L1 requirements (200 kHz, < 4 μs) latency can be met**
  - Flexible system design (use same module designs for two new complex experimental Halls)
- Studies have shown that high bunch crossing frequencies (0.5-1.5 GHz) are not a challenge for an EIC trigger
- Advanced features like vertex finding, geometrical matching, and pulse shape analysis can suppress vacuum-related background
- Prototyping and testing have been successful without pushing the bandwidth limits of FPGA technology and high speed(Gbps) serial transport techniques.
- There is room for expansion and continued development for building intelligent triggers for future experiment requirements!

Backup Stuff

Bunch Spacing from Detector Point of View

CLAS operates at a 500 MHz bunch frequency. The e^- can be traced back to the specific bunch, which is then used as "RF time tag" to calibrate the detectors for the hadrons.

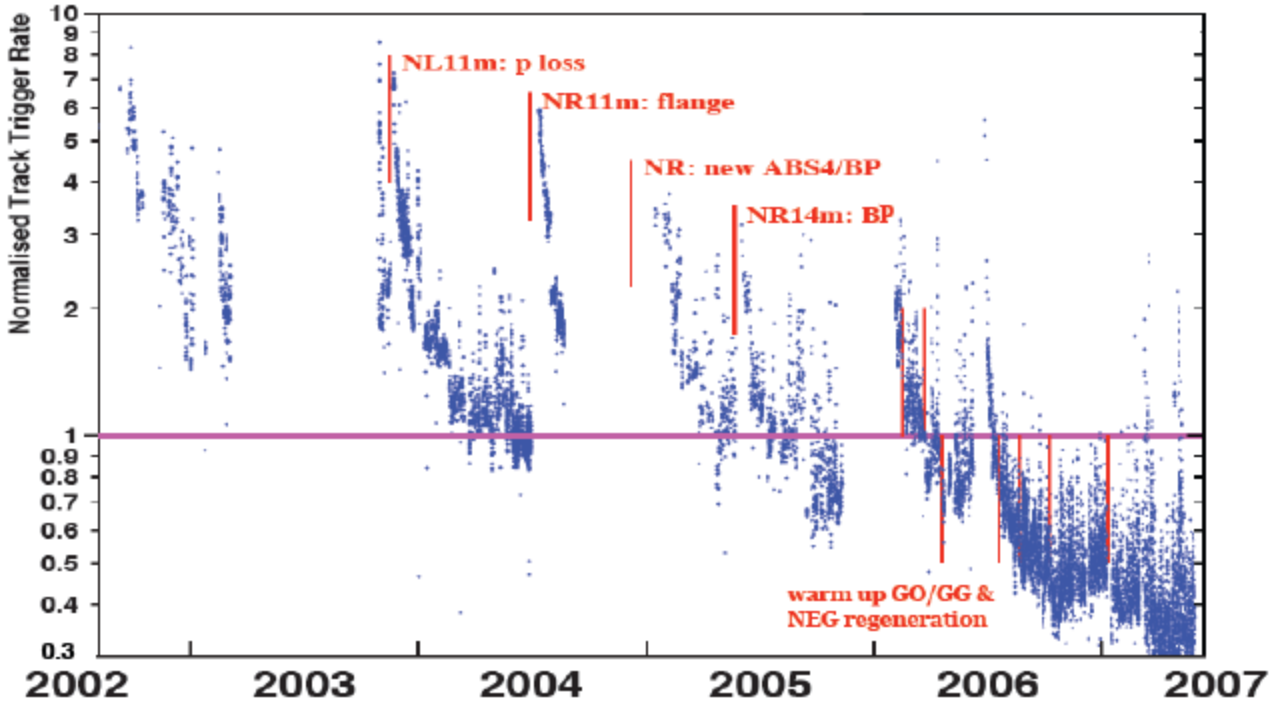
(1.5 GHz seems o.k. for this too, see next slides)

Question: What are the implications in collider mode?

1. For the specific e-ion process, you still have the (not high-rate) e^- tag
2. Collection times for (fast) detection devices is 10-20 ns
   (e.g., silicon, scintillator, and PMT's, but not for e.g. Ar calorimetry)
3. Use a pipelined ultrafast DAQ/electronics system - **not synchronized with RF bunch frequency – read out when electron trigger occurs.**
4. Digitization allows determination of time less than the resolving time of the specific detector (now, calibration becomes the main issue)
5. The multiplicity w.r.t. CLAS12 only increases by a factor of 2-4, and the luminosity is close to the same → total hadronic rates similar.
6. Hence, can one untangle the interactions separated in time by less than the resolving time of the detector in the face of pileup?
7. **Yes. If CLAS + CLAS12 can, so can an EIC. Issue is one of real coincident events versus randoms/backgrounds.**

Hadronic Background Estimate

HERA: Strong correlation between detector (trigger) rates and beam line vacuum. EIC trigger can be more selective.



Early HERA vacuum ~ 10^{-7} torr → 3 x 10^{9} atoms/cm^{3}
120 m straight section before IP → 4 x 10^{13} atoms/cm^{2}
100 mA proton current
→ luminosity = 2 x 10^{31} proton-atoms/s/cm^{2}
→ comparable to e-p luminosity

σ(pp) ~ 100 x σ(ep) → proton-residual gas interactions most severe background for HERA detector operation

Multiplicity for High-Energy Hadron Interactions

F. Braccella and L. Popova, J. Phys. G 21 (1995) 1379

Simple fit to data in article: total multiplicity ~ $2s^{1/4}$

$s^{1/2}$ (GeV)	n (article)	$2s^{1/4}$
20 (ISR/FNAL)	9	9
540 (SPS)	45	46
1800	82	86

CLAS	($L = 2 \times 10^{34}$)	n = 3.7	(close to empirical observation in CLAS)
CLAS12	($L = 1 \times 10^{35}$)	n = 4.2	
EIC	E_{cm} = 12 (MEIC-Low E)	7	Factor of 2-4
	51 (MEIC-Hi E)	14	
	100 (ELIC)	20	
HERA	319	35	

JLab is "Proof of Principle" that high RF is o.k.

"Easy" to select events of interest at a **fixed-target facility with 500 MHz beam structure.**

1.5 GHz, or 2/3 ns may be too short to "pick the electron bucket", but that simply means three random peaks are under the coincidence one. **RF frequency in principle does not matter**. It's the real to random ratio that matters, and the fact whether one can "see" bumps and valleys.

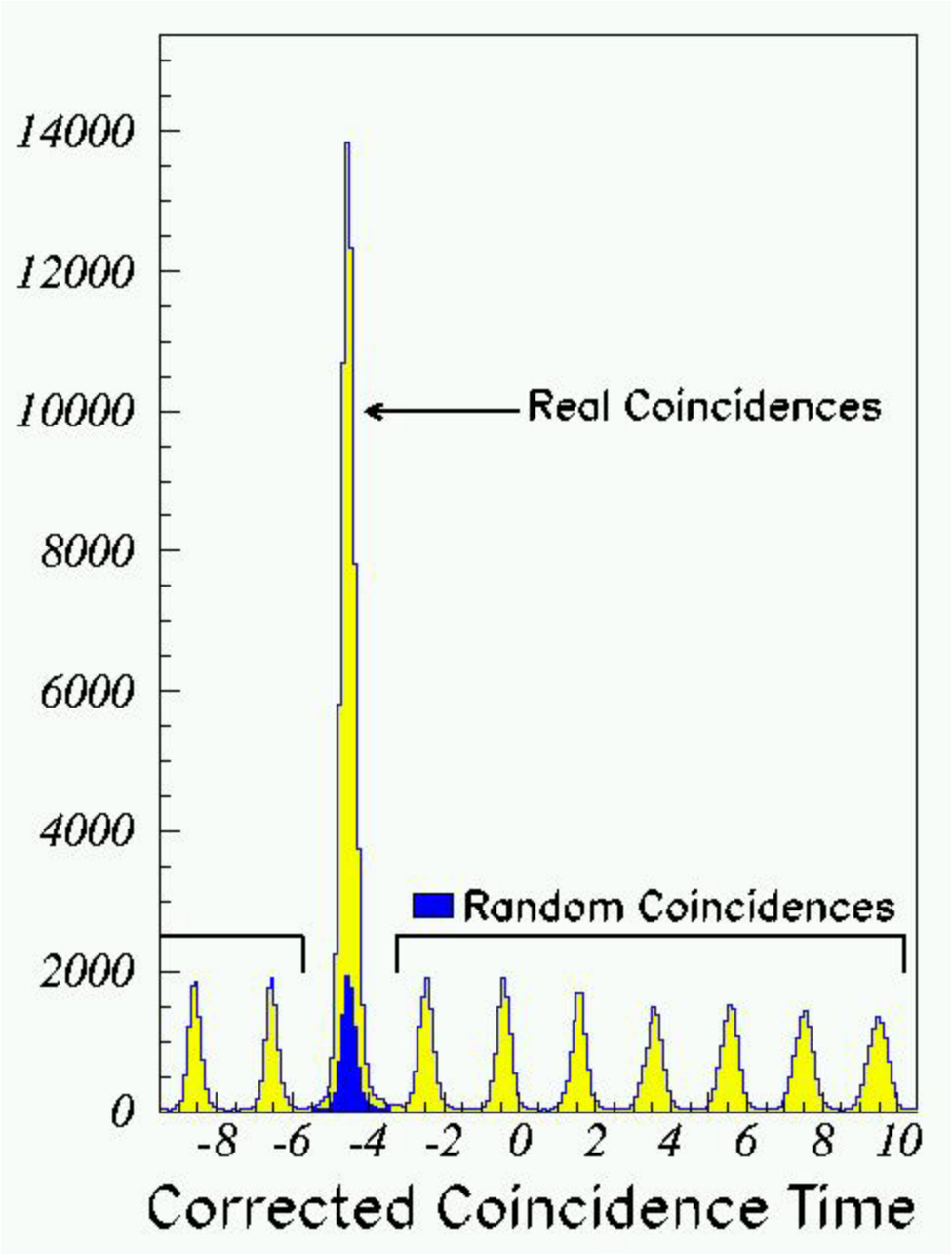


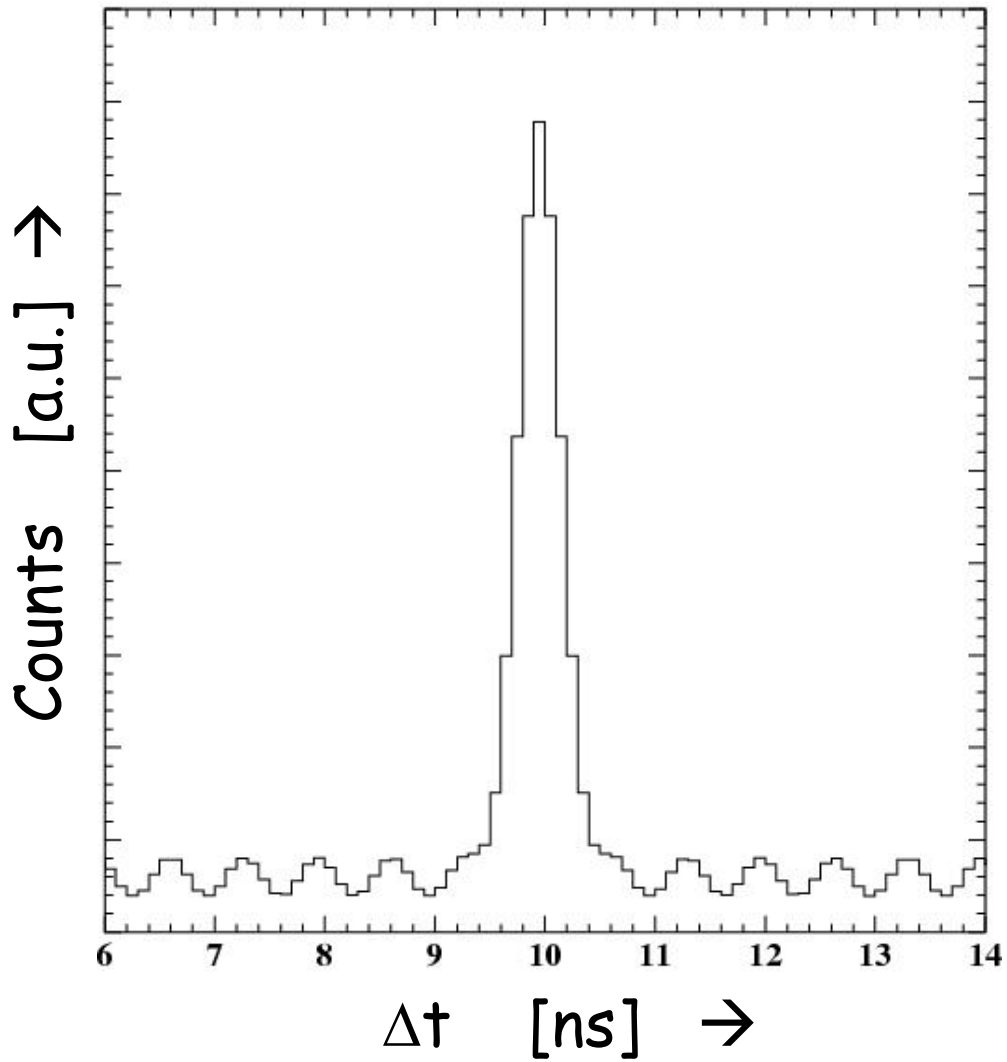
Illustration for 1.5 GHz RF

Timing resolution of JLab experiments is < 0.5 ns (FWHM)

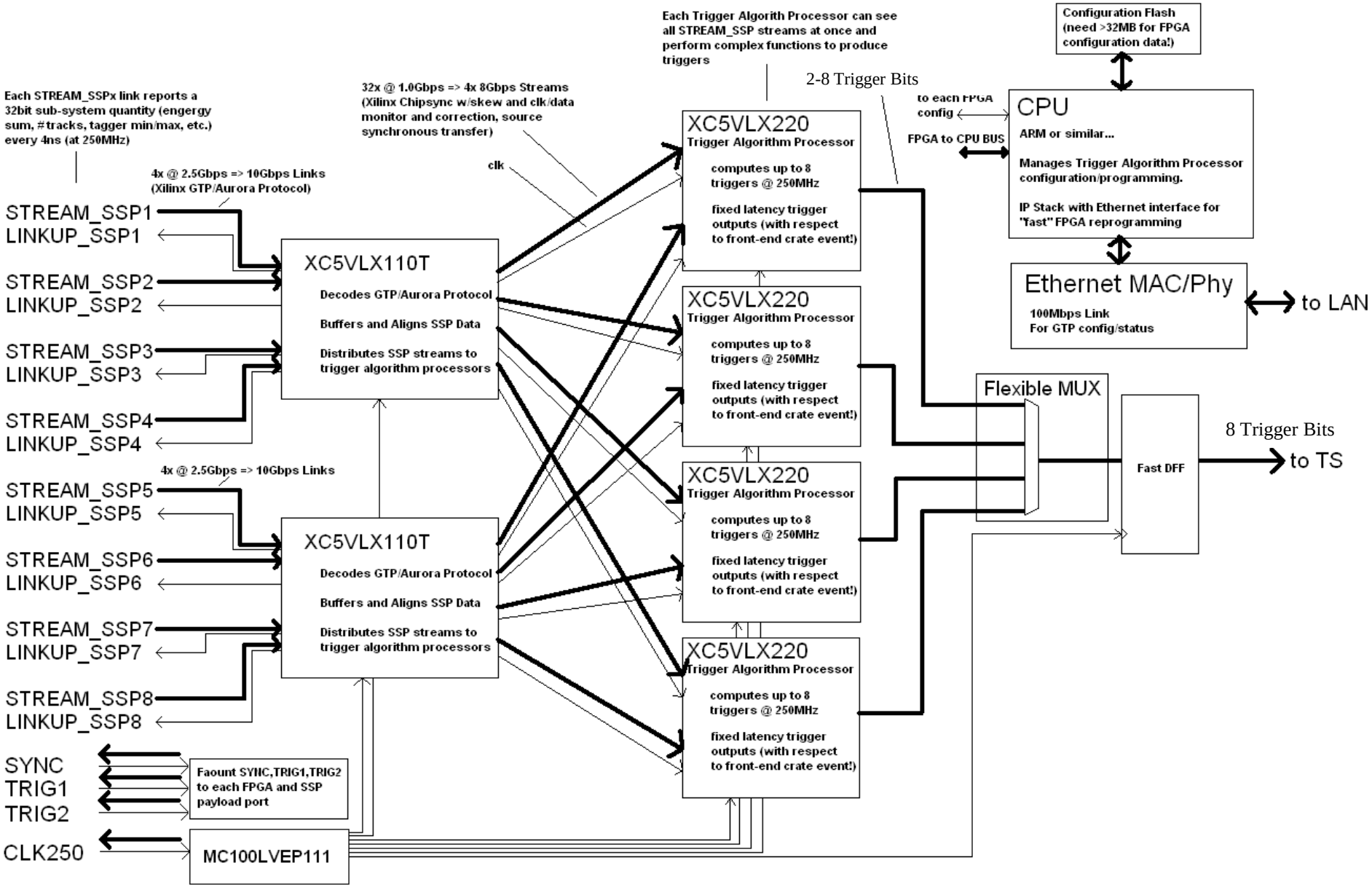
→1.5 GHz, or 2/3 ns bunch separation, is too short to pick the right bucket. But, one still sees bumps and valleys!

→ good coincident event determination by subtracting three random timing peaks from coincident + two random peaks.

R/A = 10 in this example



GTP Logic


Each STREAM_SSPx link reports a 32bit sub-system quantity (engergy sum, #tracks, tagger min/max, etc.) every 4ns (at 250MHz)
4x @ 2.5Gbps => 10Gbps Links (Xilinx GTP/Aurora Protocol)
32x @ 1.0Gbps => 4x 8Gbps Streams (Xilinx Chipsync w/skew and clk/data monitor and correction, source synchronous transfer)
clk
Each Trigger Algorith Processor can see all STREAM_SSP streams at once and perform complex functions to produce triggers
2-8 Trigger Bits
Configuration Flash (need >32MB for FPGA configuration data!)
to each FPGA config
FPGA to CPU BUS
CPU
ARM or similar...
Manages Trigger Algorithm Processor configuration/programming.
IP Stack with Ethernet interface for "fast" FPGA reprogramming
Ethernet MAC/Phy
100Mbps Link
For GTP config/status
to LAN
STREAM_SSP1
LINKUP_SSP1
STREAM_SSP2
LINKUP_SSP2
STREAM_SSP3
LINKUP_SSP3
STREAM_SSP4
LINKUP_SSP4
XC5VLX110T
Decodes GTP/Aurora Protocol
Buffers and Aligns SSP Data
Distributes SSP streams to trigger algorithm processors
4x @ 2.5Gbps => 10Gbps Links
STREAM_SSP5
LINKUP_SSP5
STREAM_SSP6
LINKUP_SSP6
STREAM_SSP7
LINKUP_SSP7
STREAM_SSP8
LINKUP_SSP8
XC5VLX110T
Decodes GTP/Aurora Protocol
Buffers and Aligns SSP Data
Distributes SSP streams to trigger algorithm processors
XC5VLX220
Trigger Algorithm Processor
computes up to 8 triggers @ 250MHz
fixed latency trigger outputs (with respect to front-end crate event!)
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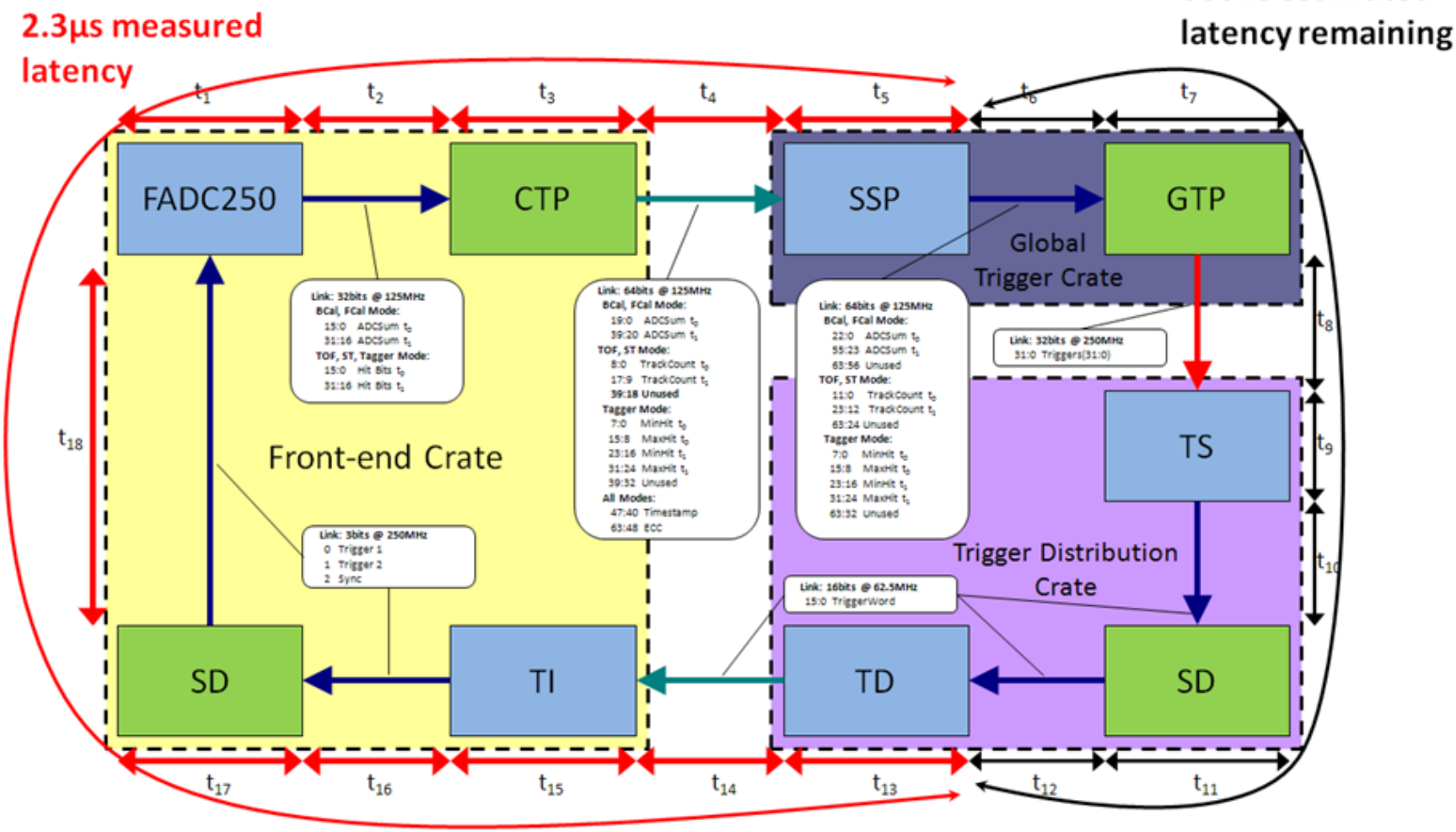
XC5VLX220
Trigger Algorithm Processor
computes up to 8 triggers @ 250MHz
fixed latency trigger outputs (with respect to front-end crate event!)
Flexible MUX
Fast DFF
8 Trigger Bits
to TS
SYNC
TRIG1
TRIG2
Faount SYNC,TRIG1,TRIG2 to each FPGA and SSP payload port
CLK250
MC100LVEP111

GlueX Level 1 Timing



2.3µs (measured) + 660ns (estimated) < 3µs!