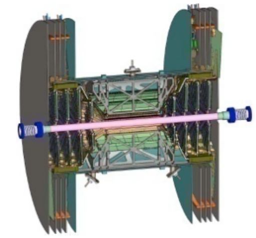
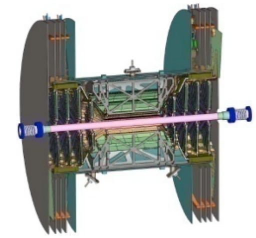


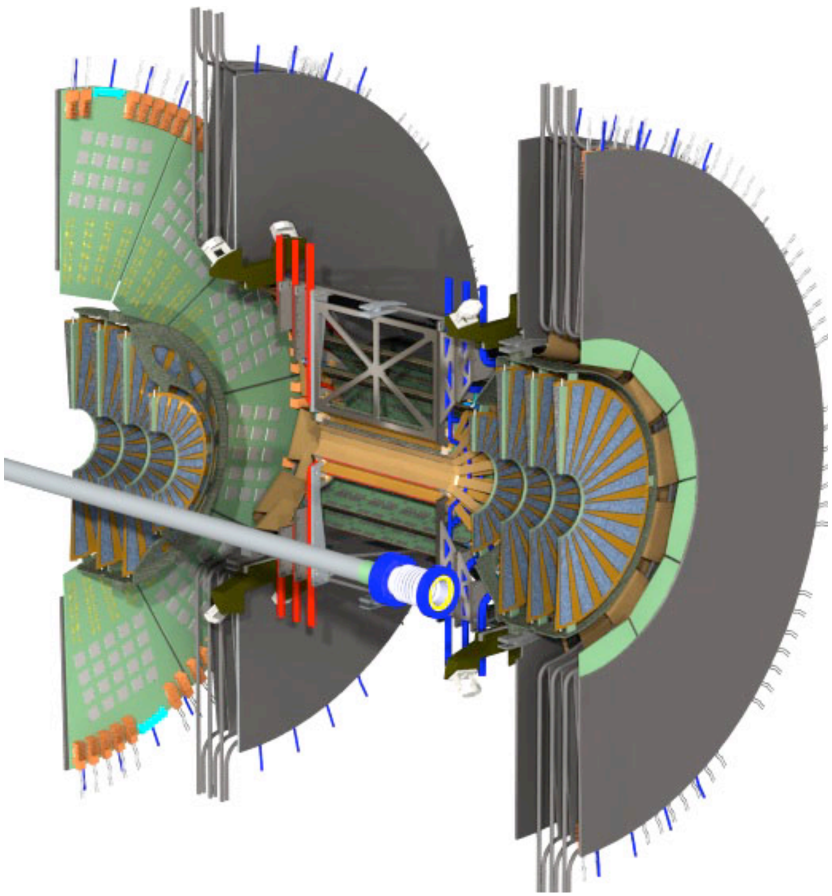
FVTX Electronics

(WBS 1.5.2, 1.5.3)

Sergey Butsyk
University of New Mexico

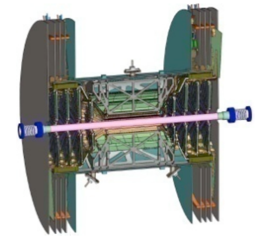
Introduction Comments



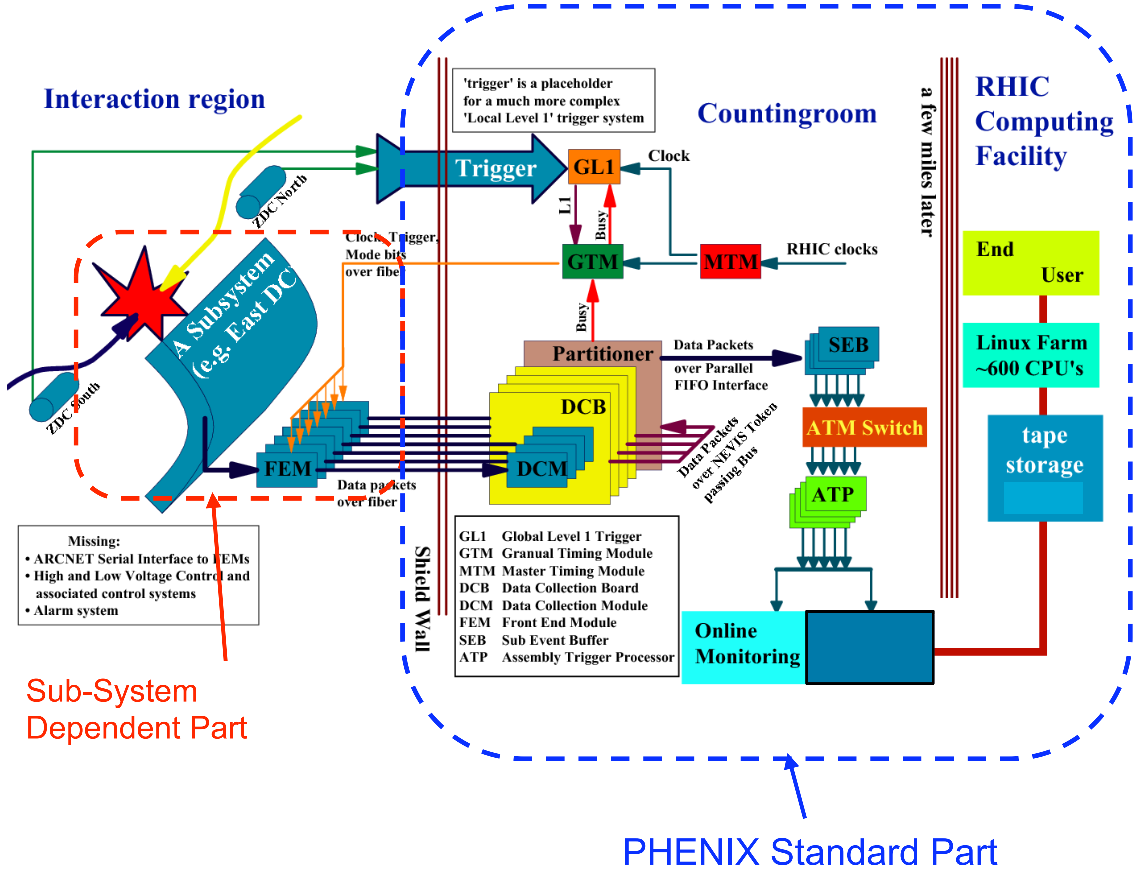


- **FVTX detector**
  - Over 1 Mil strip channels
  - "Data push" architecture (hit is sent out of the FPHX chip any time it was created)
- **PHENIX DAQ standards**
  - Triggered readout interface (data sampled, digitized and shipped out only when Level1 trigger request arrives)
- **FVTX DAQ should be able to bridge the gap between two different readout concepts and integrate FVTX detector into PHENIX DAQ environments**

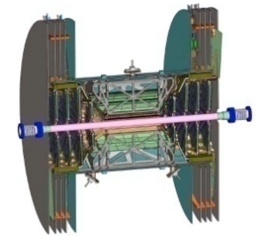
PHENIX Data Aquisition

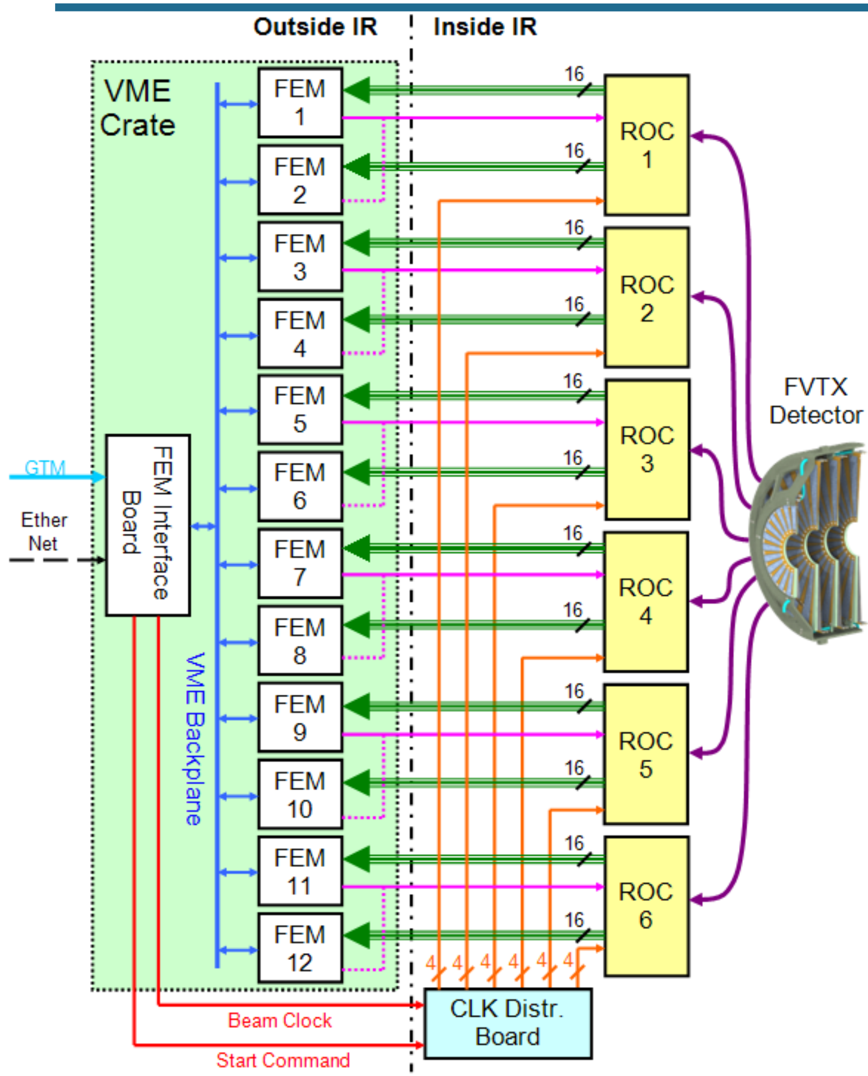


- RHIC beam clock ~ 9.4 MHz
- Data buffered by Front End Module (FEM) for 64 beam clocks
- LVL-1 Trigger issued with fixed delay w.r.t. collision
- FEM sends the data from the collision bucket to DCM in a data packet format
- Event is constructed from the packets, corresponding to the same event, by Event Builder



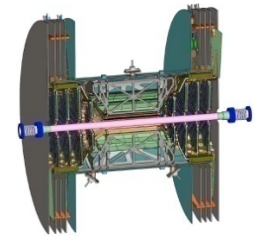
FVTX Readout Strategy





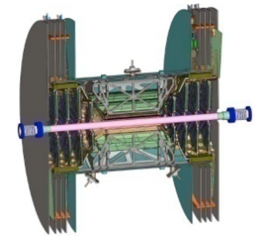
- ½ of each detector arm is read out independently
- 6 ROC cards collect and compress the data from the detector
- Each ROC send two 16 fiber output to two FEM boards in the Counting House
- Slow Control fiber send control data stream up/down the FEM↔ROC link
- Clock Distribution Board distribute Beam Clock and Start signals to individual ROC boards (the signals are sent over the optical fibers)

Overall System Status



Quantity	Description	Pre-Prod	1st article	Production	Status
24	ROC Boards	02/09	11/10	01/11	To be submitted for production before end of the month
48	FEM Boards	02/10	10/10	11/10	1st article received
4	FEM Interface Boards	02/10	08/10	10/10	Production finished
4	Clock Distribution Boards			05/09	Production finished
4	VME Crates				Purchased
96	12 ch Fiber cables				To be ordered
32	Duplex Fiber cables				To be ordered

Important Accomplishments



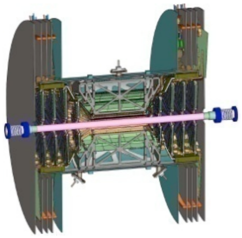
1. *Developed and Tested Fiber Optics communication between ROC and FEM using pre-production FEM board*

2. *Tested full functionality of pre-production FEM Interface Board*

3. *Implemented triggered readout of the FEM Board in calibration mode*

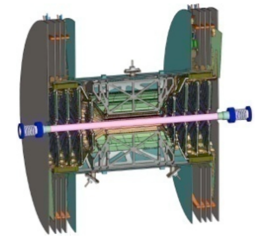
4. *Finished design of the production ROC Board*

5. *Purchased all the long lead time components for all the boards in production quantities*



1. *Fiber Optics Communications*

Pre-production Prototypes



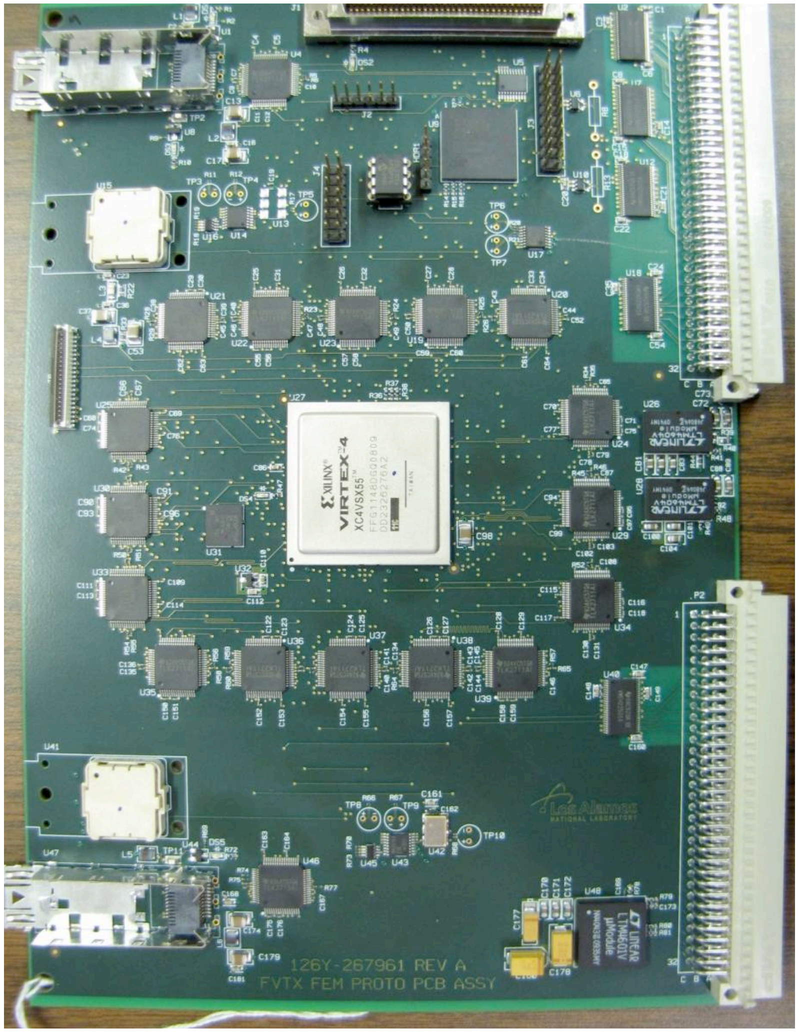
SC Fiber

Data Fiber 0

LED Panel

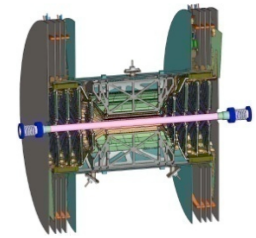
Data Fiber 1

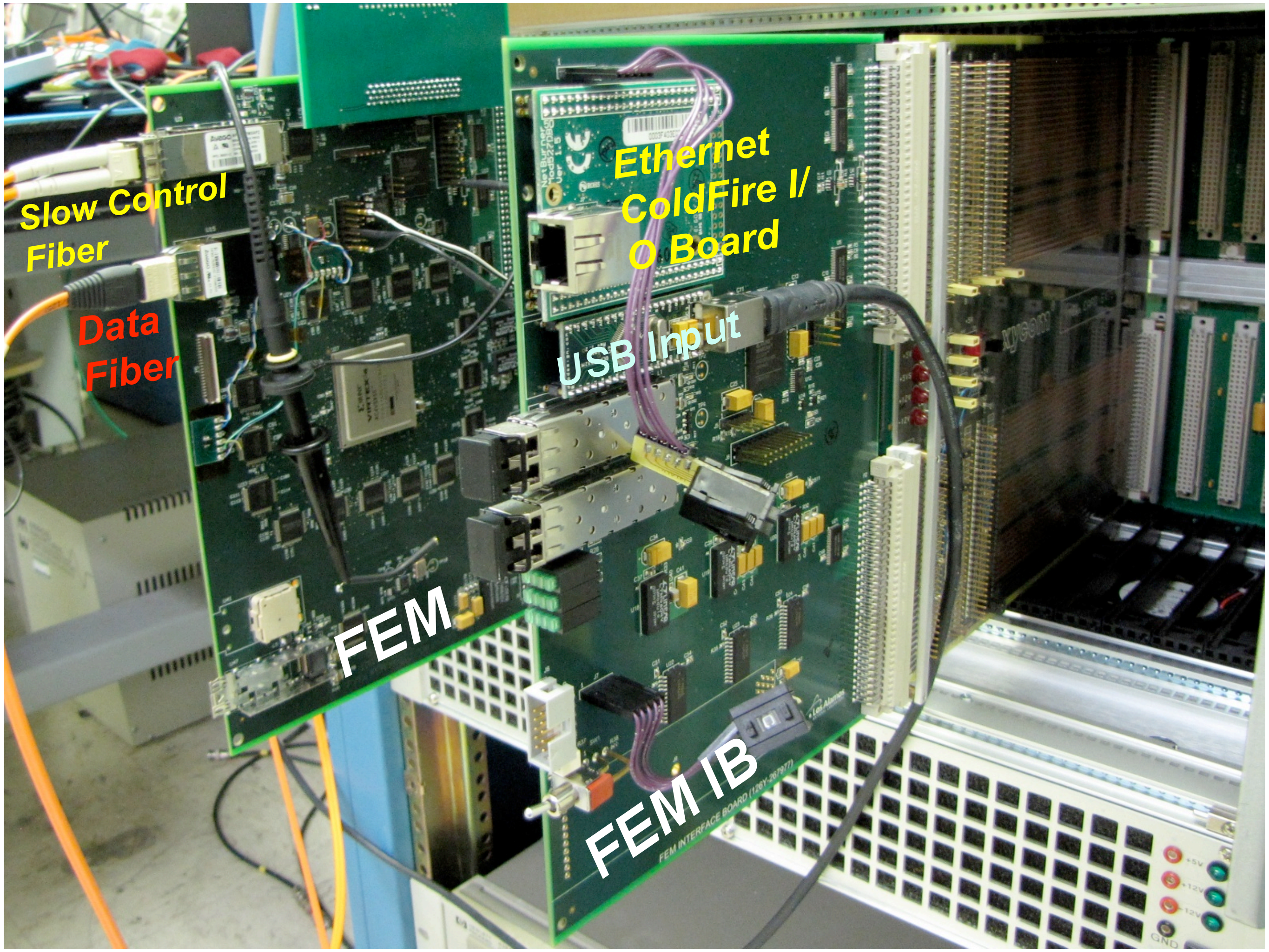
DCM Fiber



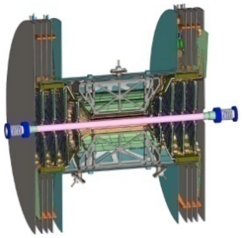
- FEM and FEM_IB prototypes arrived on 01/27/10
- Started developing FO communication protocol
- Basic idea:
  - Send synchronizing commas for TLK2711
  - Transmit 3 unique data words
  - On the receiving side, look for such unique word sequence and once it is found – consider link established
- Slow Control communication between FEM and ROC in both directions was established first

Initial Test Setup



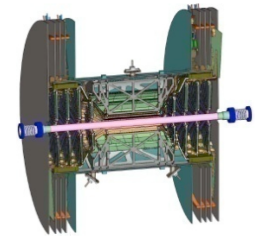


Problems Uncovered

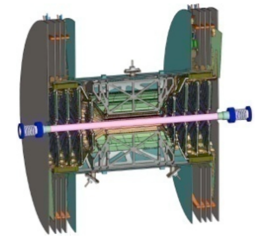


- FEM IB had USB module was rotated 180° from its desired placement
- Data receiving ser/des missed reference clock which is necessary to recover RX clock by ser/des chip (TLK2711). The following fix let us establish FO link for 2 data fibers:
  - 2 copies of SC TX_CLK clock on the FEM were wired to TX_CLK pins of TLKs, providing a proper reference
  - Data clock Oscillator on the ROC was changed from to match SC transmission rate
- After those changes we were able to establish 32 bit transmission between ROC and FEM over 2 fibers
- There were minor issues with the VME backplane pins used to send differential signals

1. Main Conclusions

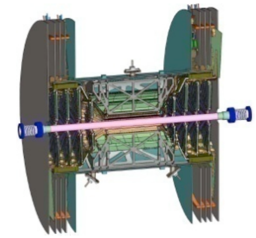


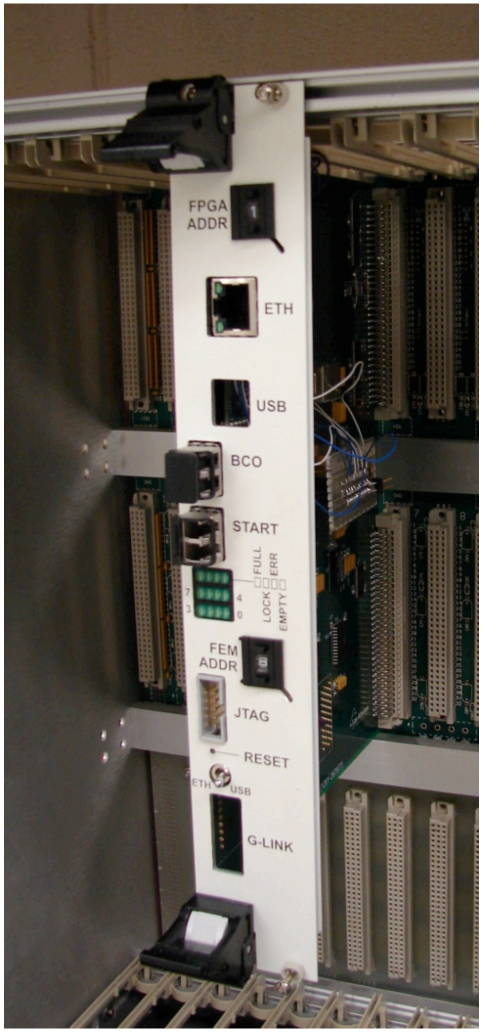
- After fixing all the uncovered issues FEM 1st article was received and FEM_IB went for production
- 1st article of FEM board has been received in October 2010 and showed that all the 16 data channels find the synchronization 3 word data sequence 100% efficiently
- We were able to collect calibration data at full (125 MHz) transmission clock speed
- Slow Control FO communication chain is working reliably in both directions



2. FEM Interface Board Testing

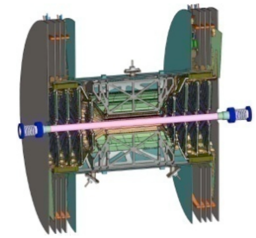
FEM Interface Board



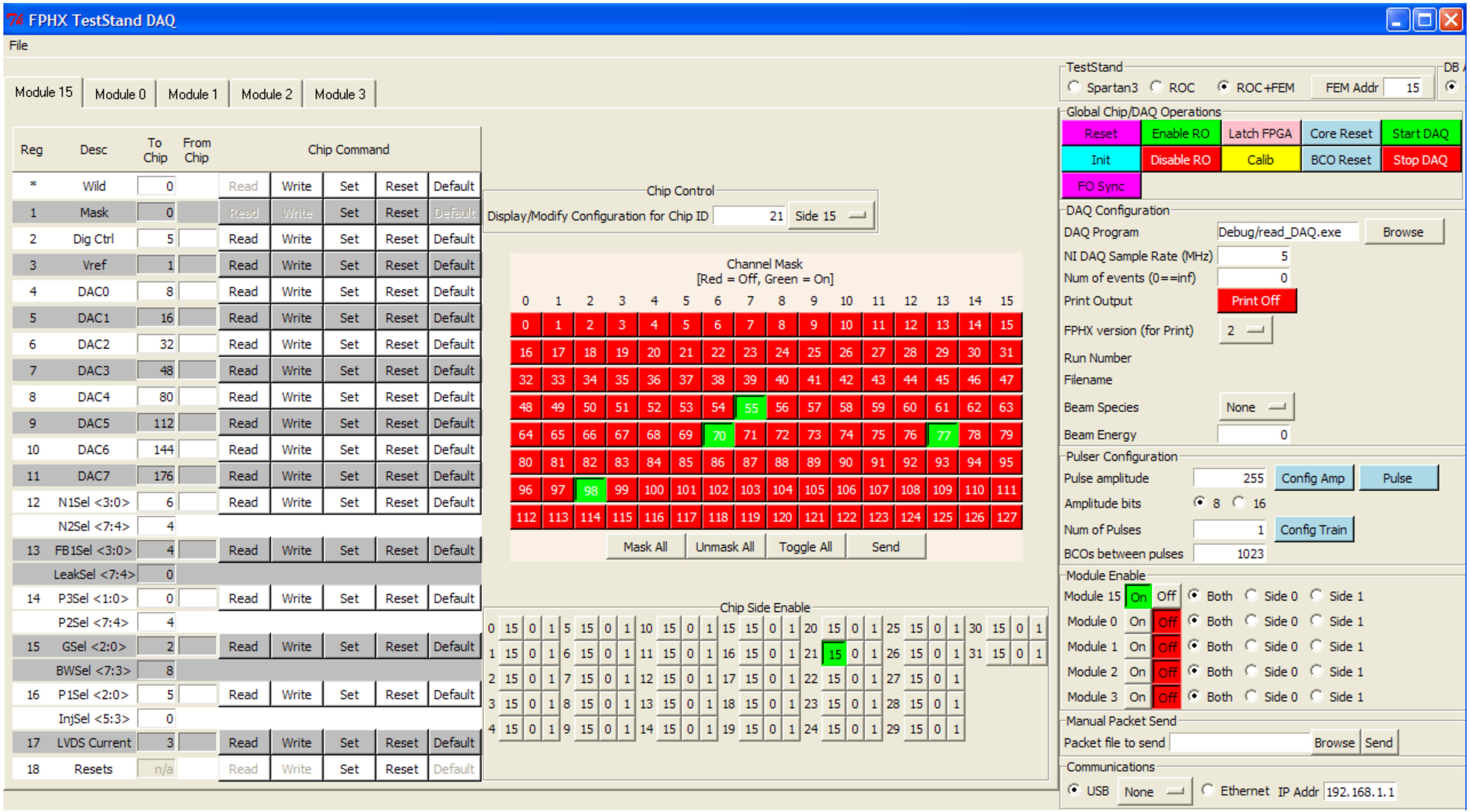


- FEM Interface Board has successfully performed the full list of tasks that it was designed for:
  - USB and Ethernet communication with host PC
  - Transmission of Beam Clock and Start signal to Clock Distribution board
  - Remote programming of any FPGA on the ROC
  - Distribution of low skew differential clock signals over VME backplane

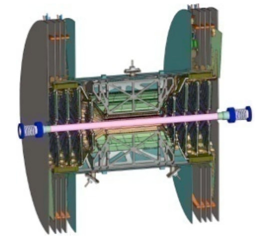
Slow Control Expert GUI



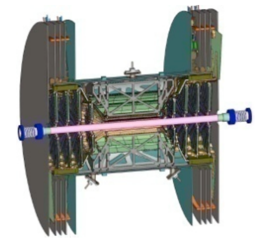
Python Based GUI control various parameters over USB or Ethernet



2. Main Conclusions

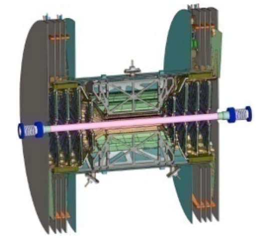


- Pre-production FEM Interface Board has been tested to its full capacity
- 1st article of FEM_IB showed that all the fixes needed had been implemented and full production quantities had been ordered and received
- Clock Distribution board functionality had been tested in this process and performed as expected



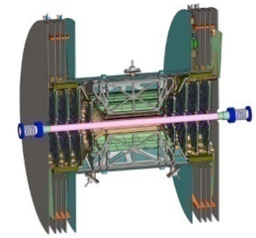
3. FEM Triggered Readout

FEM Code Validation

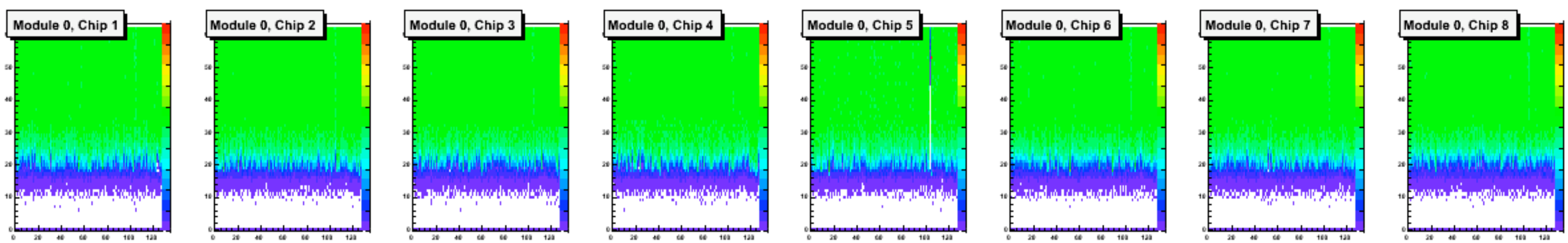


- FEM has been designed to provide buffering over the last 64 consecutive beam crossings
- Upon trigger arrival FEM calculates a bucket of interest and send its content to the output
- The main idea of this whole process had been successfully simulated and prototyped long time ago
- We were able to implement triggered readout for the full calibration chain in August 2010 using FEM board pre-production prototype

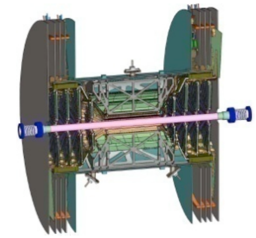
Triggered Readout



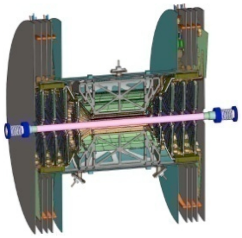
- The basic idea is following:
  - Take pulsing request from the ROC
  - Delay this signal by 30 beam clocks
  - Send this signal as trigger to the FEM over the Slow Control Fiber
  - Start the BCO counter on the FPHXs and on the FEM synchronously
  - Adjust delay to catch the proper clock bucket
- This all had been successfully implemented and showed the results identical to trigger-less calibration



3. Main Conclusions

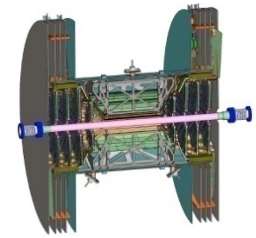


- Triggered readout of Calibration data with full fiber optics data transmission worked fine
- 4 event buffering had been tested by generating trigger in 4 consecutive beam crossings
- FEM code showed no problem running in multi-event readout mode and showed an expected slewing of hits with low pulser amplitude to the next clock bucket



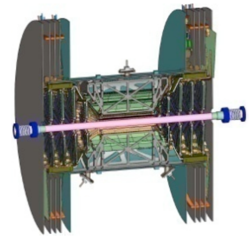
4. ROC Development

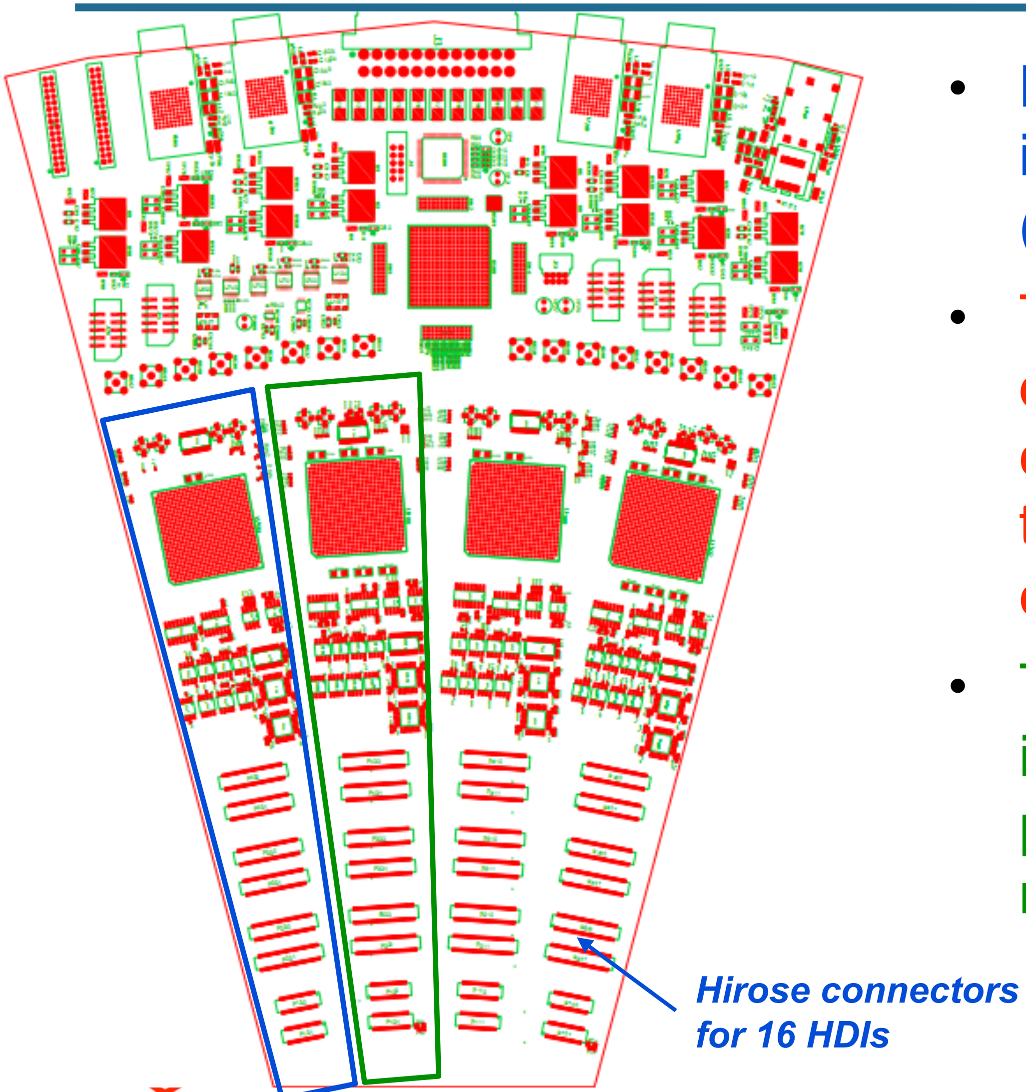
ROC Board Development



- Production ROC has been slipping in schedule in 2010 mainly due to:
  - Complexity of design
    - Limited board space for 1050 differential pairs and 2933 components.
      - Increased the number of layers used in the board design
      - Deployed "stitching" technique for routing differential pairs
  - Availability of qualified designers at LANL
- All the long lead time components in production quantities had been ordered
- Design is finalized in November 2010 and sent for production
- 1st article should be available in December, if tests show no issues, we start production

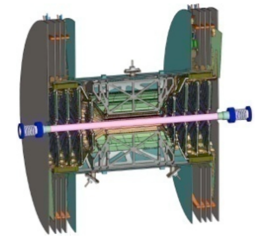
ROC Board Layout





- Design had been broken into wedge like blocks (green and blue)
- Those blocks carry LVDS data from extension cables to the FPGA are the most dense and challenging to design
- The remaining schematics is nearly identical to the pre-production ROC and relatively easy to trace

22 Layer Board Stack-Up



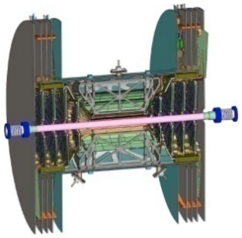
126Y-267898 FVTX FABRICATION STACKUP

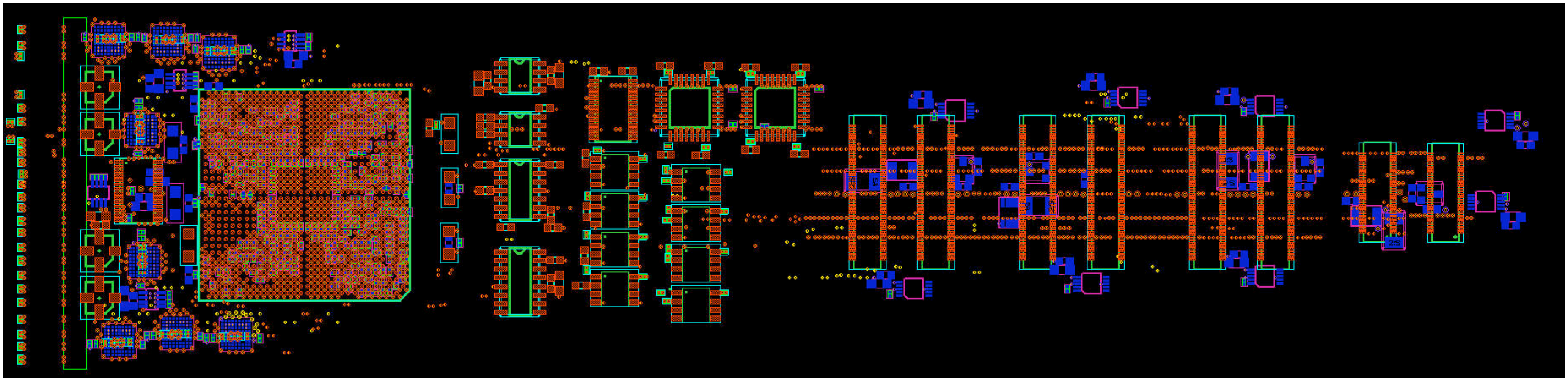
Los Alamos NATIONAL LABORATORY

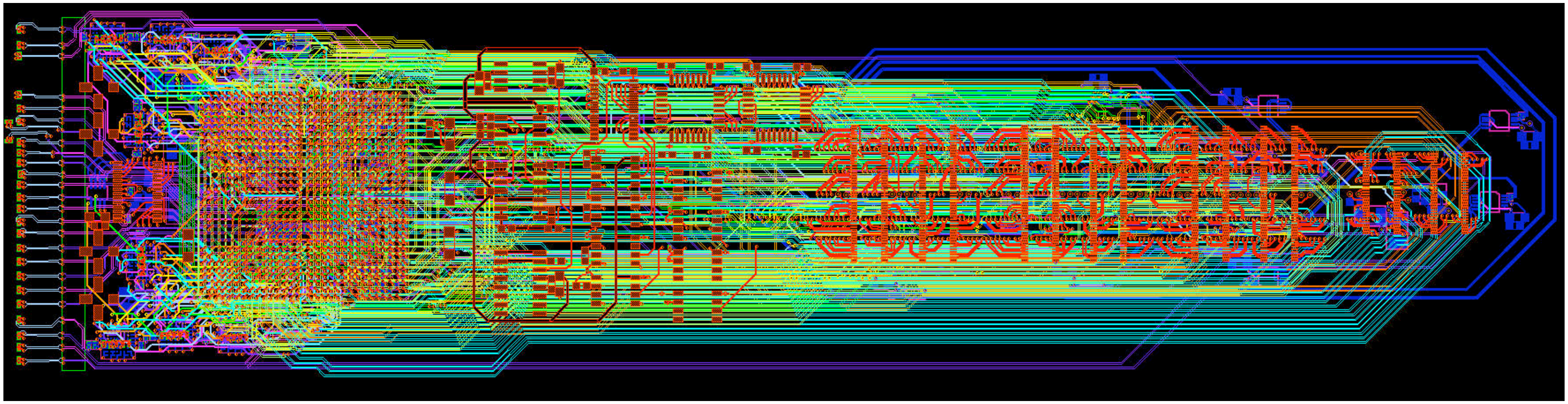
22 layers Class 2			GND				POSSIBLE VIAS 1808 (.018 P .008 H) 2010 (.020 P .010 H)
1	copper 3/8 OZ	0.000525	.008 h			1	SURFACE Pair LYR 1 (4.5 w-5 sp)
	dielectric	0.0025	1-3				
2	copper 1/2 OZ	0.0007	0.018			2	GND /PWR PLANE
	dielectric	0.004					
3	copper 3/8 OZ	0.000525			.010 h	3	Pair LYR 2 (3.5 w-5 sp)
	dielectric	0.0045			1-22		
4	copper 1/2 OZ	0.0007			.020p	4	PLANE
	dielectric	0.004					
5	copper 3/8 OZ	0.000525				5	Pair LYR 3 (3.5 w-5 sp)
	dielectric	0.0045					
6	copper 1/2 OZ	0.0007				6	PLANE
	dielectric	0.004					
7	copper 3/8 OZ	0.000525				7	Pair LYR 4 (3.5 w-5 sp)
	dielectric	0.0045					
8	copper 1/2 OZ	0.0007		.008 h		8	PLANE
	dielectric	0.004		1-9			
9	copper 3/8 OZ	0.000525		.018 p		9	Pair LYR 5 (3.5 w-5 sp)
	dielectric	0.0045					
10	copper 1/2 OZ	0.0007				10	PLANE
	dielectric	0.004					
11	copper 3/8 OZ	0.000525		.008 h		11	Pair LYR 6 (3.5 w-5 sp)
	dielectric	0.0045		11-22			
12	copper 1/2 OZ	0.0007		.018 p		12	GND /PWR PLANE
	dielectric	0.004					
13	copper 3/8 OZ	0.000525				13	Pair LYR 7 (3.5 w-5 sp)
	dielectric	0.0045					
14	copper 1/2 OZ	0.0007				14	PLANE
	dielectric	0.004					
15	copper 3/8 OZ	0.000525				15	Pair LYR 8 (3.5 w-5 sp)
	dielectric	0.0045					
16	copper 1/2 OZ	0.0007	.006 h			16	PLANE
	dielectric	0.004	16-22				
17	copper 3/8 OZ	0.000525	.014 p			17	Pair LYR 9 (3.5 w-5 sp)
	dielectric	0.0045					
18	copper 1/2 OZ	0.0007	req			18	PLANE
	dielectric	0.004	for				
19	copper 3/8 OZ	0.000525	1/2 mm			19	Pair LYR 10 (3.5 w-5 sp)
	dielectric	0.0045	pitch				
20	copper 1/2 OZ	0.0007	bga			20	PLANE
	dielectric	0.004	on				
21	copper 1/2 OZ	0.0007				21	PLANE
	dielectric	0.0025					
22	copper 3/8 OZ	0.000525				22	SURFACE Pair LYR 1 (4.5 w-5 sp)

0.0032 ***FINISH COPPER FOR LAYERS 9 & 16 (.0016 EACH)
0.0038 ***FINISH COPPER FOR LAYERS 1 & 22

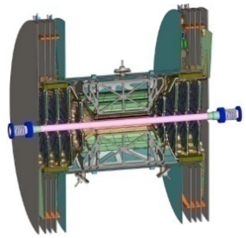
Manually Routed Section



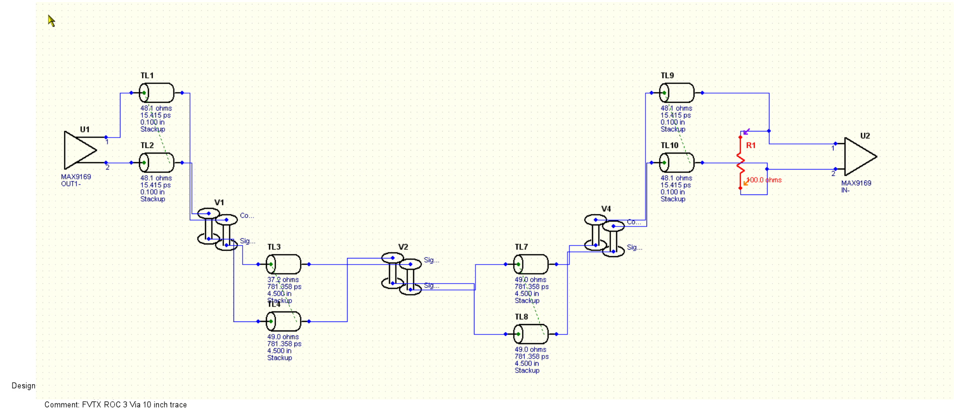


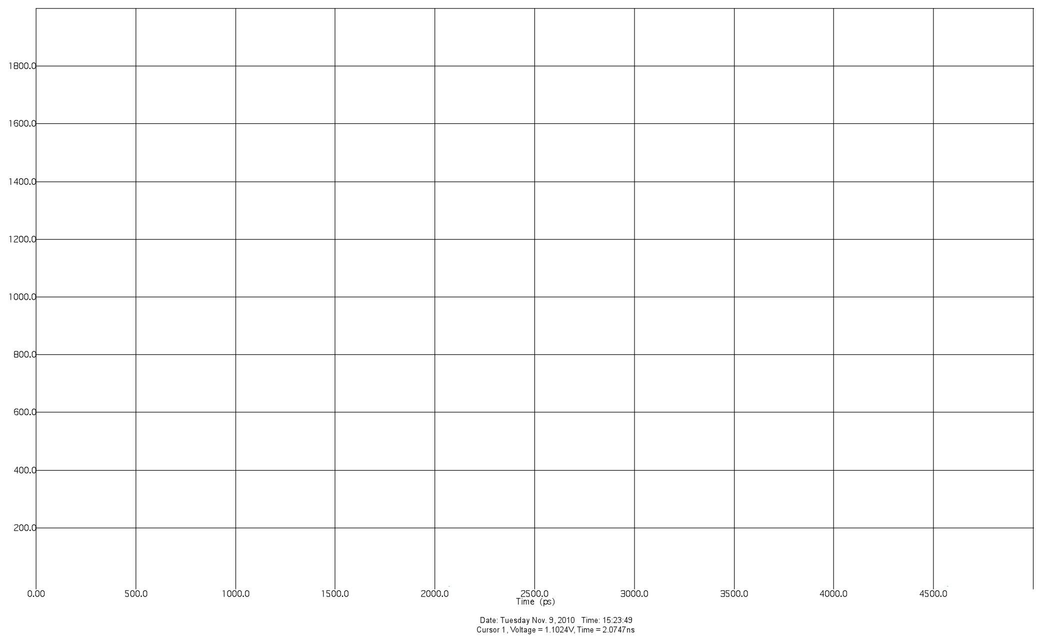


Stitching Circuit Simulation

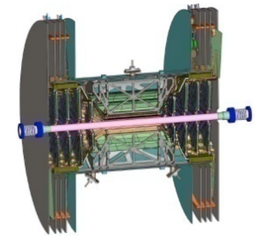


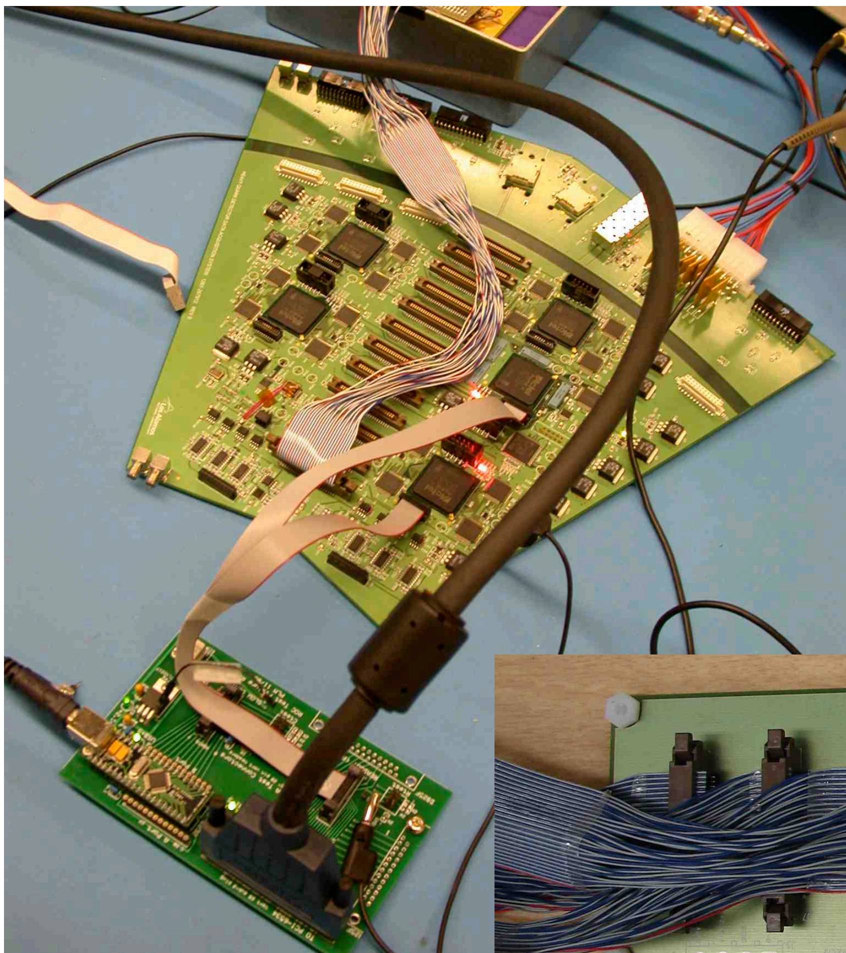
- Transmission line based on ROC board stack-up architecture
- 200 MHz Clock
- Used MAX9169 LVDS driver model
- 3.5 mil lines, 5 mil spacing on internal layers



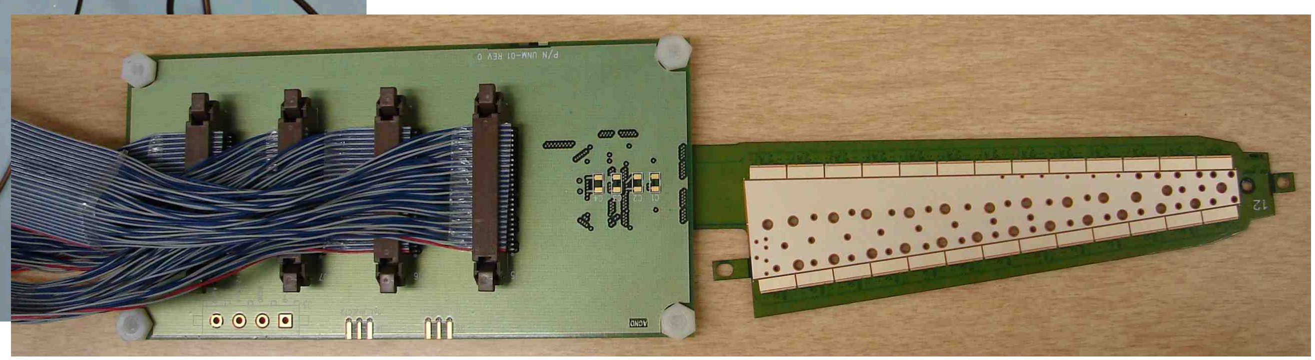


Wedge Testing

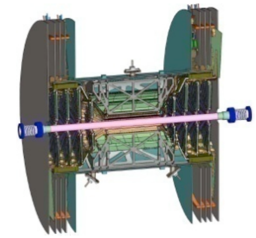


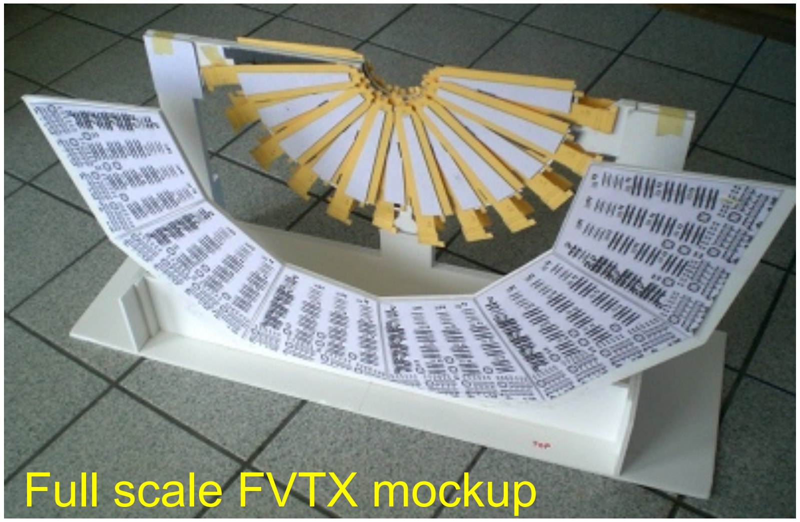


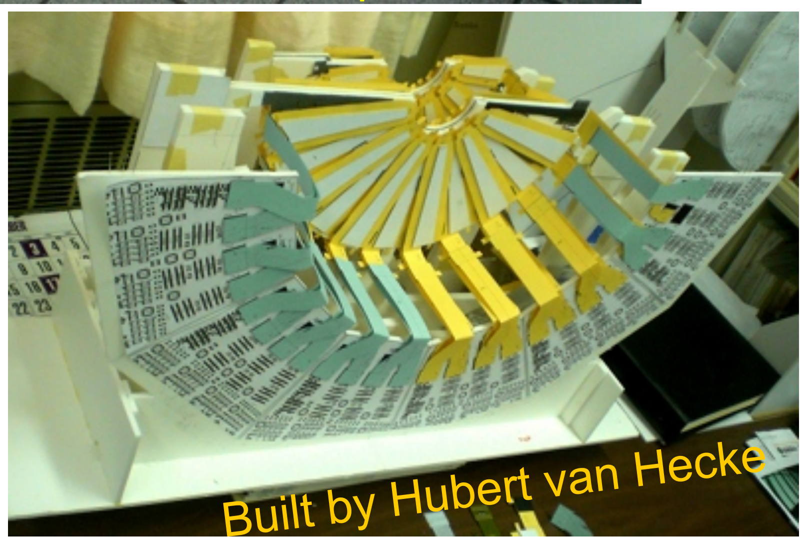
- 5 existing pre-production ROCs had been used extensively for testing assembled wedges
- Various Interface boards had been developed to transfer signals from small, large HDI as well as from small Extension Cable to pre-production ROC



Big Wheel ROC Testing

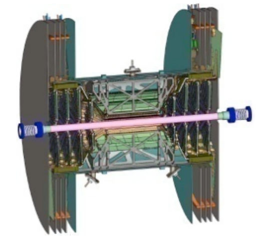






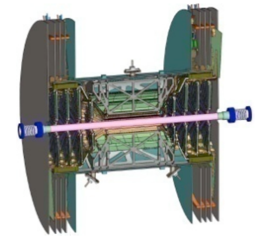
- ROC Board functionality is going to be tested with a reference wedge (large and small) plugged into each available slot
- The boards that have passed those tests are going to be installed into big wheel area and a station will be connected to the ROCs one by one

4. Main Conclusions



- ROC board design is finalized and is going to be submitted for manufacturing by the end of this month
- Testing of assembled wedges successfully accomplished by using pre-production ROC and varieties of interface boards
- Big Wheel assembly should be done with tested and approved ROC boards and the full assembly should be done station by station in the assembly area

Summary and Outlook



- Pre-production FEM and FEM_IB fully tested
- FEM_IB has been submitted for production
- FEM 1st article had been received and is being tested. No problems discovered so far
- ROC production board design in finished, expect to receive 1st article by the end of 2010 and submit full production batch at the beginning of 2011
- All the long lead time components for the boards had been purchased
- Software development for the Slow Control of multiple wedges has been developed
- Expect test of the readout of the full chain in PHENIX environment (with PHENIX GTM and DCM II) by the end of 2010

Snapshot of 2010 Results