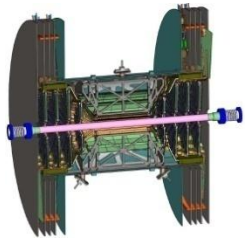
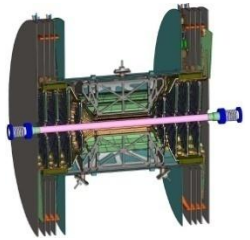


High Density Interconnect
WBS 1.4.3

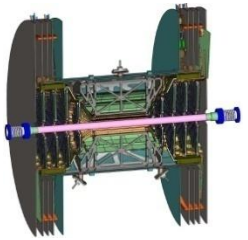
Douglas Fields

University of New Mexico



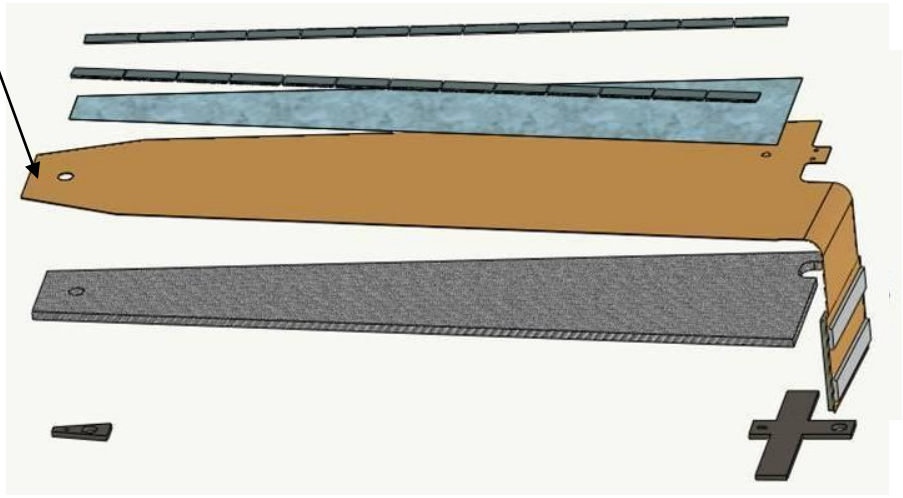
Talk Outline

- Prototype Overview
  - Design
  - Tests
  - Issues
  - Re-Design
- Production, Q/A Plans
- Summary Cost and Schedule
- Summary Technical



fVTX Prototype HDI Wedge Assembly (Nov. 08)

HDI

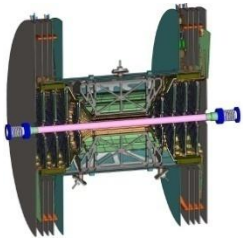


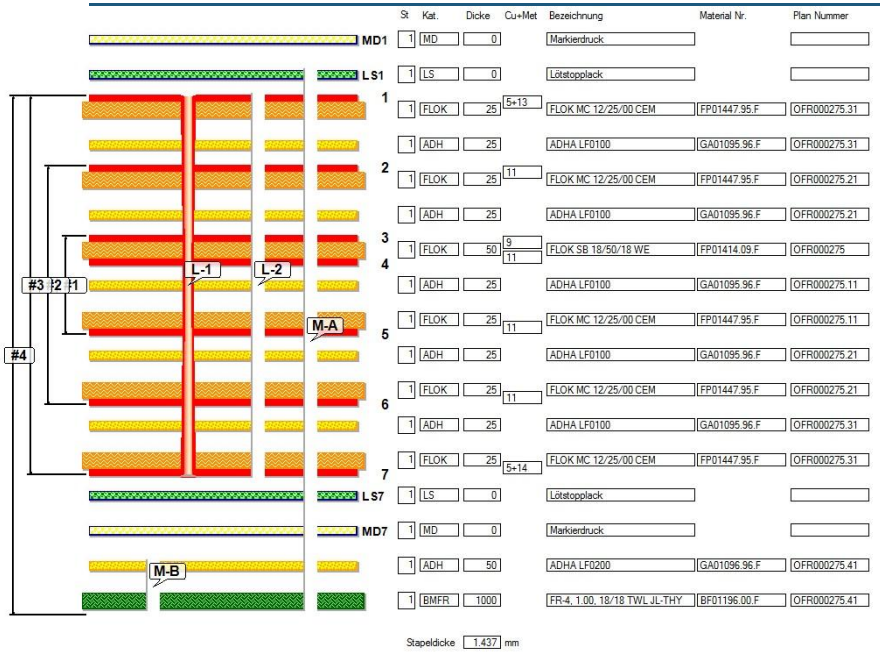
- **High Density Interconnect (HDI) – kapton flat cable to supply bias to sensor and power to FPHX chips, and transfer data from the chips to the read-out electronics**
  - **~440μm thick**
  - **7 copper planes, 6 Kapton films**
  - **Thickness/Rad length = 0.00425**

HDI trace count

2 R/O lines x LVDS pair x 26 chips	104	100Ω impedance
4 Download and Reset lines	4	100Ω impedance
2 Clocks x LVDS pair	4	100Ω impedance
1 Calibration line	1	50Ω impedance
	113	

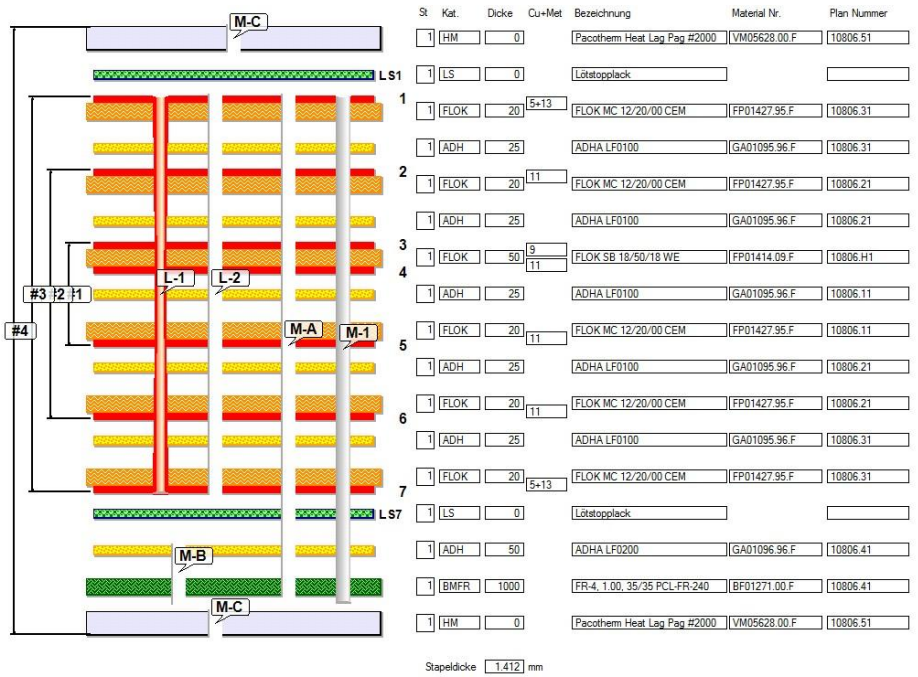
fVTX Prototype HDI Stackup

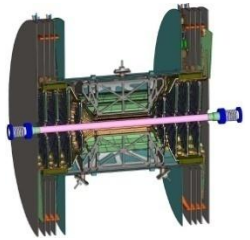




Original

Prototype Production





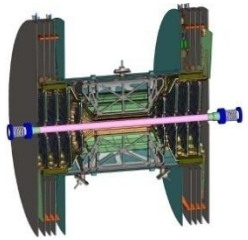
(Total thickness)/(Radiation length): 0.00419

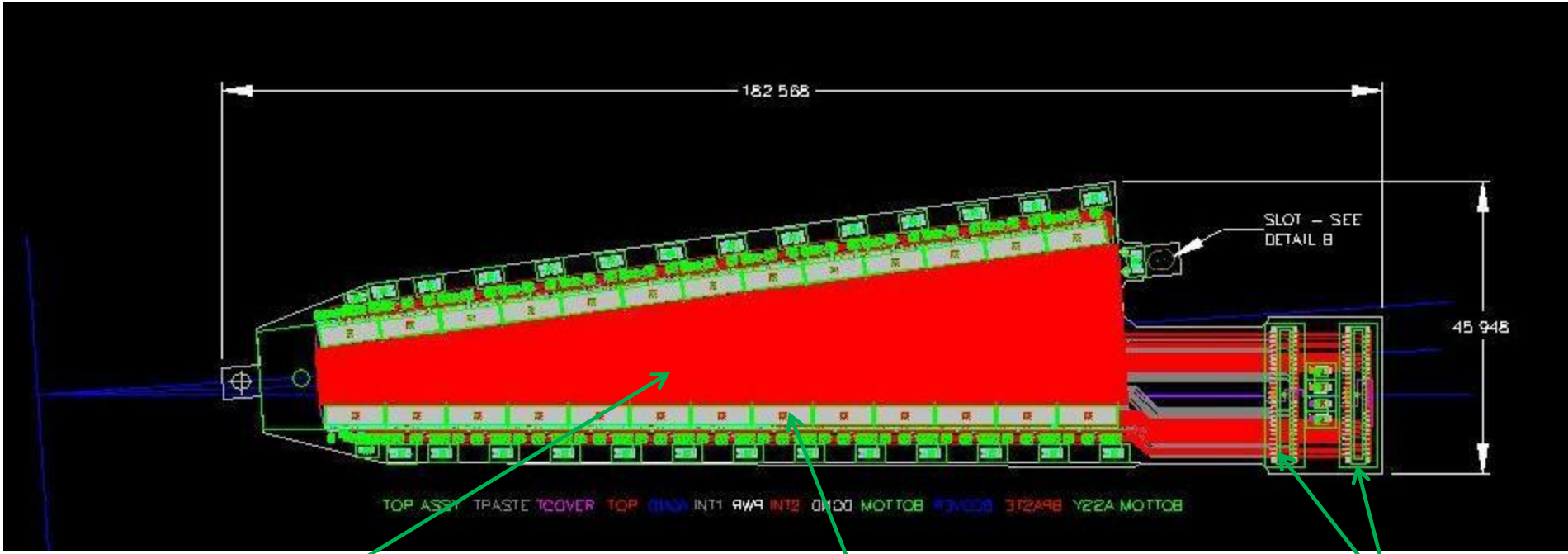
fVTX Prototype HDI
Layer Thickness and Radiation Thickness

Radiation lengths (cm) of Layers: copper: 1.43 kapton: 28.6 epoxy: 44.37

	#of layers	fraction of layers	thickness (μm)	R_L	thickness (μm)	Production	Imp target	Ref plane (layer)
top covercoat	1	0.2	38	0.171287	10	10		
copper 1	1	0.8	12	6.713287	25	18	50 SE	2
kapton 1	1	1	25	0.874126	25	20		
epoxy 1	1	1	12	0.270453	12	15		
copper 2	1	0.9	12	7.552448	12	11		
kapton 2	1	1	40	1.398601	25	20		
epoxy 2	1	1	12	0.270453	12	15		
copper 3	1	0.1	12	0.839161	12	9	100 DIFF	2,4
kapton 3	1	1	50	1.748252	50	50		
copper 4	1	0.9	12	7.552448	12	11		
epoxy 3	1	1	12	0.270453	12	15		
kapton 4	1	1	40	1.398601	25	20		
copper 5	1	0.1	12	0.839161	12	11	100 DIFF	2,4
epoxy 4	1	1	12	0.270453	12	15		
kapton 5	1	1	40	1.398601	25	20		
copper 6	1	0.9	12	7.552448	12	11		
epoxy 5	1	1	12	0.270453	12	15		
kapton 6	1	1	25	0.874126	25	20		
copper 7	1	0.2	12	1.678322	25	18	50 SE	6
bottom covercoat	1	0.7	38	0.599504	10	10		
Total thickness (μm) of HDI:			440	42.54264	365	334		

fVTX Prototype HDI Layout

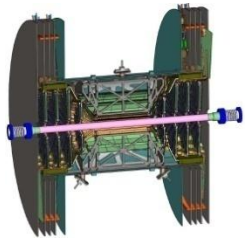




Sensor

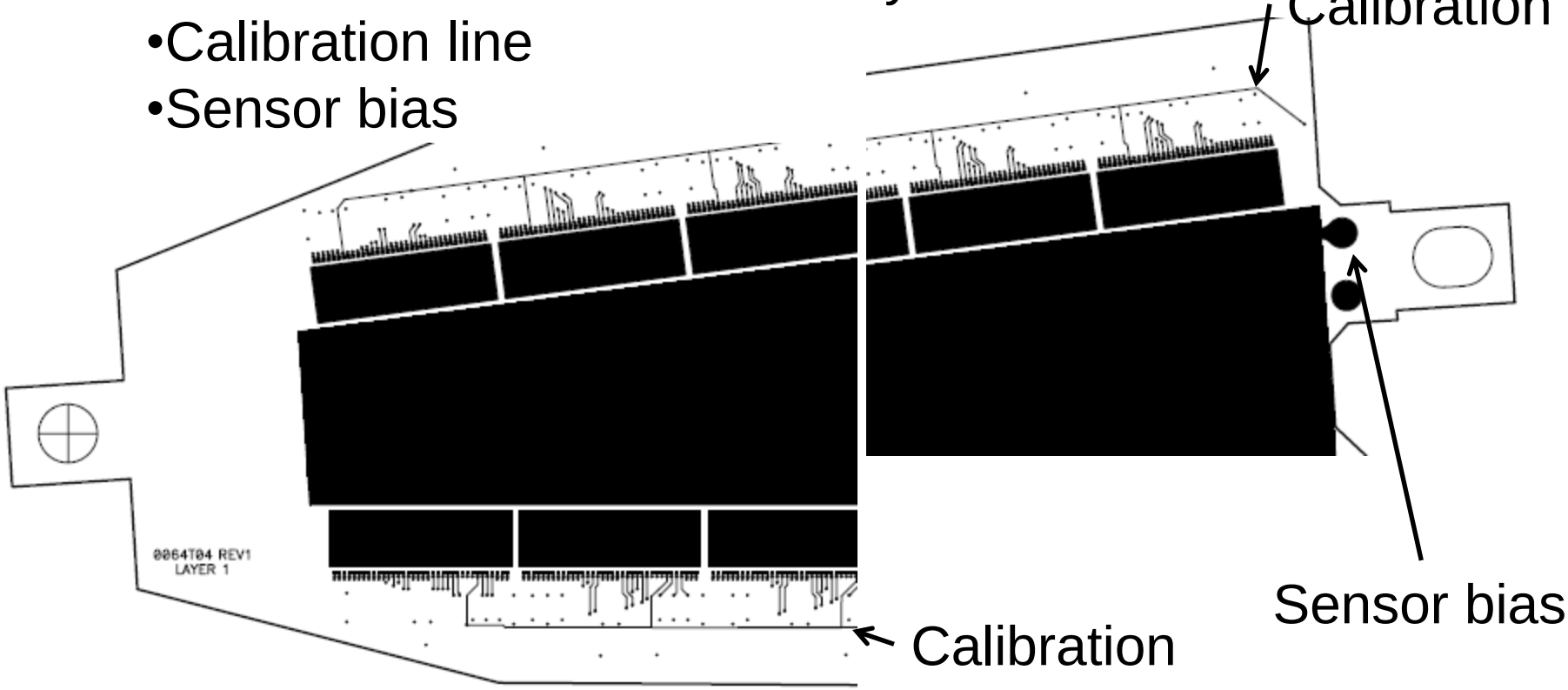
FPHXs

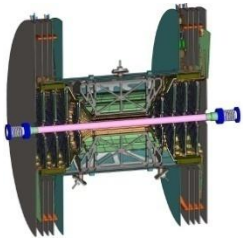
Connectors



fVTX Prototype HDI Layout

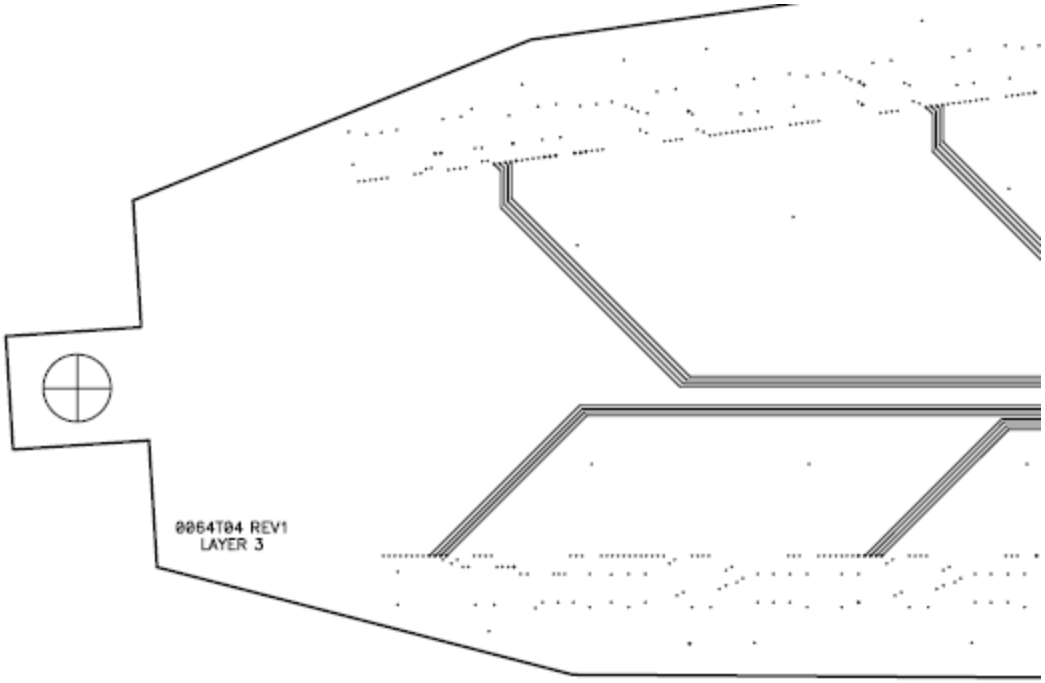
- Layer 1
  - Vias to internal and bottom layers
  - Calibration line
  - Sensor bias

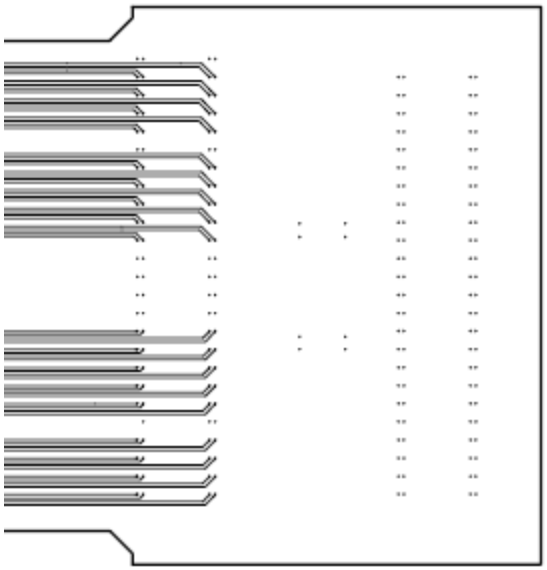


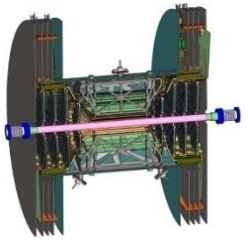


fVTX Prototype HDI Layout

- Layer 3
  - Read-out LVDS lines (partial)

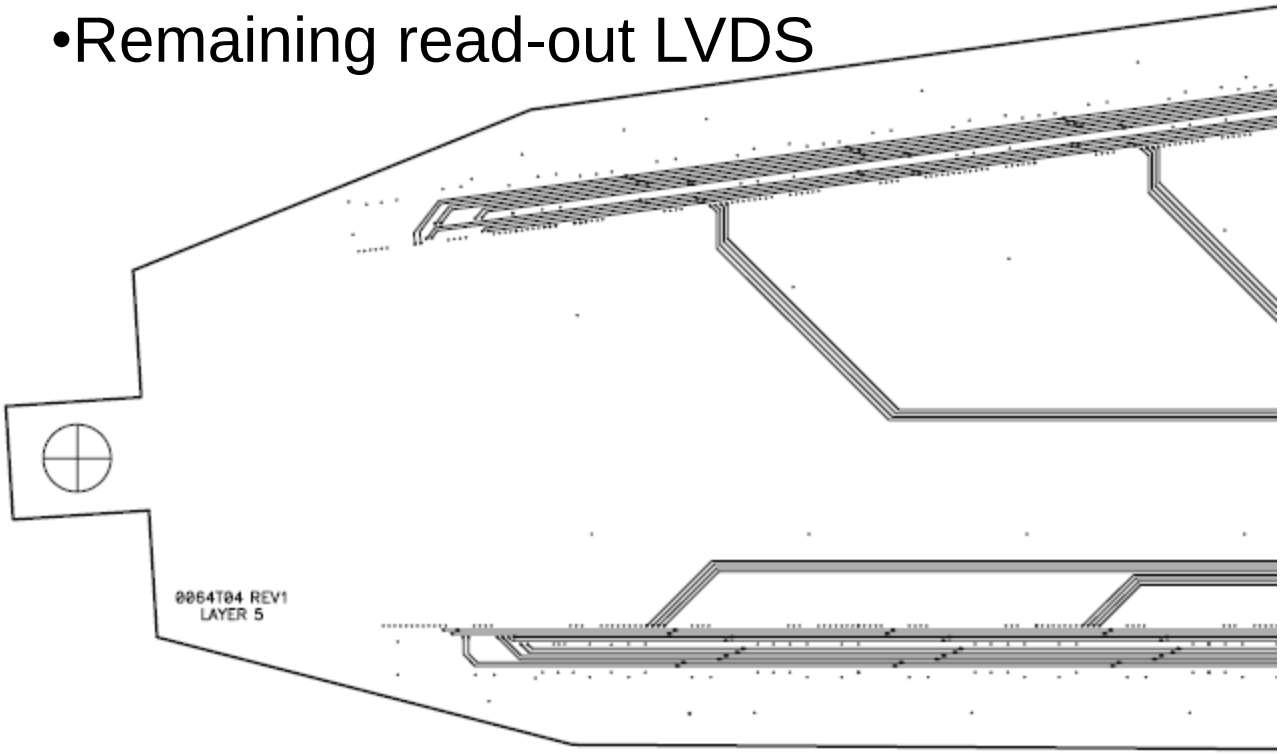


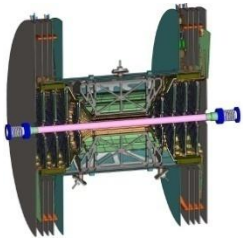




fVTX Prototype HDI Layout

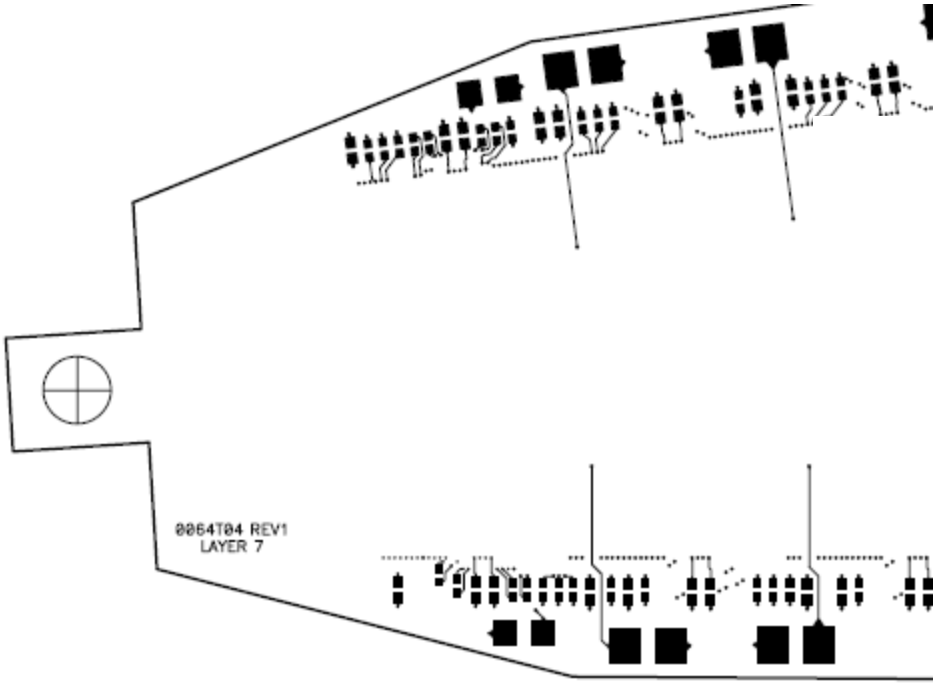
- Layer 5
  - Clocks and control
  - Remaining read-out LVDS

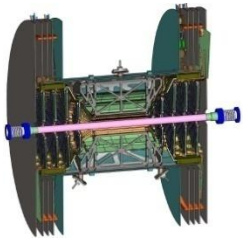




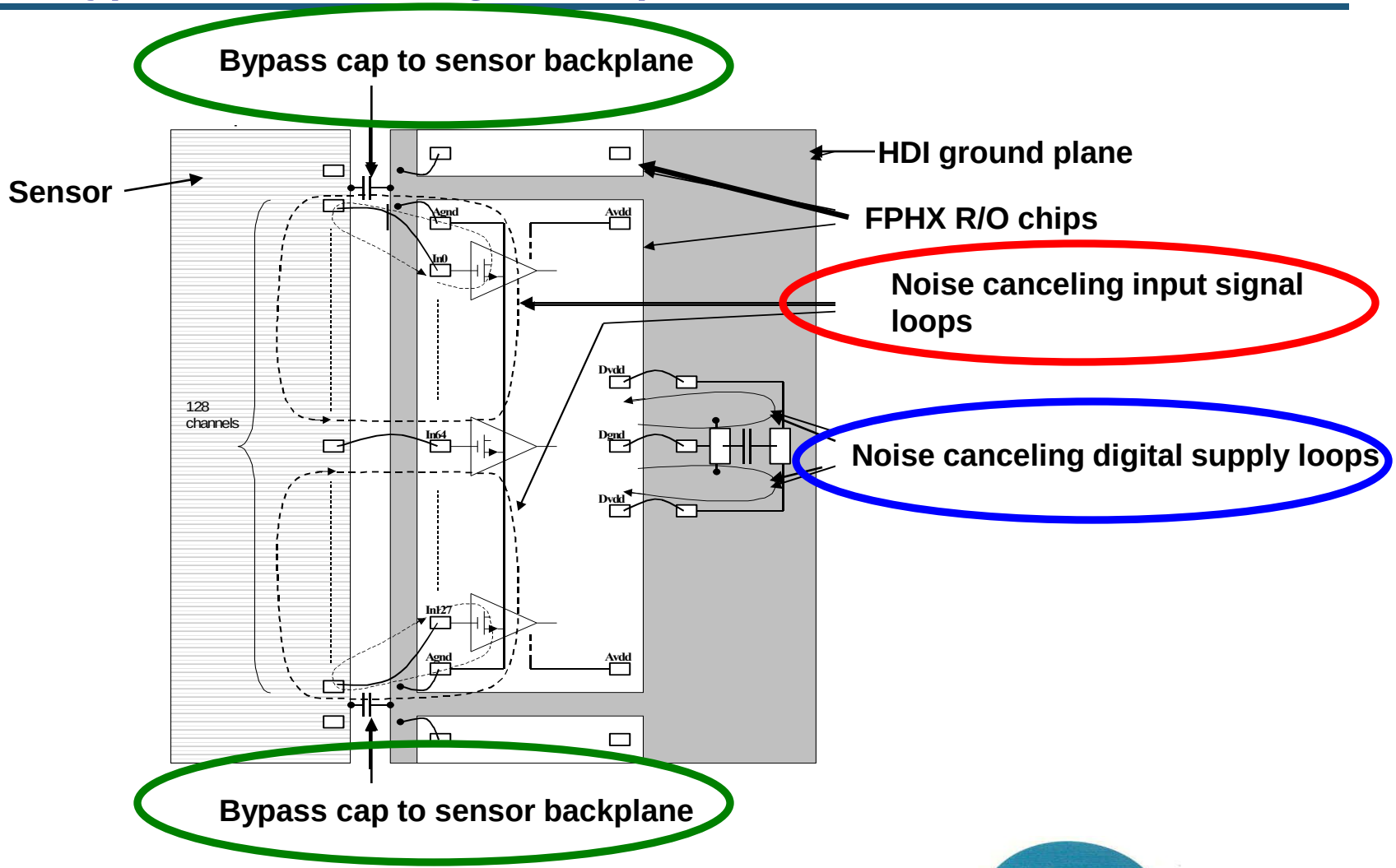
fVTX Prototype HDI Layout

- Layer 7
  - Filtering and termination, passive components

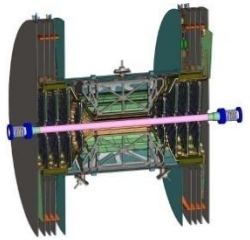




fVTX HDI
Prototype Power Filtering Concept



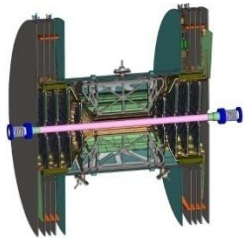
fVTX Prototype HDI Components

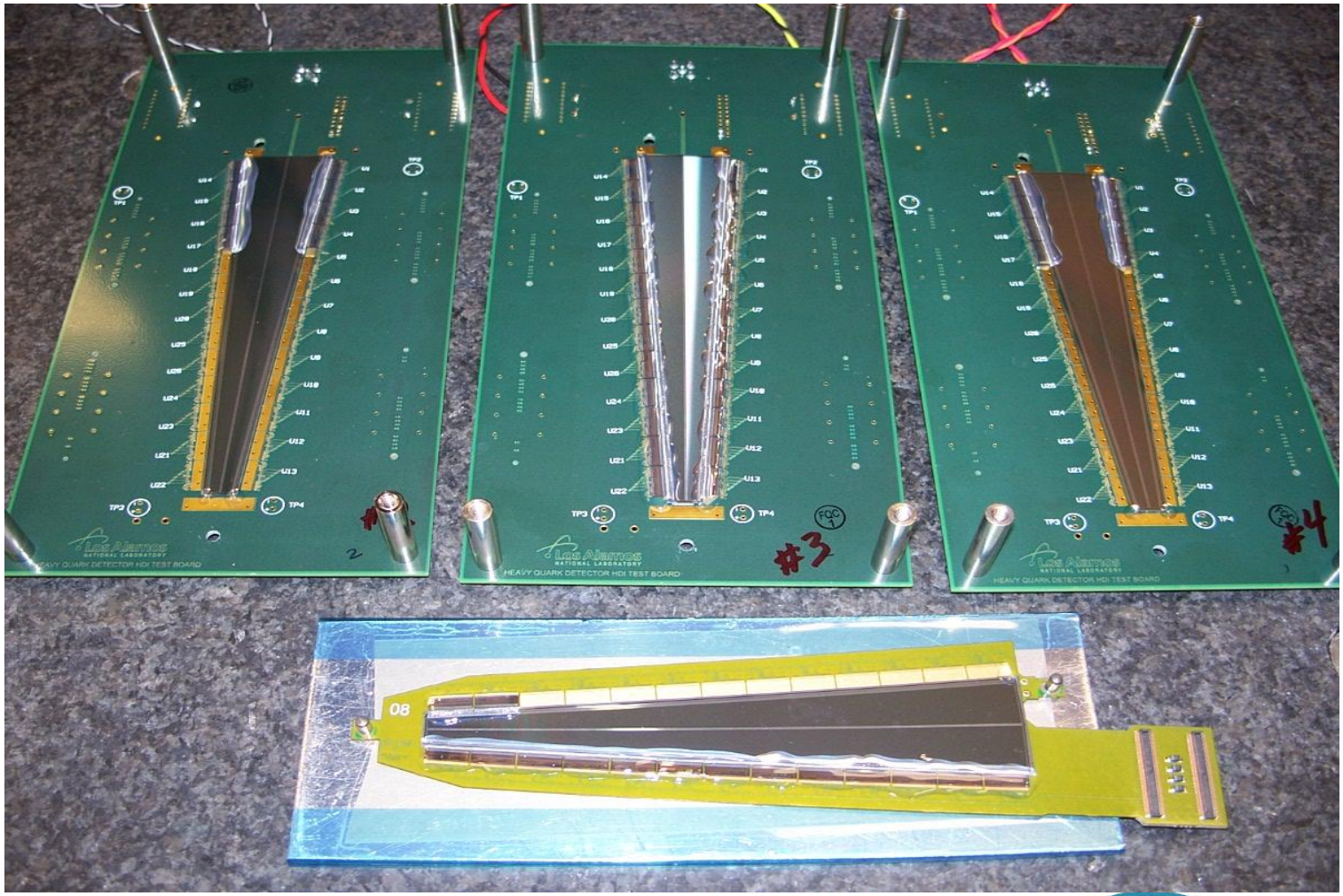


RefDes	Count	Description	Value	MPN	MFR
C1	4	CAPACITOR, SM TANTALUM, 0805	10u	TCP0G106M8R	ROHM
C5	27	CAPACITOR, SMD 0805, 200V NP0	470p	201T15N471JY6	AMC
C32	104	CAPACITOR, SMD 0201, 6.3V X7R	0.1u	ECJ-ZEB0J104K	PANASONIC
P1	2	PLUG, B-TO-B, 0.4MM, 100 PIN		DF18C-100DP-0.4V	HIROSE
R1	26	RESISTOR, 1/20W 1% 0201 SMD, 0.0 OHM	0.0	CRCW02010000Z0ED	VISHAY DALE
R27	8	RESISTOR, 1/20W 1% 0201 SMD, 100 OHM	100	CRCW0201100RFNED	VISHAY DALE
R35	2	RESISTOR, 1/16W 1% 0603 SMD, 49.9 OHM	49.9	CRCW060349R9FRT1	VISHAY DALE
R37	26	RESISTOR, 1/20W 1% 0201 SMD, 10K	10K	CRCW020110K0FNED	VISHAY DALE
R39	56	RESISTOR, 1/20W 1% 0201 SMD, 0.0 OHM	0.0	CRCW02010000Z0ED	VISHAY DALE

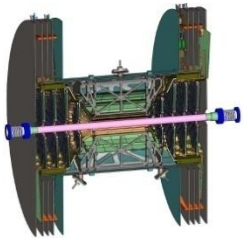
- All components except connectors on back side
- Connectors and HV caps now in hand for prototypes

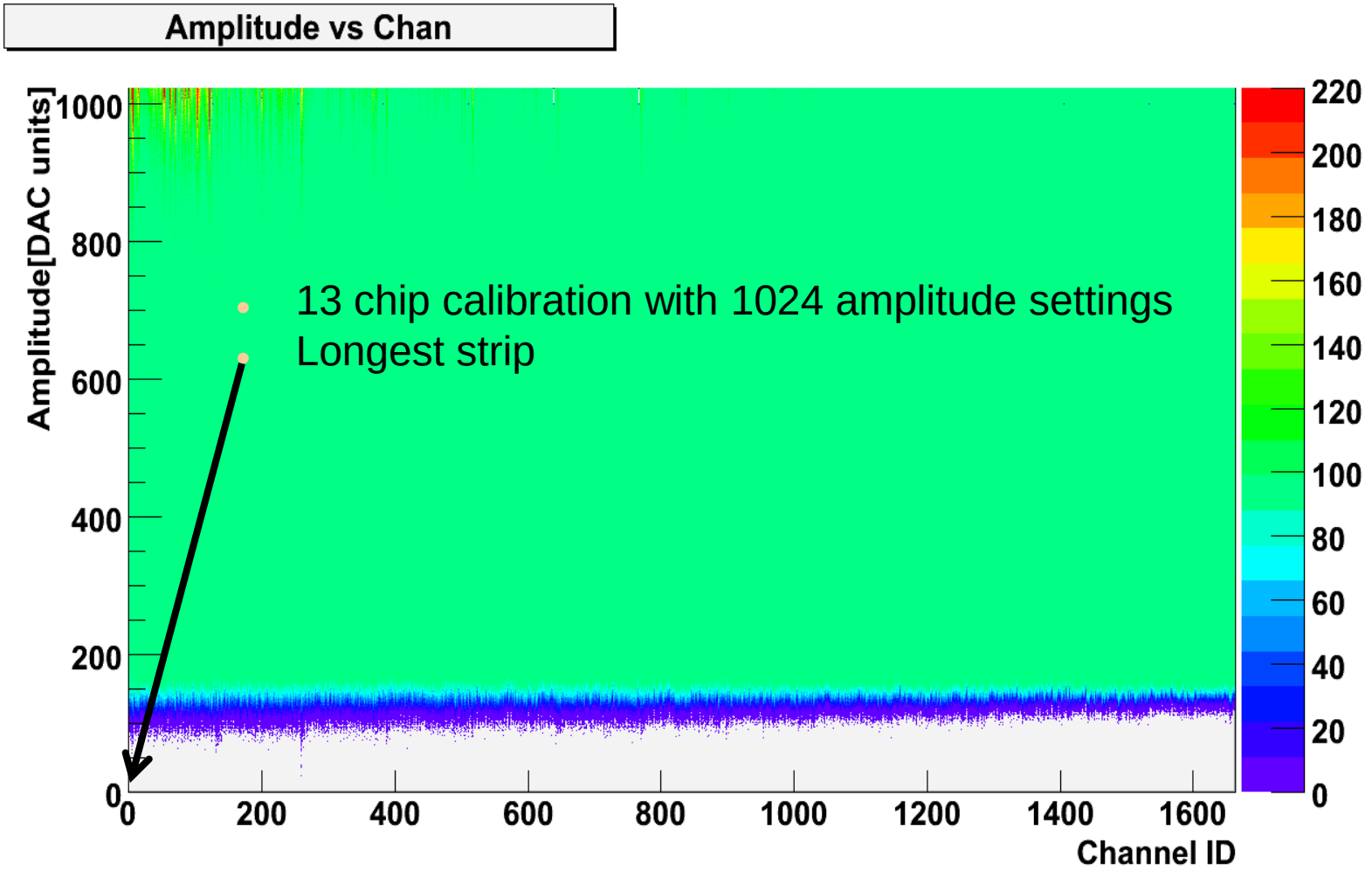
fVTX Prototype HDI Realization (PCB HDI also)



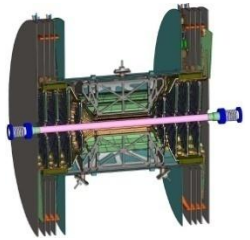


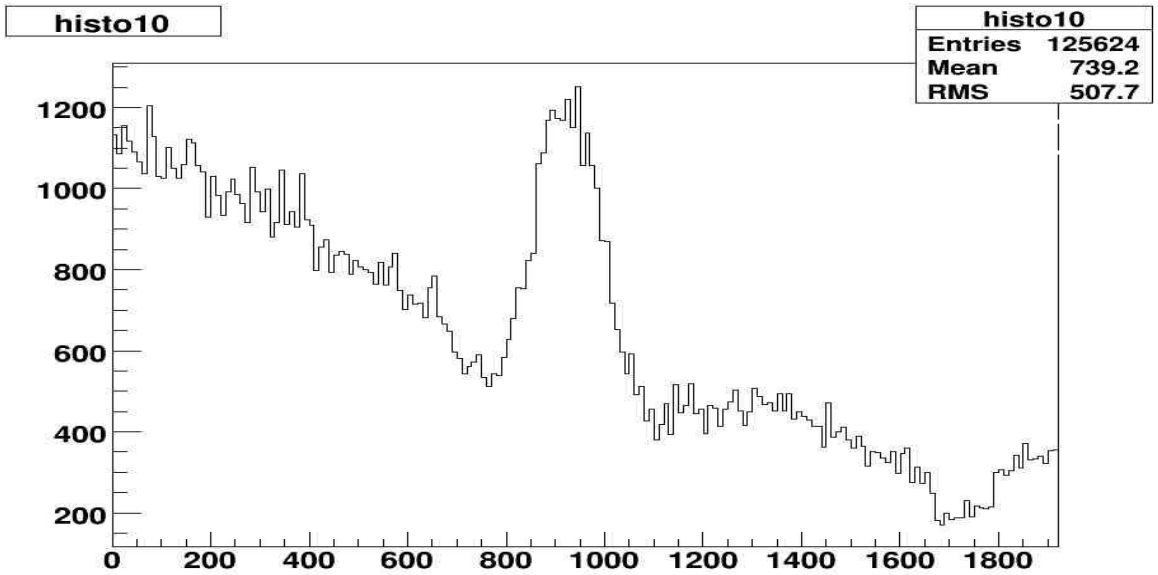
fVTX Prototype HDI Calibration





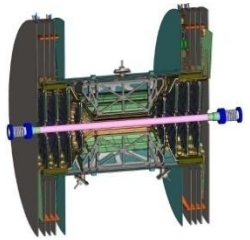
fVTX Prototype HDI
Data Taking with Source





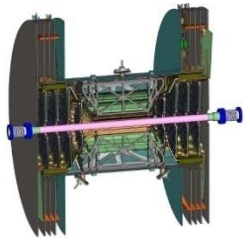
- In this mode we ran with
  - All the channels enabled
  - Threshold set to keep noise level reasonably small
  - Pulser is off
- Data taking runs in continuous triggerless fashion, every hit over the threshold is being outputted

fVTX Prototype HDI
HDI Stress Tests



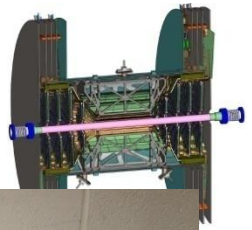
- Kapton HDI with 15 chips had been tested in calibration mode with following parameters
  - Beam clock was varied in a range of 4/5, 4.5/5, 5.5/5, 6/5 of the original
  - No problems at 4/5, 4.5/5 settings
  - One data line is lost at 5.5/5 = 11.11 MHz
  - Swamped with data at 6/5 = 12 MHz
- This means that HDI design has at least 10% safety factor in terms of the read clock frequency (ROC FPGA design may already be a limiting factor in this case)

fVTX Prototype HDI
HDI Stress Tests cont'd

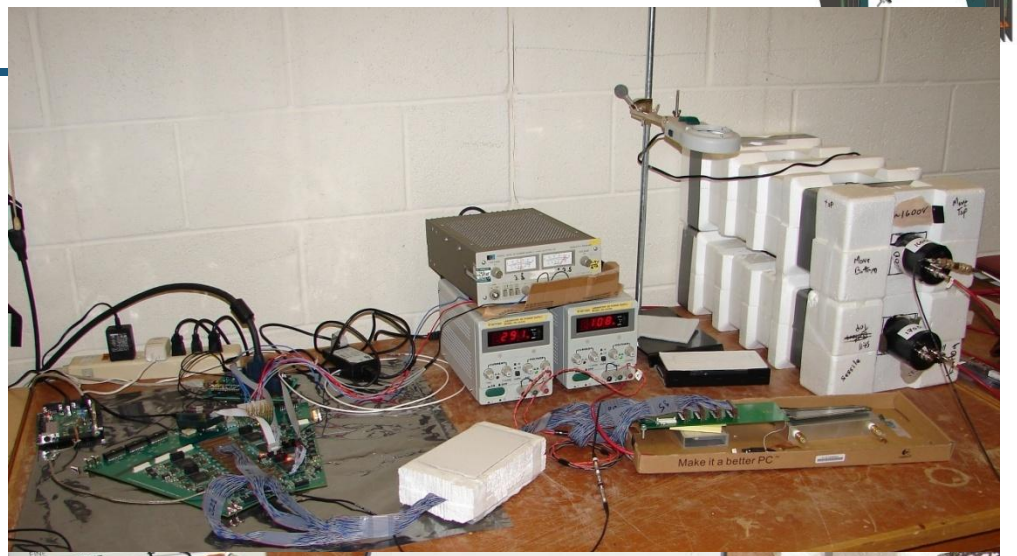


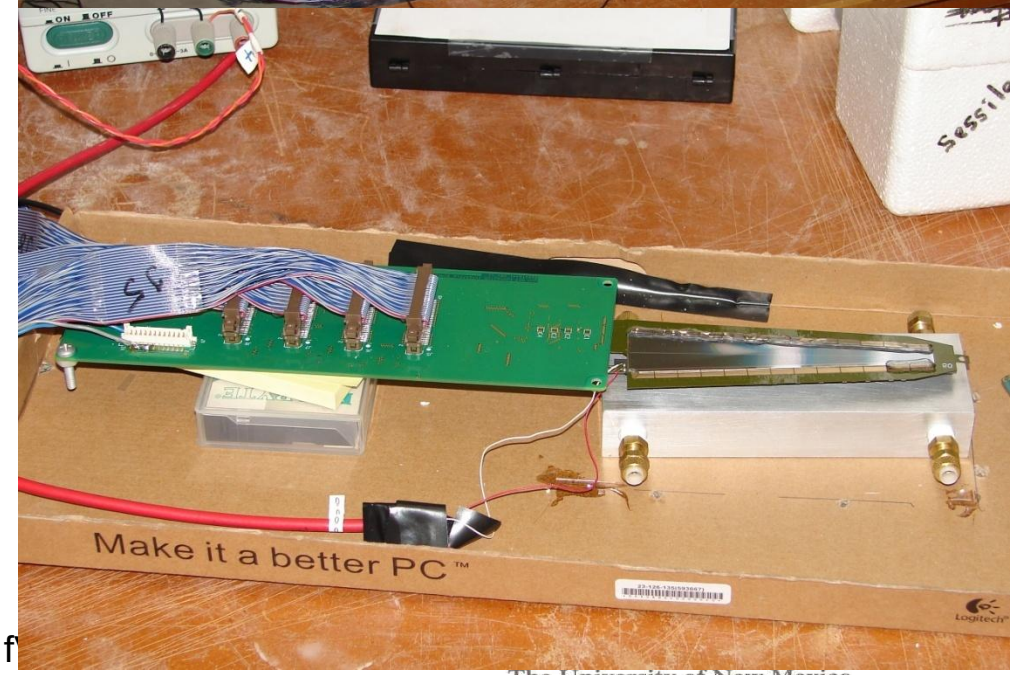
- Additional tests included
  - Checking the edge of the Reset w.r.t the BCO clock edge (need to be issued on rising edge)
  - Checking the effect of the phase of the read clock w.r.t the beam clock (found no effect)
  - Check the response to the long pulse train with the predefined spacing (1,000,000,002(4) hits from every chip for 1 Mil pulses issued)
- Collected a lot of data with Sr^{90} source as well as cosmic muons

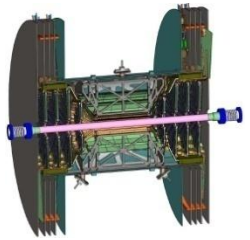
fVTX Prototype HDI
HDI Tests Bench



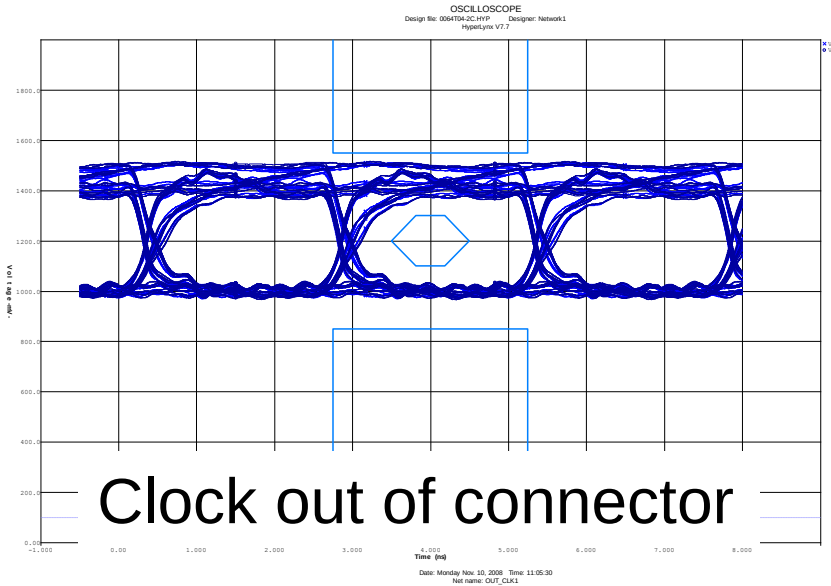
- HDI + Sensor + FPHX chips (15) tested with PCB interconnect and iFVTX ROC.
- No particularly great care taken to shield from noise, etc.
- Are currently working to implement a trigger for cosmics using scintillators and PMTs.



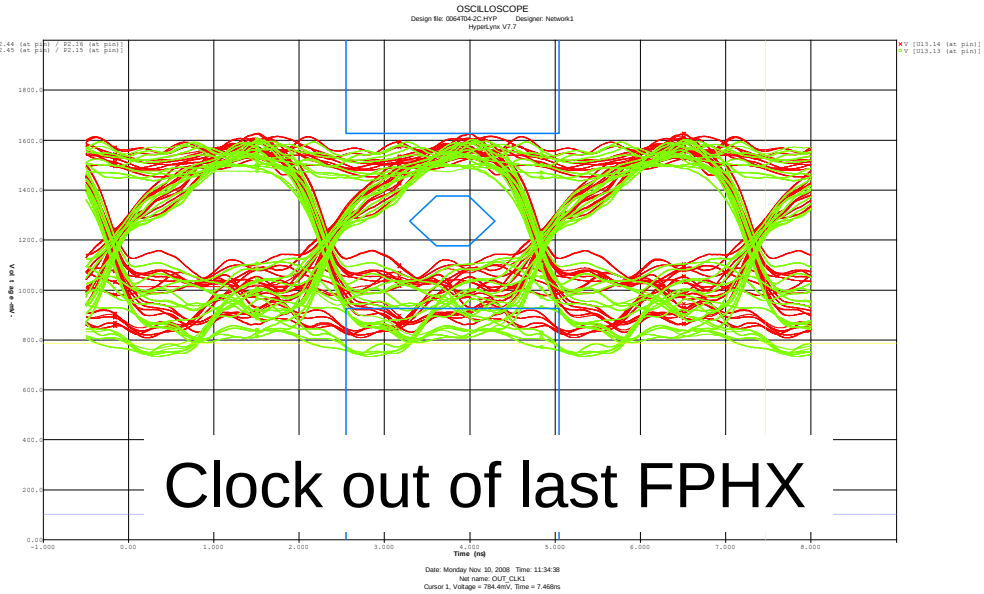




fVTX Prototype HDI
Simulations of Clock Integrity

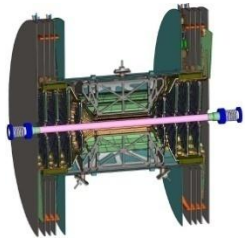


Clock out of connector

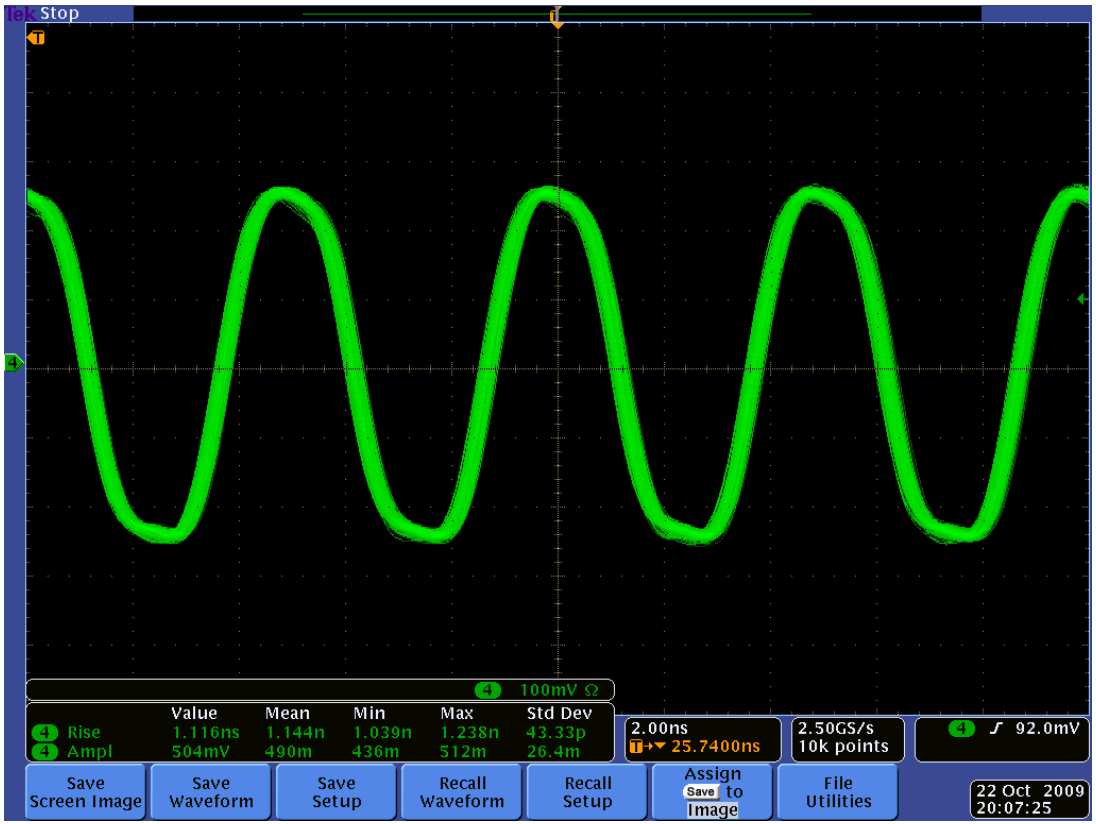


Clock out of last FPHX

- Clock signal Integrity is adequate
- More sophisticated termination of multi-drop clock line may improve performance due to reflections
- Specification of clock entering wedge important to achieving performance
- Via change on HDI had significant effect

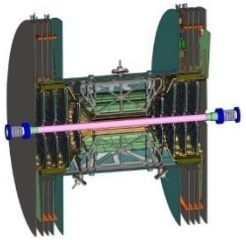


fVTX Prototype HDI
Measurements of Clock Integrity



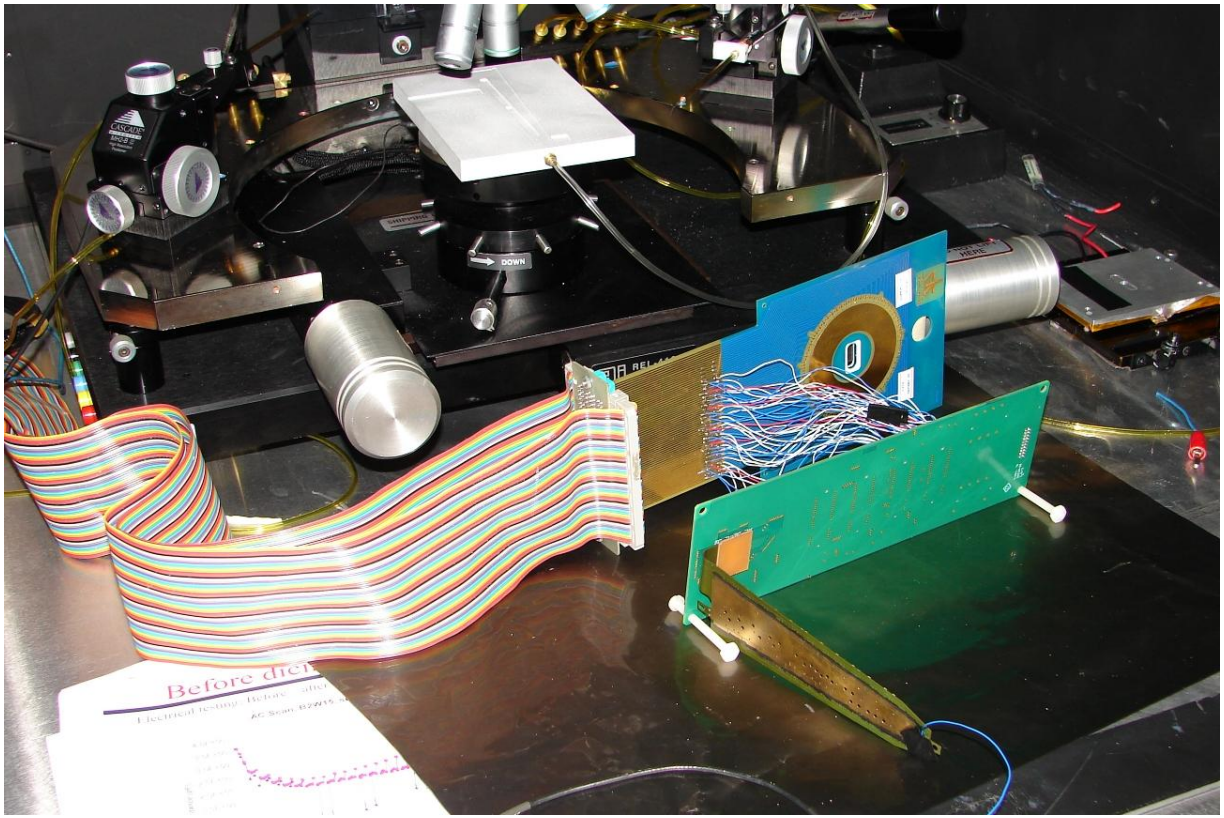
200MHz Clock out of last FPHX
450mV out of 700mV

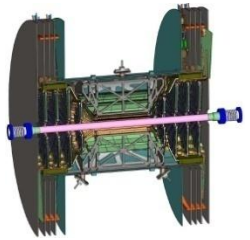
- Clock signal Integrity is adequate



fVTX Prototype HDI Bend Testing

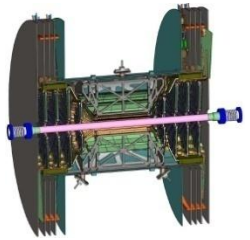
- HDI bent with a jig, heated with a hot-air gun. Temperature and duration of heating not well specified.
- Tested by connecting all wire-bond pads (with graphite) and putting some potential on them.
- Then connected to an automatic switch controlled by LabView





fVTX Prototype HDI
Initial Manufacturability Concerns

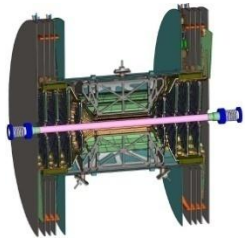
- Via diameters were initial specified at 50 microns with 150 micron pads
    - Because the boards became thicker, vias had to be increased to 70 microns with 200 micron pads.
- Some concern about the coverlay between adjacent pads on top surface (especially between connector pads))
    - No coverlay needed between pads
- Generally, the design is pushing the technology a bit, but within reasonable proximity to production capabilities.
    - Might have an impact on yield.



fVTX Prototype HDI
Initial Manufacturability Concerns

- Bend radius
  - With thicker HDI, bend radius may have to increase, or bend may have to be done by vendor)
- Heat transfer
  - With thicker HDI, we will need to test heat transfer from FPHX through the HDI to the cooling plate (carbon backplane).
- Clock integrity
  - Initial simulations showed marginal performance of the clock signals to the far end of the HDI, however, this assumed a 30cm interconnect with the same impedance/resistance as the HDI. This can be improved.

fVTX Prototype HDI
Post Manufacturability Concerns



Kapton HDI Design Changes

✓Change FPHX-->HDI bond pattern to match latest FPHX design bond pattern, and make associated schematics changes.

✓Need bond pads for sensor bias ring.

✓ChipID should be numbered 1-13 on each side rather than 1-26 for module.

xShould revisit usage of vias in design, possibly other ways to improve manufacturability.

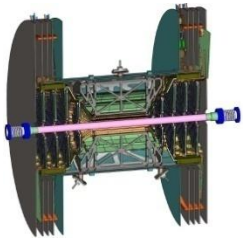
xAny design changes to help heat dissipation?

✓Need screw hole at bottom of HDI .

xShould round edges around bottom tab.

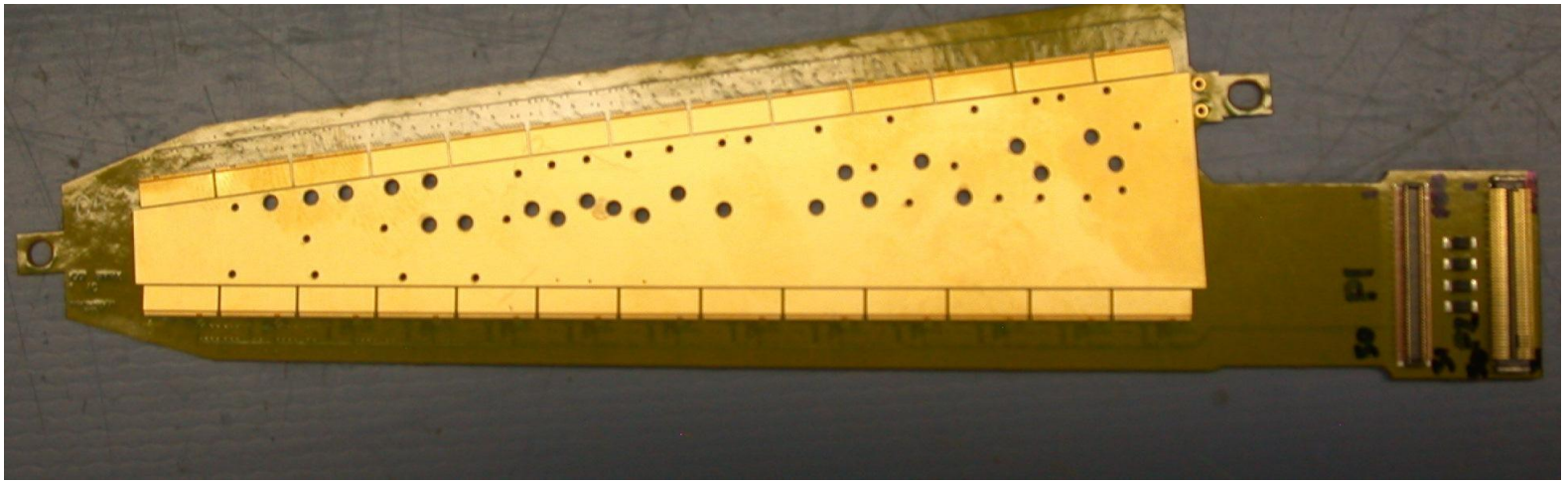
✓Different scheme for bias connection.

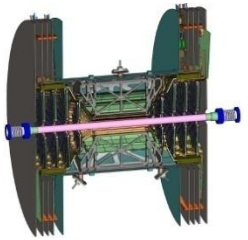
✓Holes in middle of HDI!



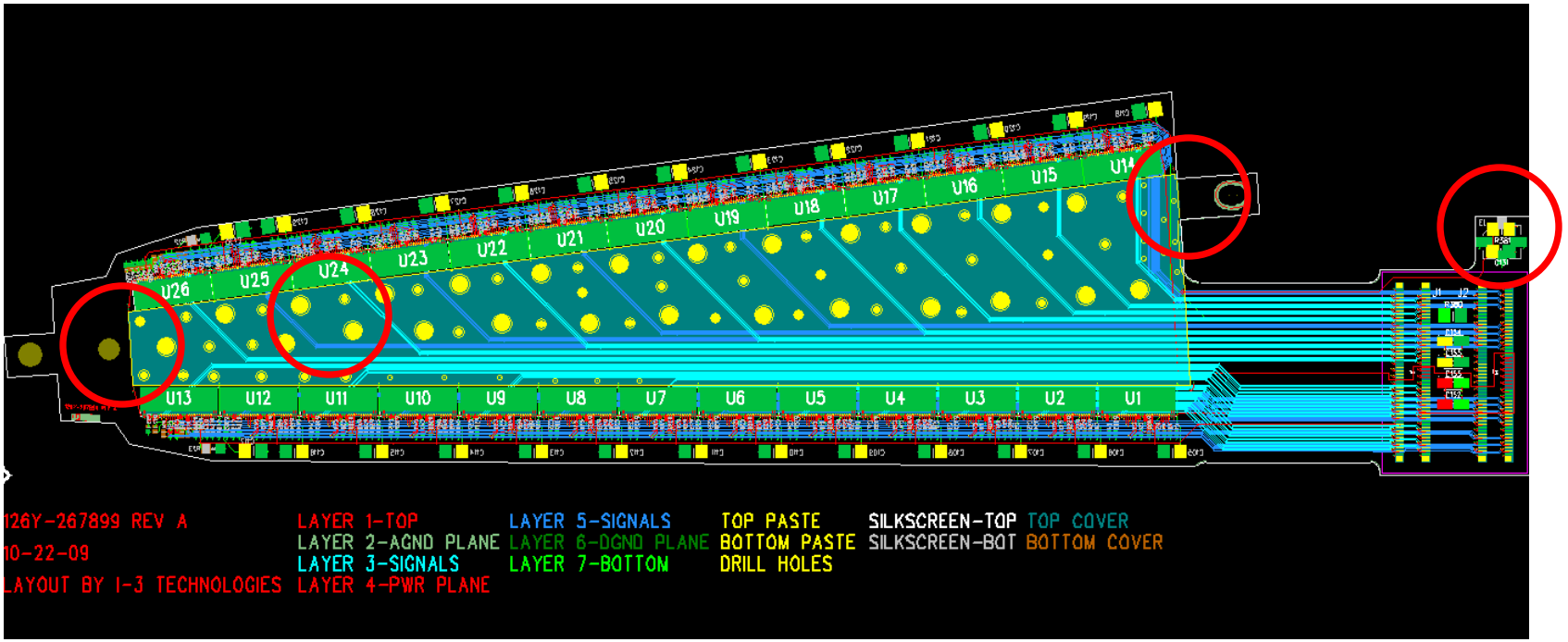
fVTX HDI
Prototype Post Manufacturability Concerns

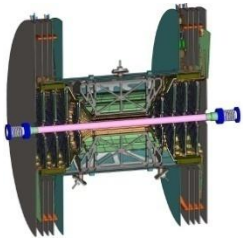
- Holes in middle of HDI!
  - Were told that these were to vent trapped gases.
  - Had no pull back from bias and ground planes!
  - Created shorts between power, bias and ground planes
  - Only could get bias on one HDI…



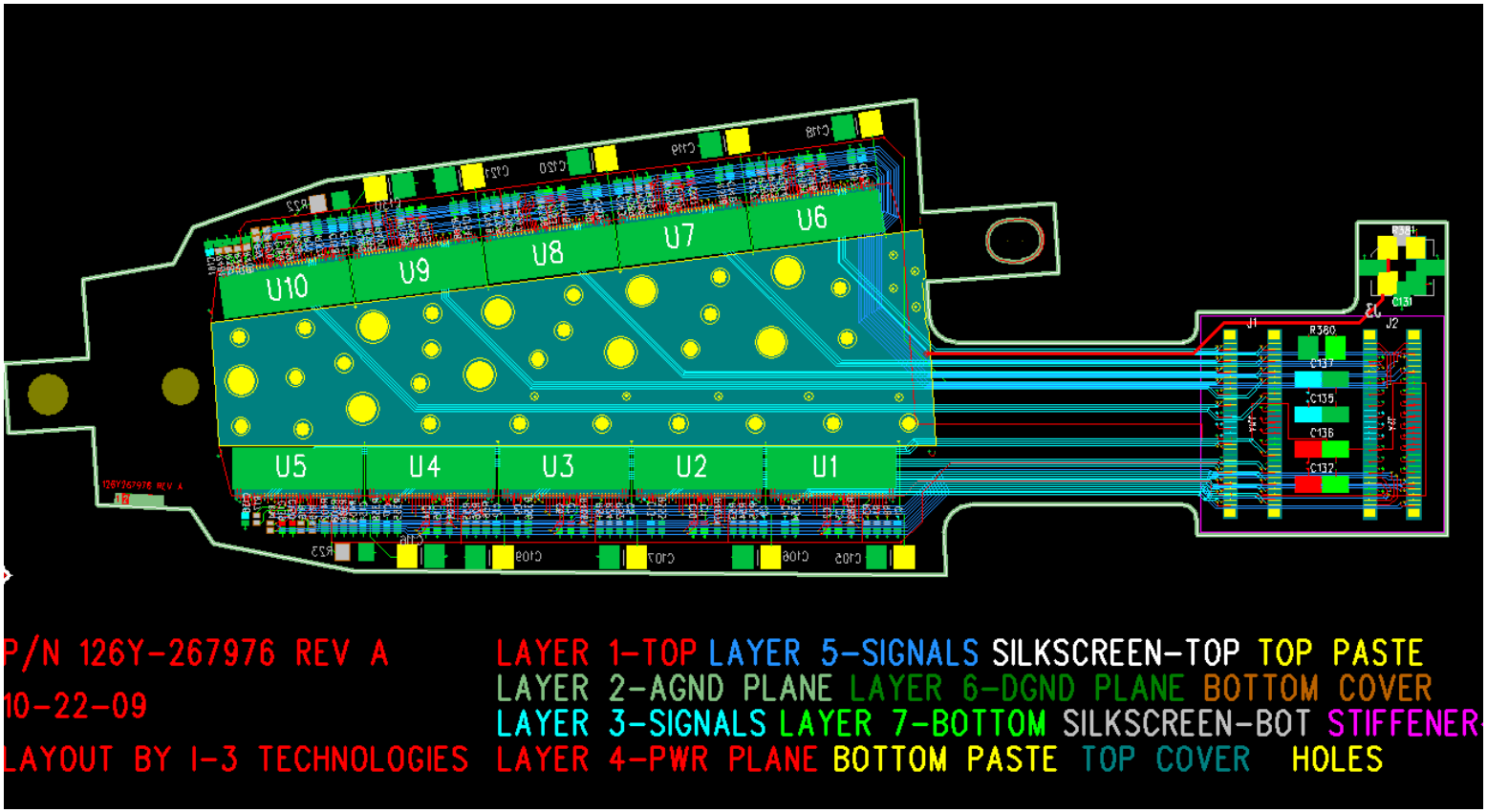


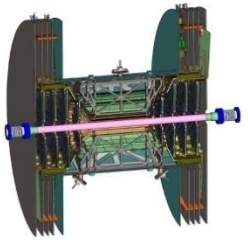
fVTX Production HDI Design





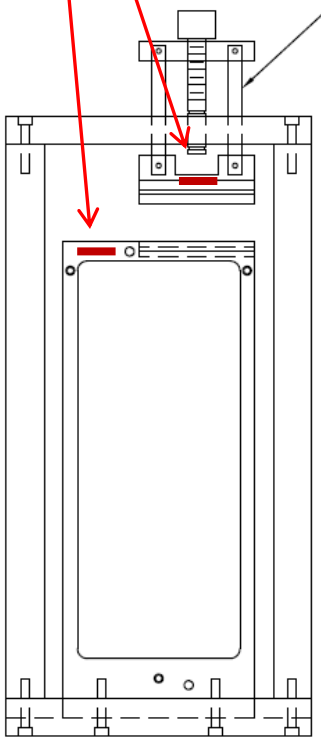
fVTX HDI
Production Design



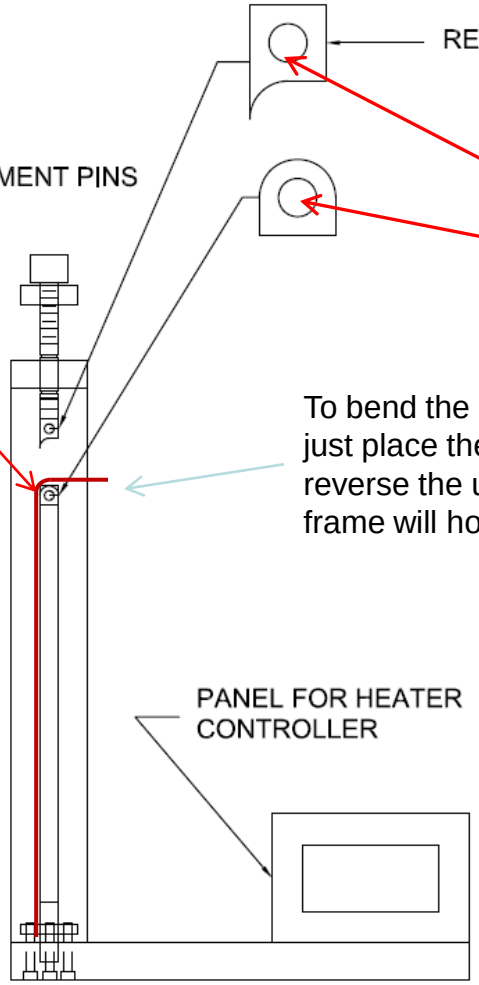


fVTX Prototype HDI
New HDI Bending Jig and Heating System

Thermocouples



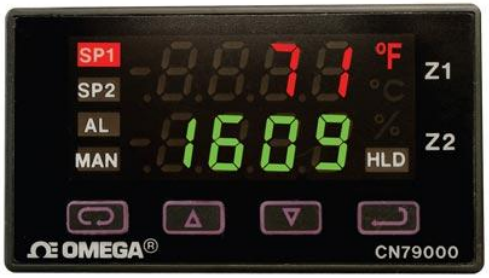
HDI will be held in place with a rectangular frame (not shown). Its open from both sides so that the components stay cooler with air circulation.



To bend the HDI in other directions, we just place the HDI on this side, and reverse the upper heater. The same frame will hold the HDI on this side.

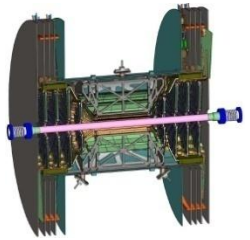
Cartridge Heaters
1/8" x 1.5"

Dual-Zone Controller



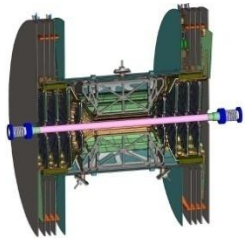
PHOENIX

The University of New Mexico



QA HDI

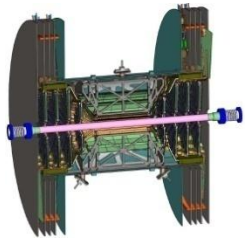
- Manufacturer inspection
  - Complete (bare-board) electrical test
  - Visual inspection after SMT placement
- UNM inspection
  - Look for shorts and opens after SMT placement (some rework is possible)
  - Inspect bond pad quality
  - Alignment fiducial metrology
- Electronic tests
  - Continuity
  - LCR response
- Bench test facilities exist at UNM, Columbia and LANL
- Tests will be performed by technicians and students with oversight by UNM



HDI design, production and testing

- 1.4.3.1 HDI design, preliminary design complete UNM
- 1.4.3.1 HDI (small version) design (Jan. ‘09)
- 1.4.3.2 .1 Procure prototype HDI (Under way)
- 1.4.3.2.2 Test prototypes (Jan. – Sep. ‘09)
- 1.4.3.2.3 Redesign (Oct. ’09)
- 1.4.3.2.4 Procure second prototype (Jan. ’10)
- 1.4.3.2.5 Test second prototype (Jan. – Feb. ‘10)
- 1.4.4 HDI-ROC interconnect design (begin Oct. ‘09)

- 1.4.3.3.1 Procure production run (Feb. ‘10)
- 1.4.3.3.2 Test production HDI (Jan. ‘10 -)



Summary

- First prototype design, testing and re-design is complete.
- The design has been demonstrated to work.
- Schedule for HDI production has slipped, but no technical roadblocks.
- Will soon have “first article” in hand as a second prototype, can test quickly and procure remaining production quantity quickly.