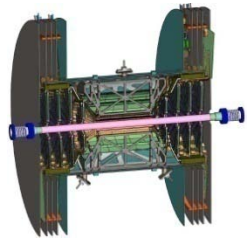
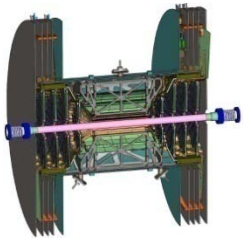


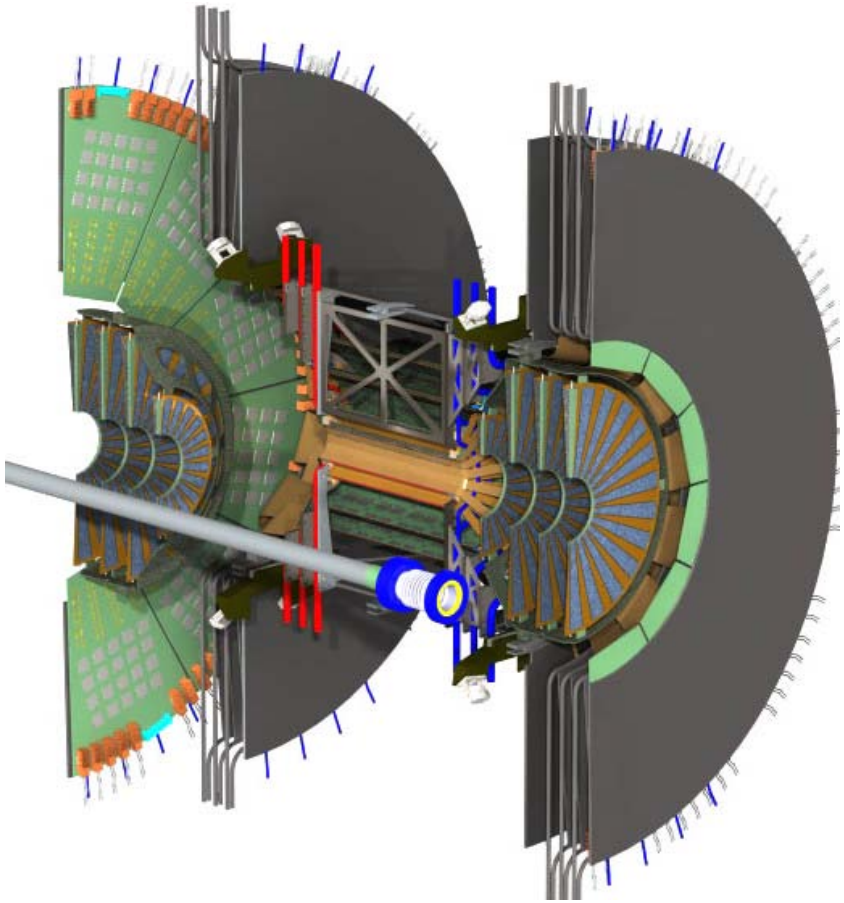
FVTX Electronics

(WBS 1.5.2, 1.5.3)

Sergey Butsyk
University of New Mexico

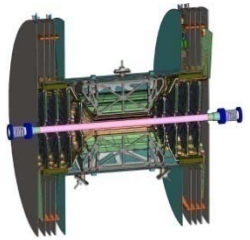
Introduction Comments



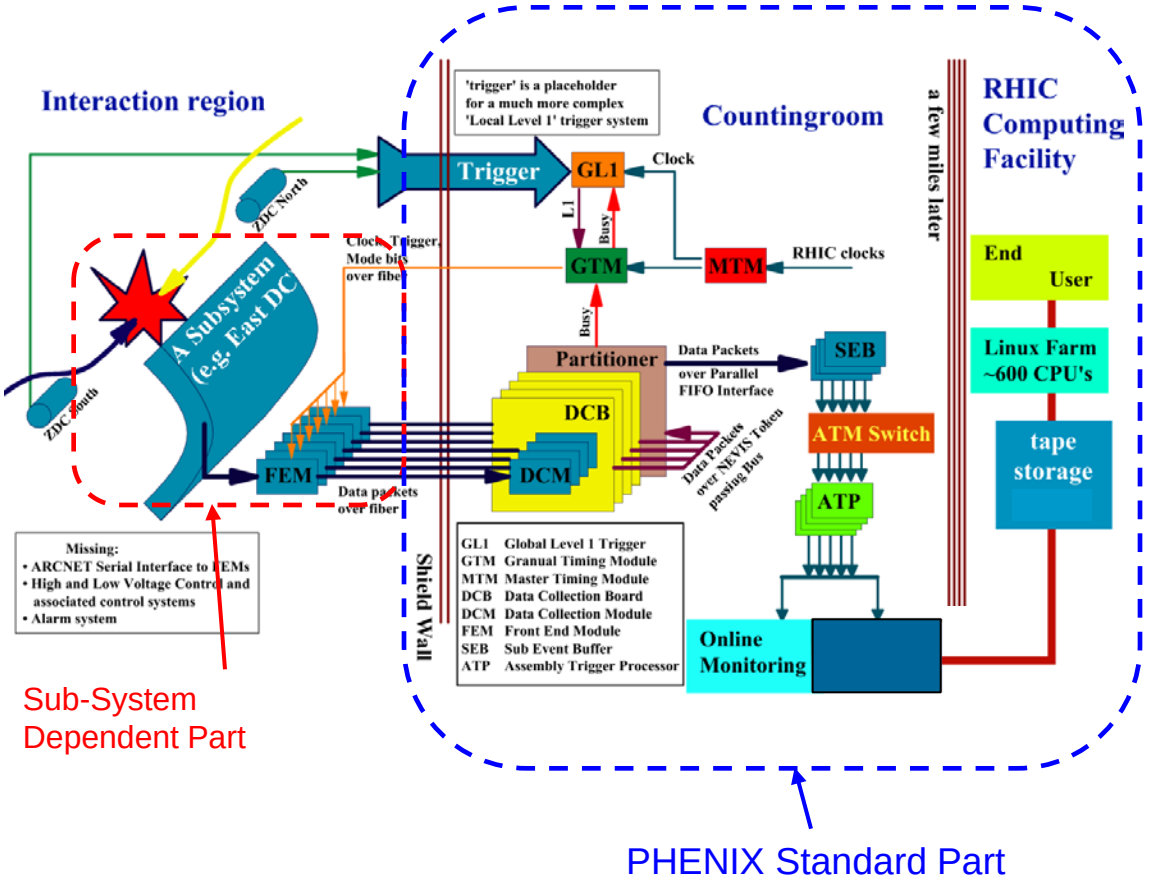


- **FVTX detector**
  - Over 1 Mil strip channels
  - “Data push” architecture (hit is sent out of the FPHX chip any time it was created)
- **PHENIX DAQ standards**
  - Triggered readout interface (data sampled, digitized and shipped out only when Level1 trigger request arrives)
- **FVTX DAQ should be able to bridge the gap between two different readout concepts and integrate FVTX detector into PHENIX DAQ environments**

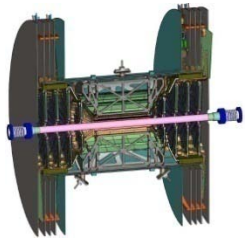
PHENIX Data Aquisition

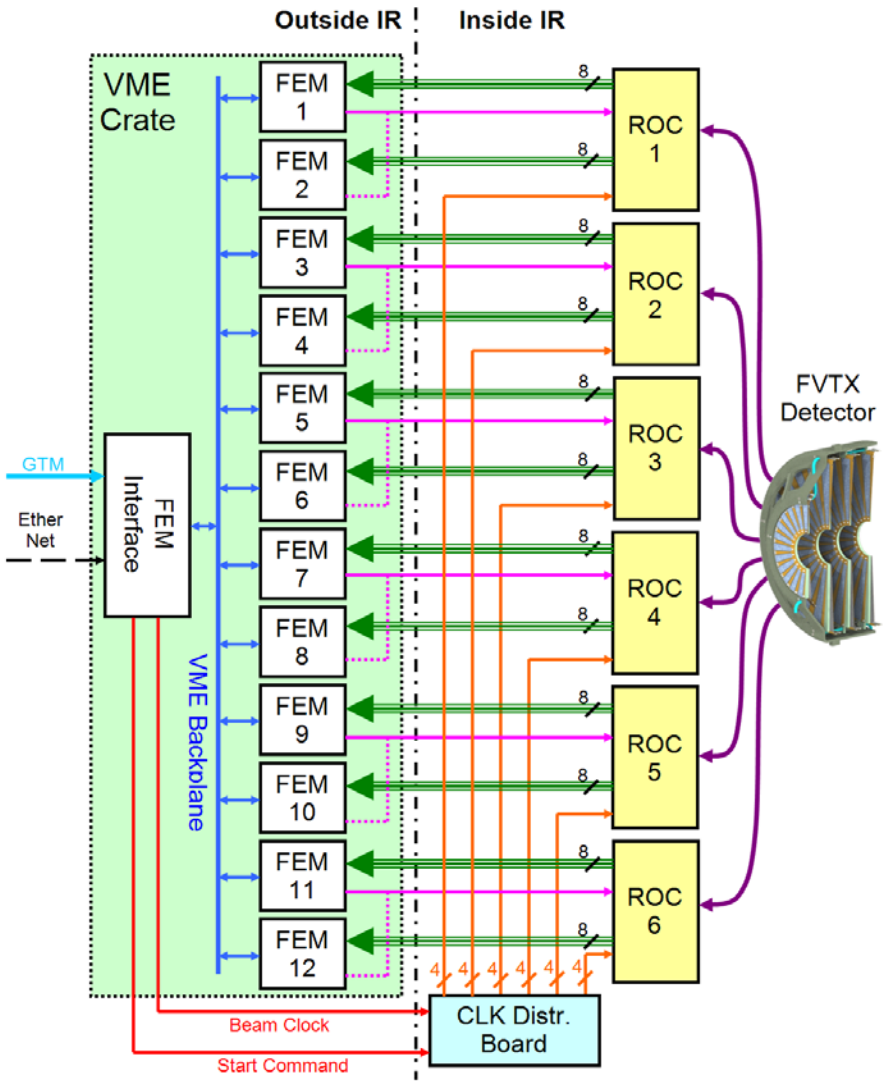


- RHIC beam clock ~ 9.4 MHz
- Data buffered by Front End Module (FEM) for 64 beam clocks
- LVL-1 Trigger issued with fixed delay w.r.t. collision
- FEM sends the data from the collision bucket to DCM in a data packet format
- Event is constructed from the packets, corresponding to the same event, by Event Builder



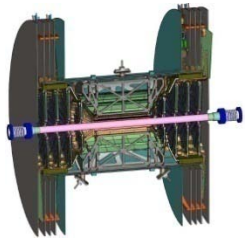
FVTX Readout Strategy





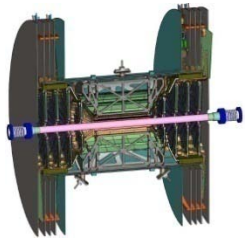
- ½ of each detector arm is read out independently
- 6 ROC cards collect and compress the data from the detector
- Each ROC send two 8 fiber output too two FEM boards in the Counting House
- Slow Control fiber send control data stream up/down the FEM↔ROC link
- Clock Distribution Board distribute Beam Clock and Start signals to individual ROC boards (the signals are sent over the optical fibers)

Important Accomplishments



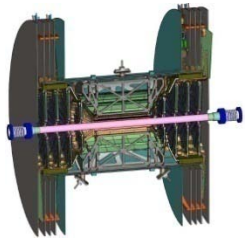
1. Doubled bandwidth of the link between ROC and FEM by doubling the number of fibers in the system and multiplexing data 2-to-1 on the input to FEM
2. Completed full timing simulation of ROC and FEM FPGA design in response to the limits of the current design
3. Successfully tested **all** the main parts of the ROC design on the LDRD funded ROC prototype board
4. Reliably run ROC board based DAQ in a realistic data acquisition mode ***for several days in a row without any hang ups***

Uncovered Problems



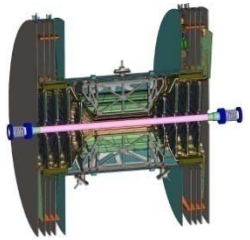
5. ROC 2nd and FEM 1st prototype development had been slipping down the schedule to the point that WBS 1.5.2 became very close to critical path

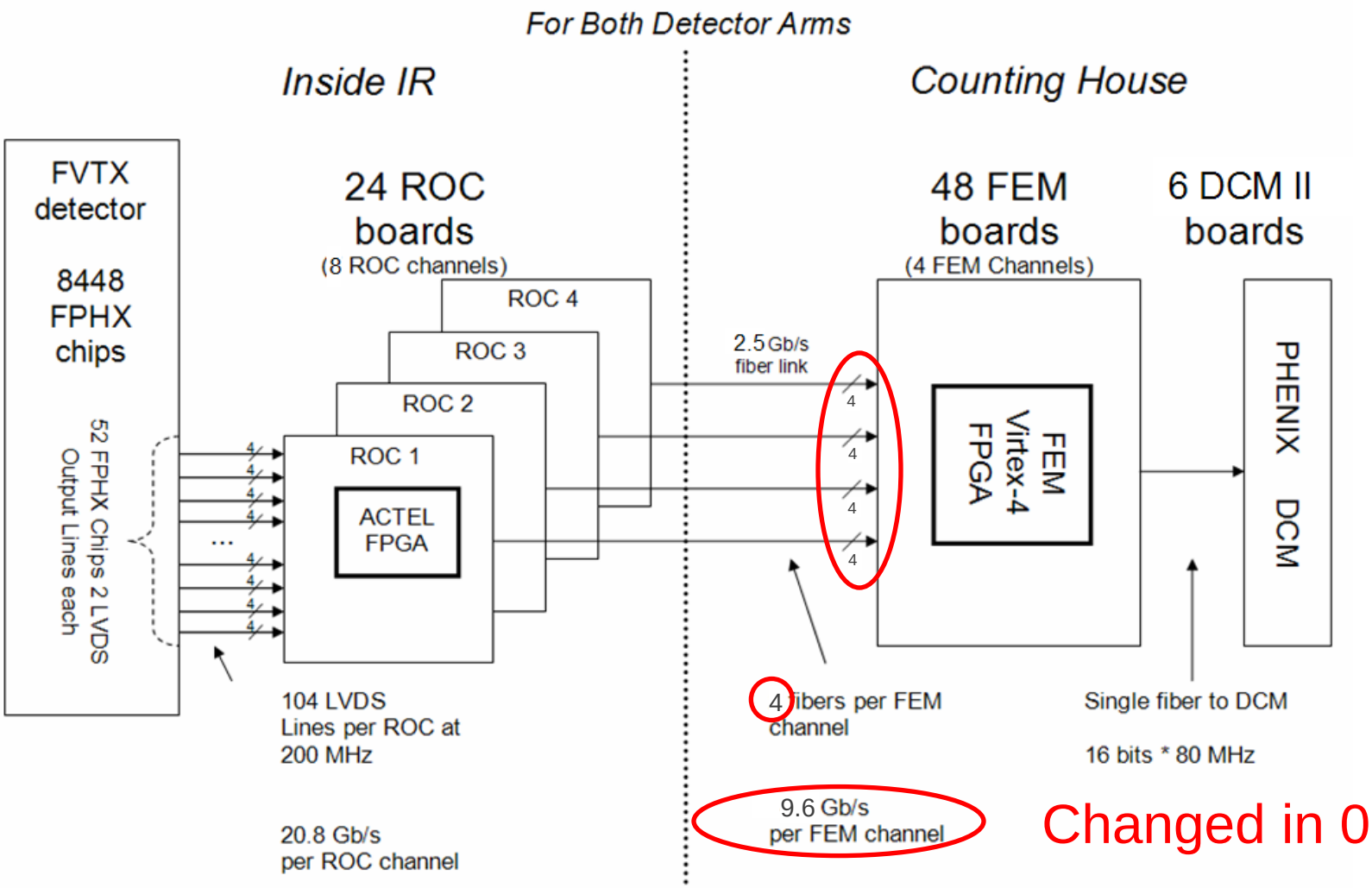
- **Reasoning:**
  - Lack of experienced ECAD designer availability
  - Increased complexity of the board design
- **Solutions:**
  - ECAD designer for the ROC 2nd prototype has been identified (same person who is currently working on FEM layout)
  - Procurement time for FEM and ROC can be reduced
- **Current situation:**
  - Proto-ROC(FEM) schematics - ready
  - Proto-FEM layout - will be ready by 12/01/09
  - 2nd Proto-ROC layout - started 11/01/09



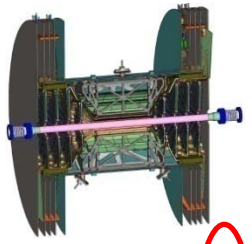
1. Doubling Fiber Optics bandwidth

FVTX Readout Diagram

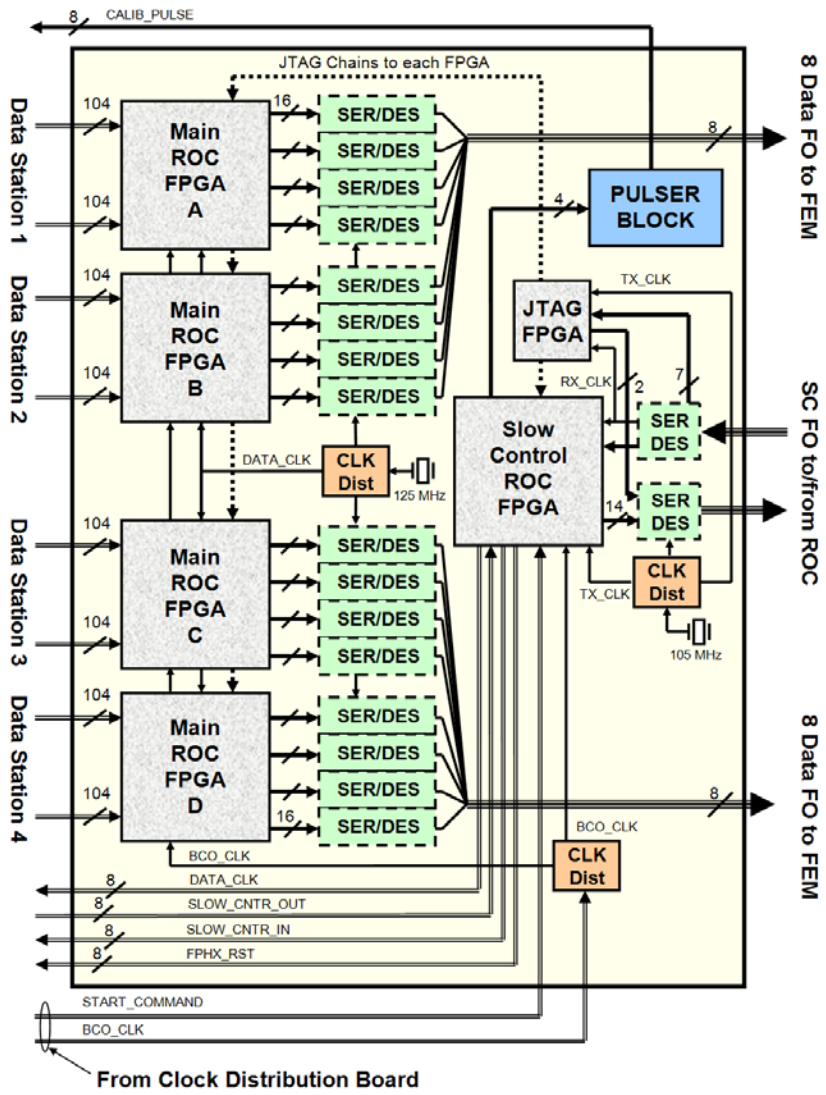


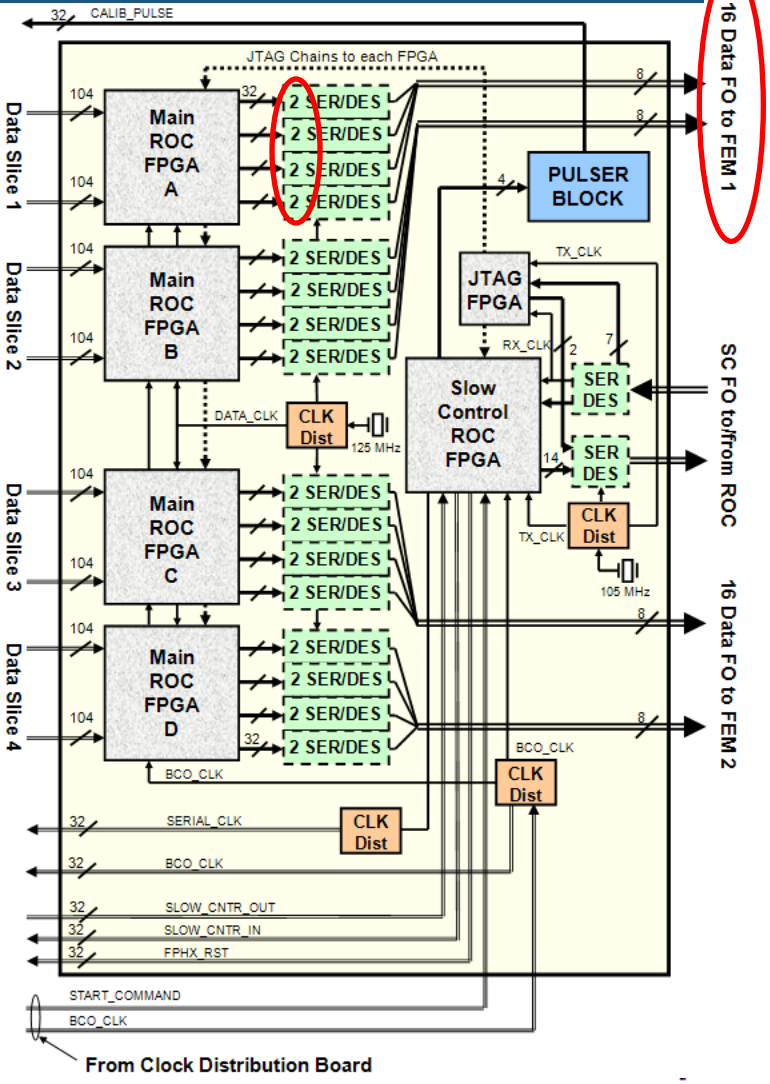


ROC Board Changes



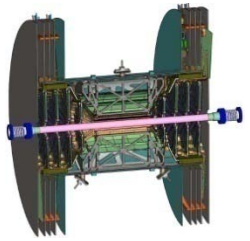
2009 Version

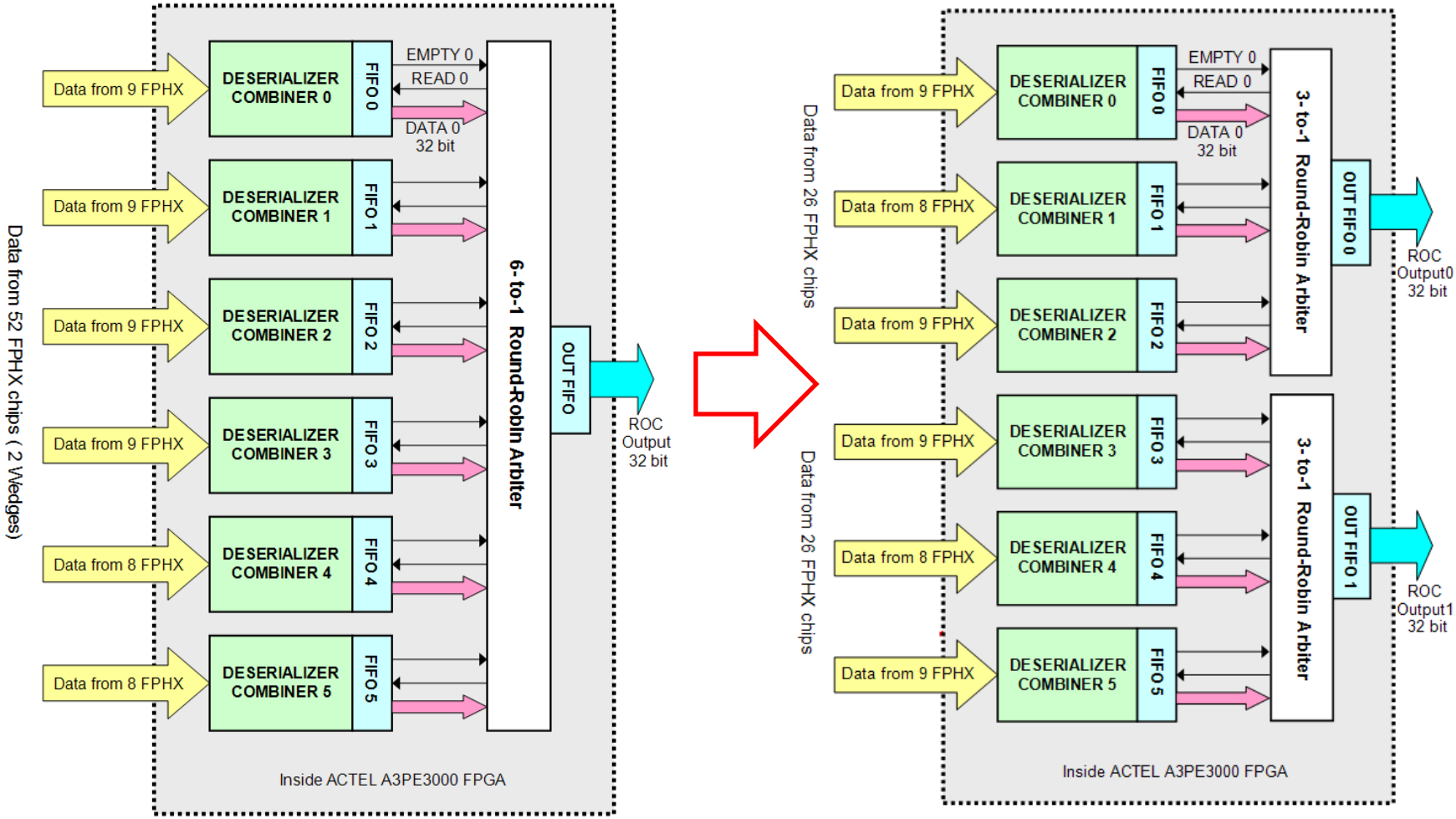




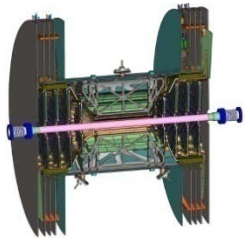
ROC Channel Changes

2009 Version





FPGA of Choice for ROC



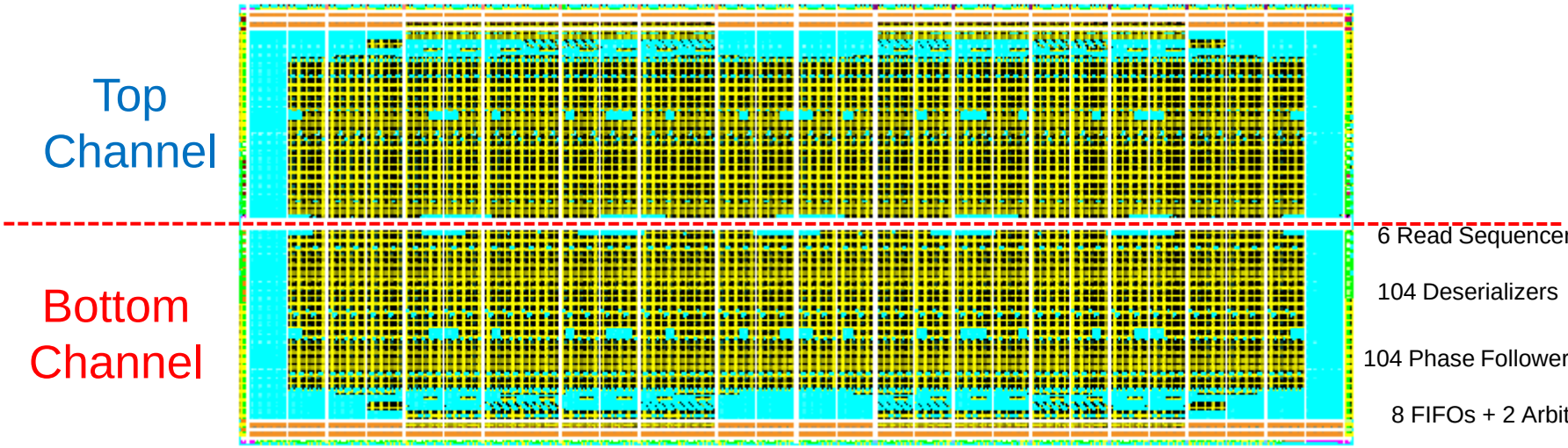
- ROC Design uses ACTEL ProASIC3E FLASH based FPGAs
  - Radiation tolerance to 200kRad integrated dose
  - Enough I/Os to implement 2 ROC channels on a single chip (need ~ 210 LVDS pairs + 64 LVCMOS outputs)
  - Low cost ~$250/chip
  - Well tested, reliable commercial technology

FAST !

Running at 200 MHz should be fine

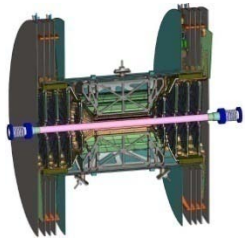
Clock Details:

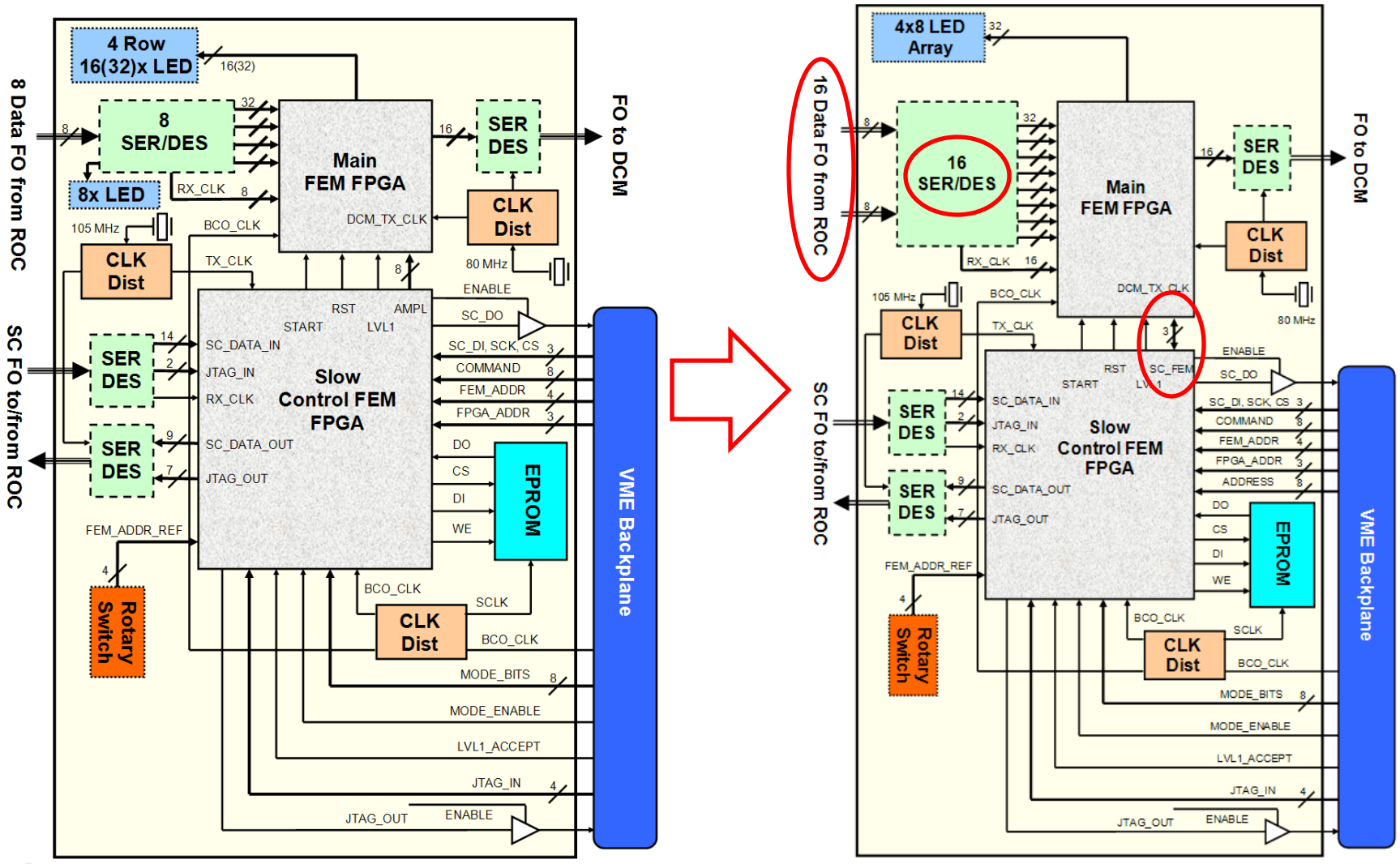
	Name	Period (ns)	Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)
	CLK	3.729	268.168	4.546	219.974
ⓘ	CLK90	0.712	1404.494	4.546	219.974



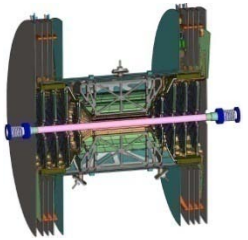
FEM Board Changes

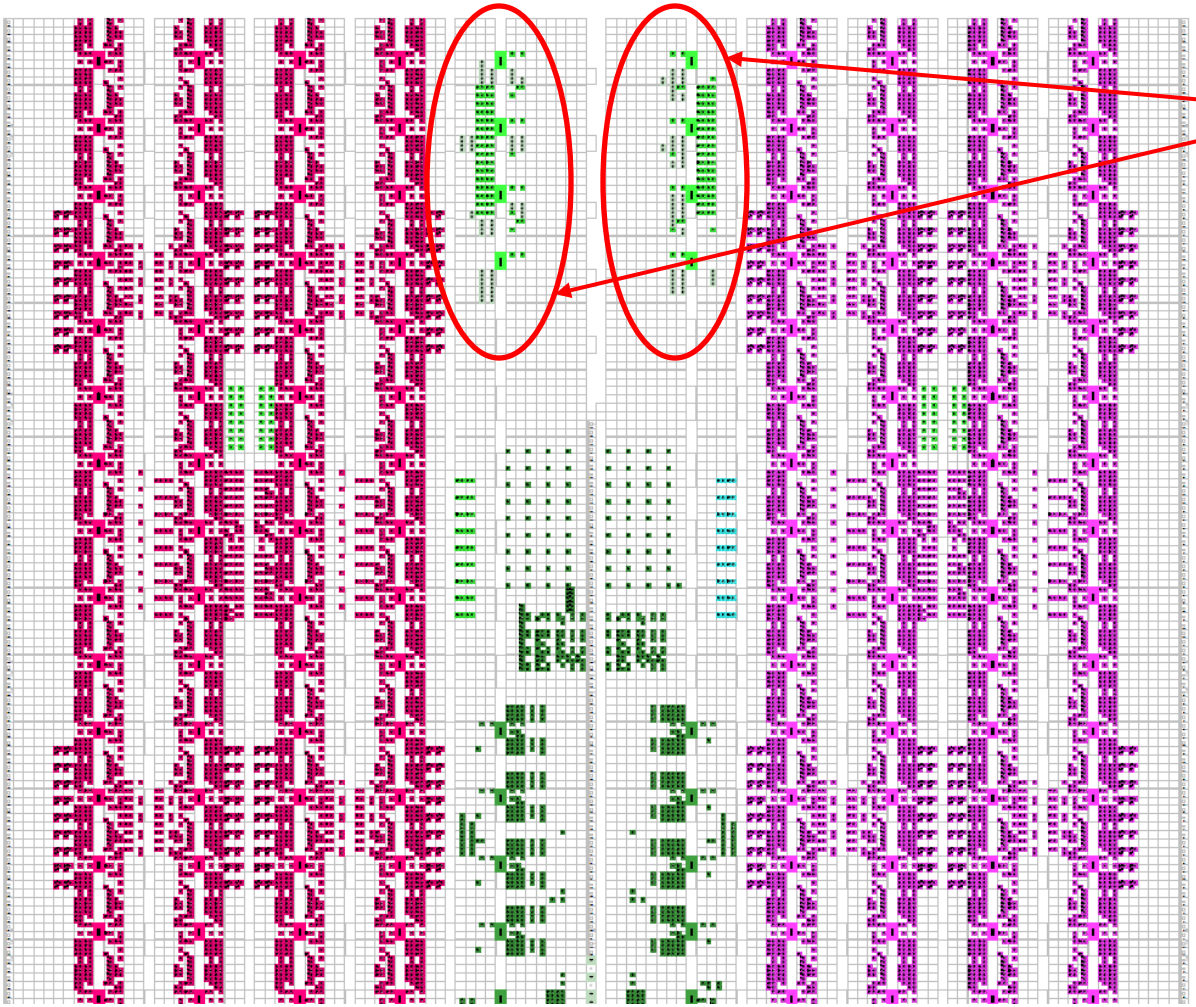
2009 Version





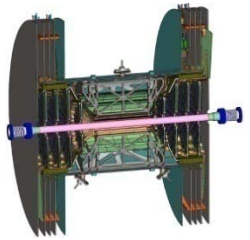
FEM Channel Changes

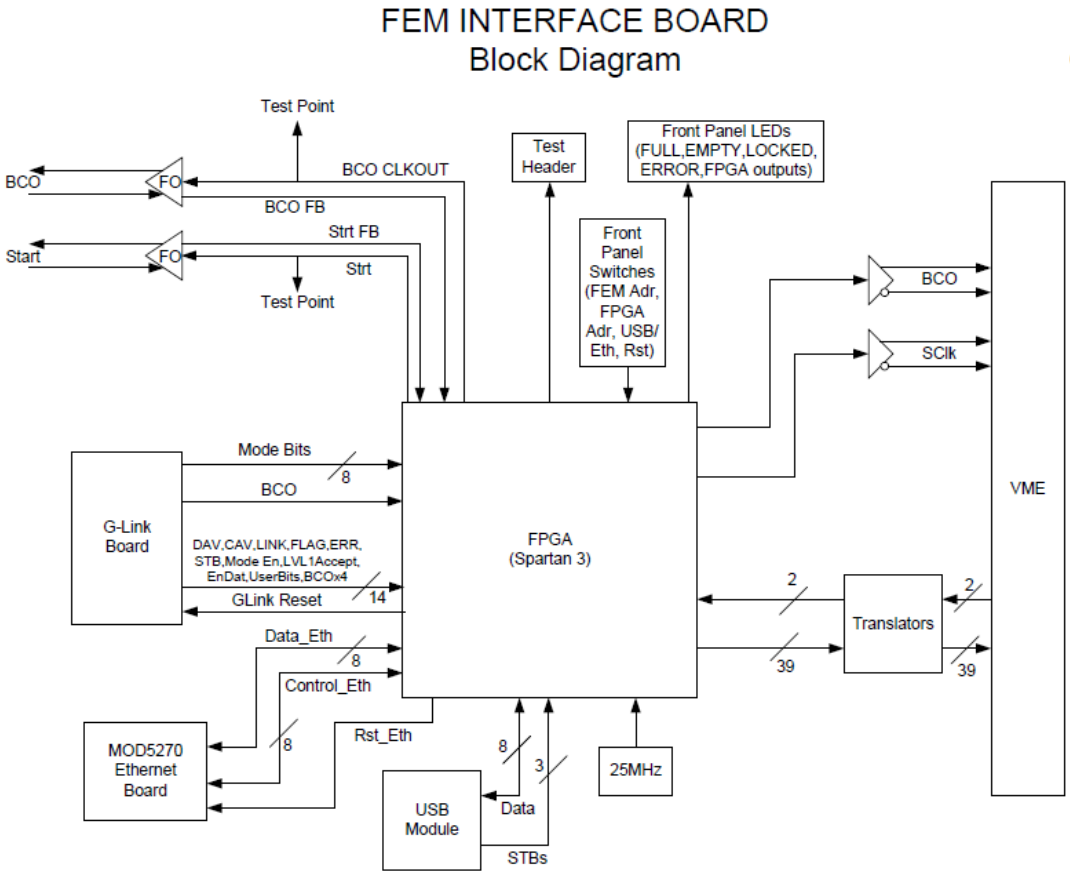




- Input Multiplexers added
- Design was speed up to run at 300 MHz both for writing and for reading
- 300 MHz > 125 MHz* 2 ➔ have enough time to multiplex two input streams

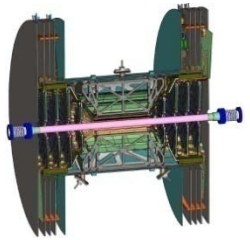
FEM Interface Board



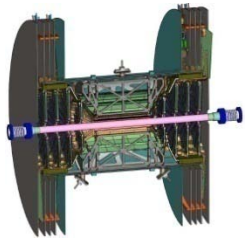


- 6/24/2009
- FEM interface board controls VME Crate with 12 FEM boards
- Receives Slow Control Data via Ethernet or USB
- Transmits the data to all FEM boards via VME backplane
- Slow Control Data running at ~12 MHz Clock

1. Main Conclusions

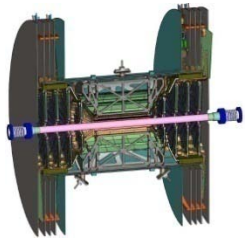


- Doubling Fiber Optics bandwidth between ROC and FEM board had been implemented in the design of the boards and in FPGA design
- The consequential speed up on the FEM code to operate entirely on 300 MHz clock lowers latencies on the design and makes clock distribution more uniform and simple
- The output buffer size on the ROC effectively doubled to two 256 deep FIFOs which lowers a chance of potential buffer overflow



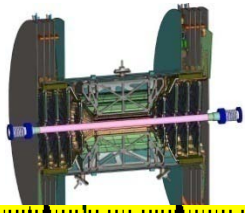
2. Worst Case Event VHDL Simulation

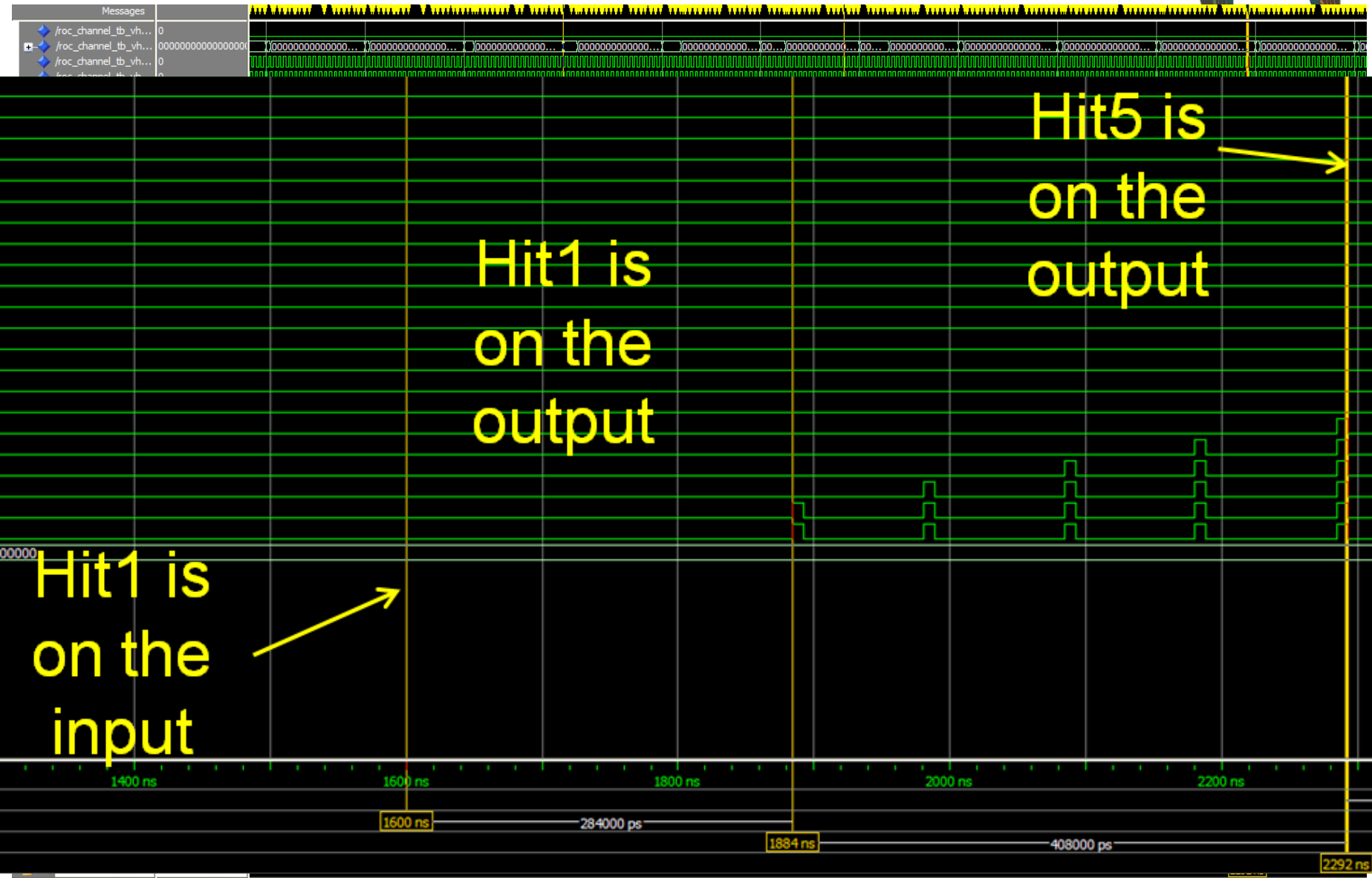
Idea of ROC Simulation



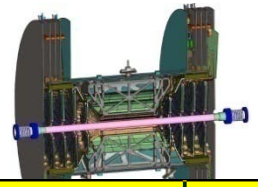
- FEM design provides a solid bottleneck of maximum 512 hits from a single BCO to be stored as one event
- This corresponds to ~10 hits/FPHX or 5 hits/output as FEM channel reads data from 52 chips
- The idea is to generate 5 hits/output on all of 52 chips and see the propagation through the ROC
- To make situation more interesting a phase advance of **50 ps** was introduced from channel to channel so the phase of the input signal to the serial clock had all the values it can possibly get (testing phase followers)

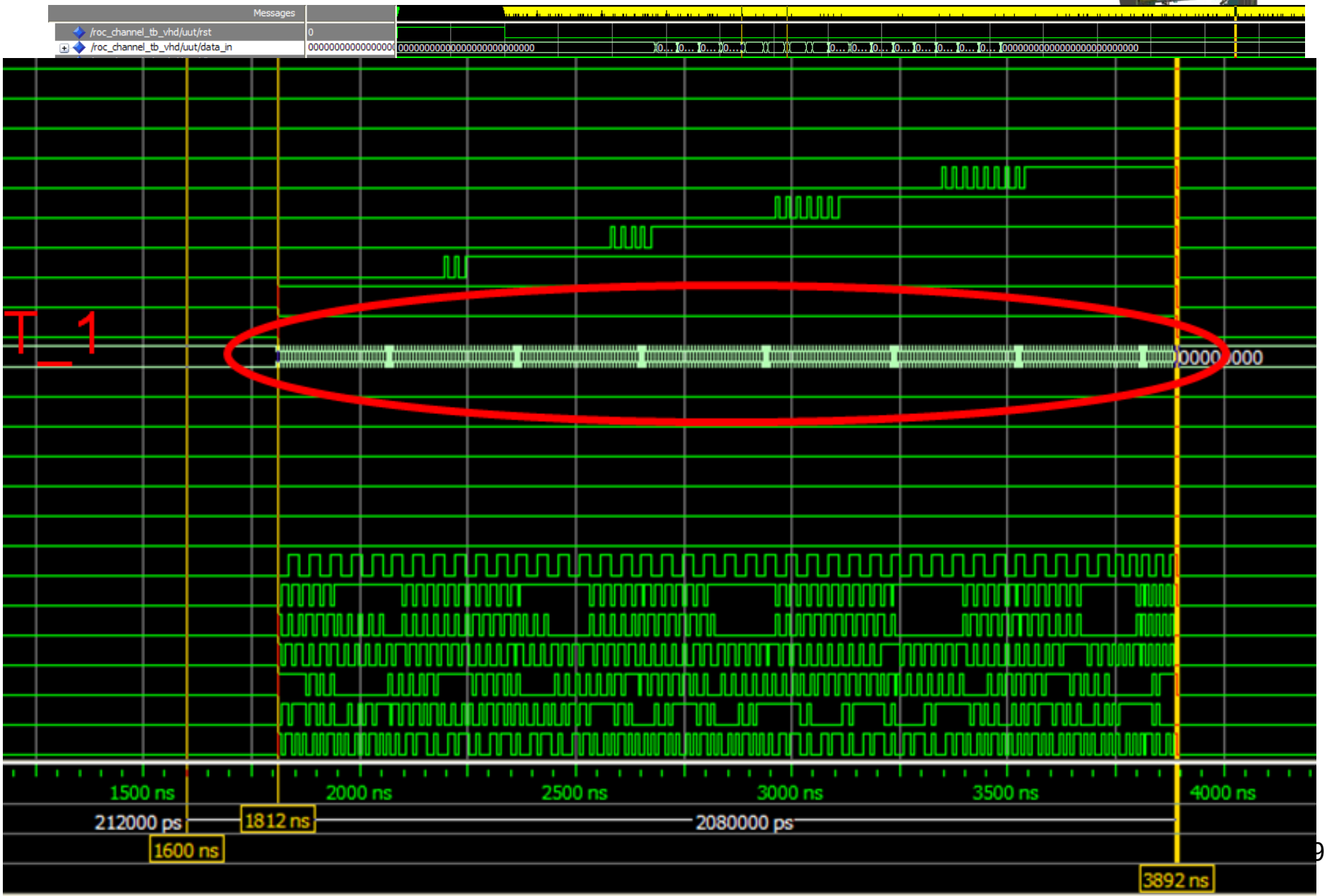
ROC Simulation Warm-up



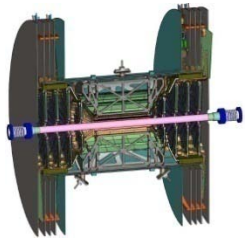


ROC Simulation





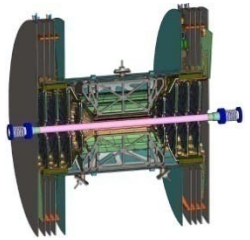
ROC is Not a Bottleneck



Even 10 hits/output can leave the ROC without problem

Output buffer is never full

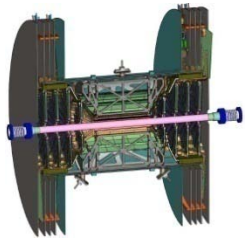
2. Main Conclusions for ROC



- There is 200 – 300 ns (2-3 beam clock) latency from the arrival of the last bit of the data word to the data output from the ROC
- It takes 408 ns to send 5 hits from one channel (no delay here, data just pass through the design)
- It takes 2080 ns (20 beam clocks) to send 10 hits from every chip. ***This is much less than PHENIX 64 clock buffering requirement***

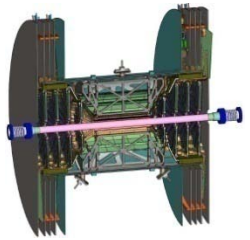
ROC design works in full timing simulation

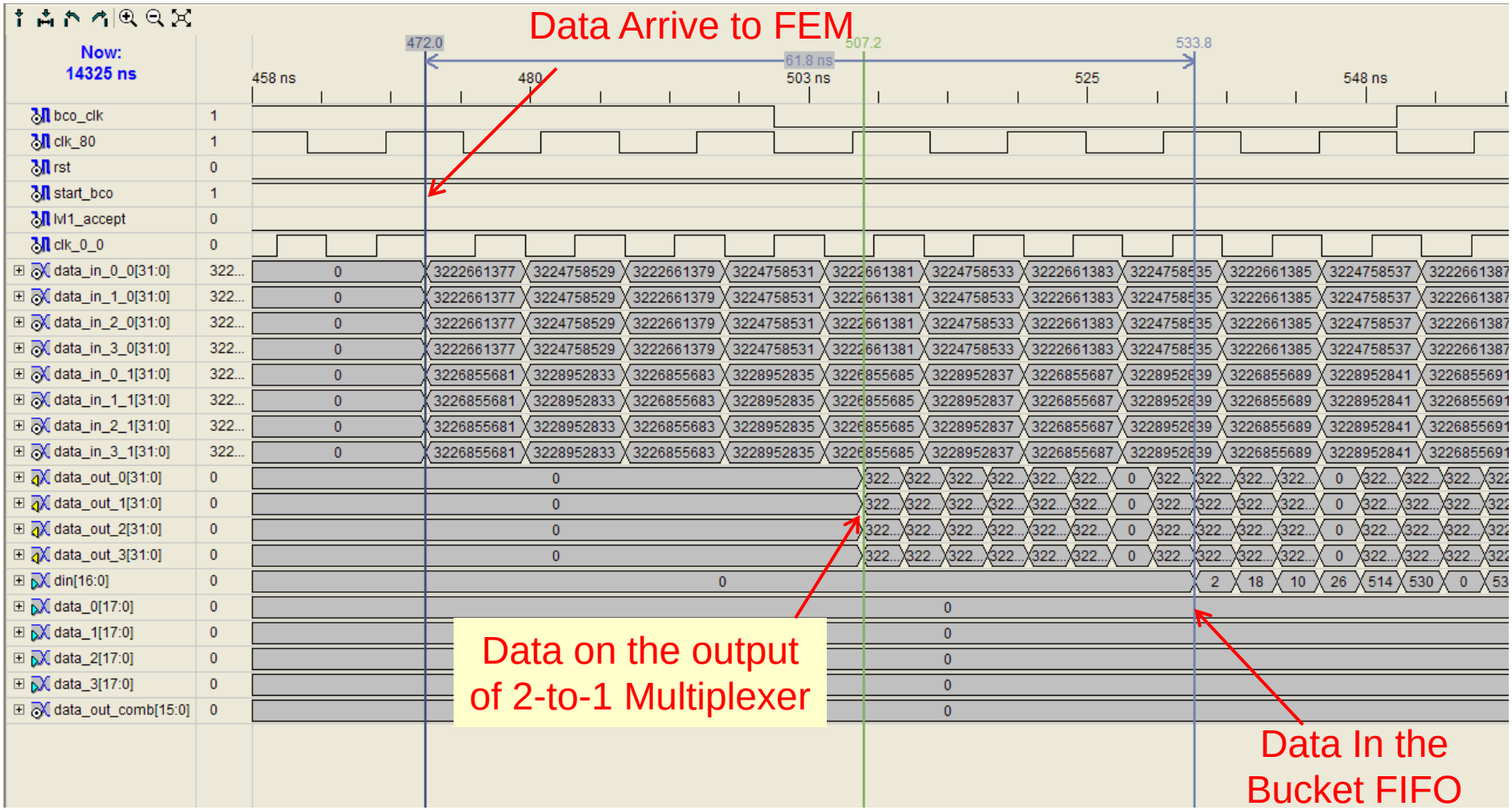
Idea of FEM Simulation



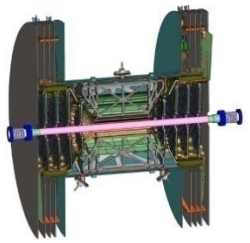
- FEM design provides a solid bottleneck of maximum 512 hits from a single BCO to be stored as one event
- Want to check how long it will take to combine 4 FEM channels that all receive 512 hits packet from the ROC
- This is potentially the largest event that need to be successfully assembled without raising error condition
- Writing into the bucket FIFO latency is important for writing
- Issue LVL1 Trigger at some point in time and study the latency w.r.t the LVL1 Trigger request for reading

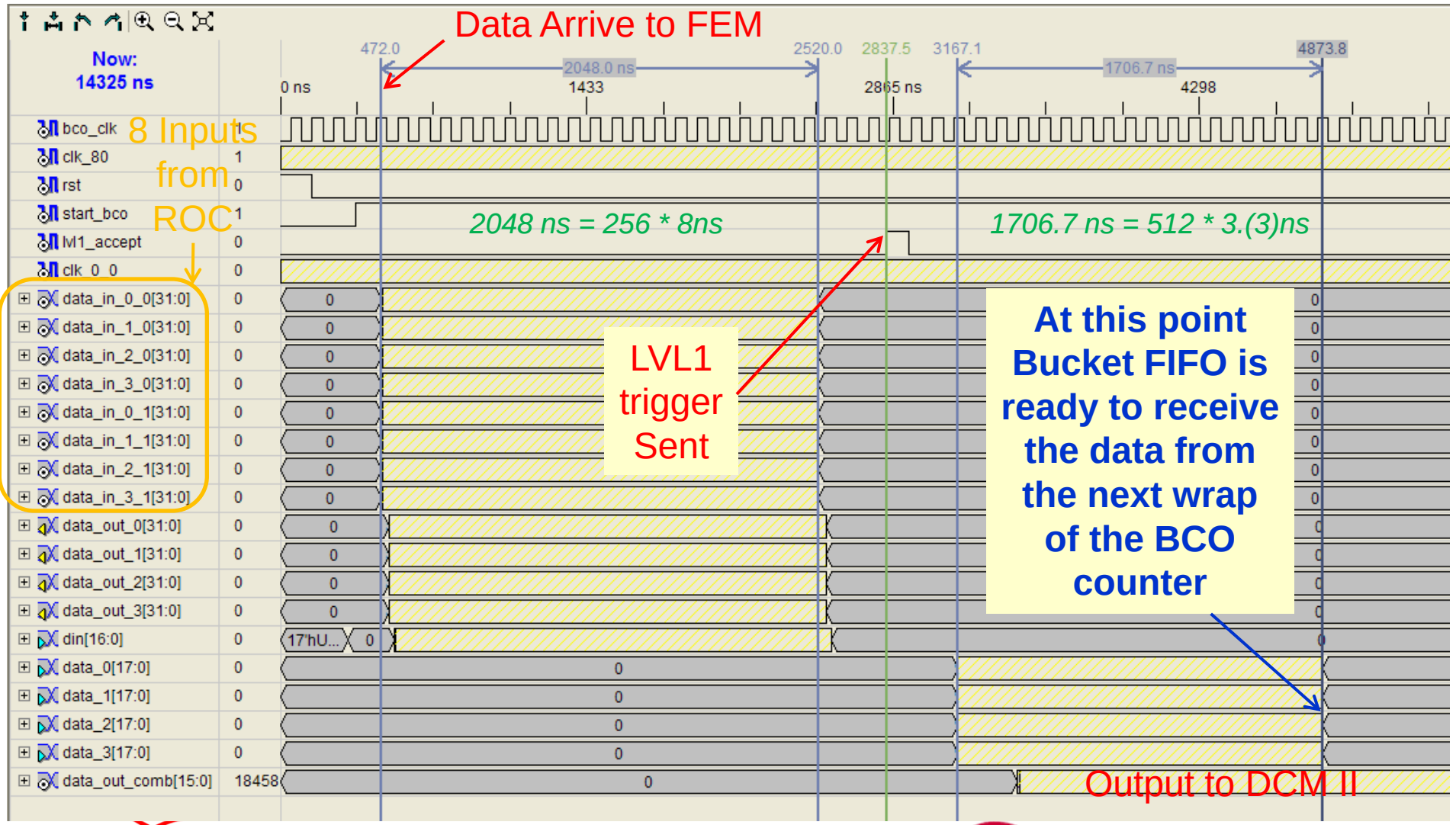
FEM Data Input Latencies



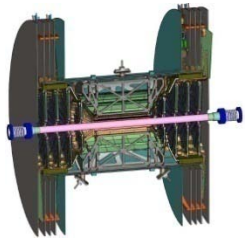


FEM Data Read Latencies



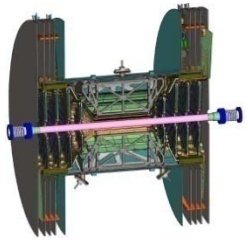


2. Main Conclusions for FEM



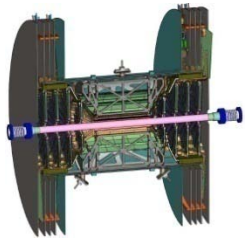
- The worst possible event that need to be assembled on the ROC without raising error condition was simulated
- There is 60 ns latency from the arrival of the data to the ROC to the placement into Bucket FIFO
- LVL1 trigger delay was set to ~ 28 BCO clocks from the data arrival to the ROC
- 46-48 clocks after collision the Bucket FIFO is **emptied** into sub-Event buffer and we are ready to accept the data from the next wrap of the Beam Counter

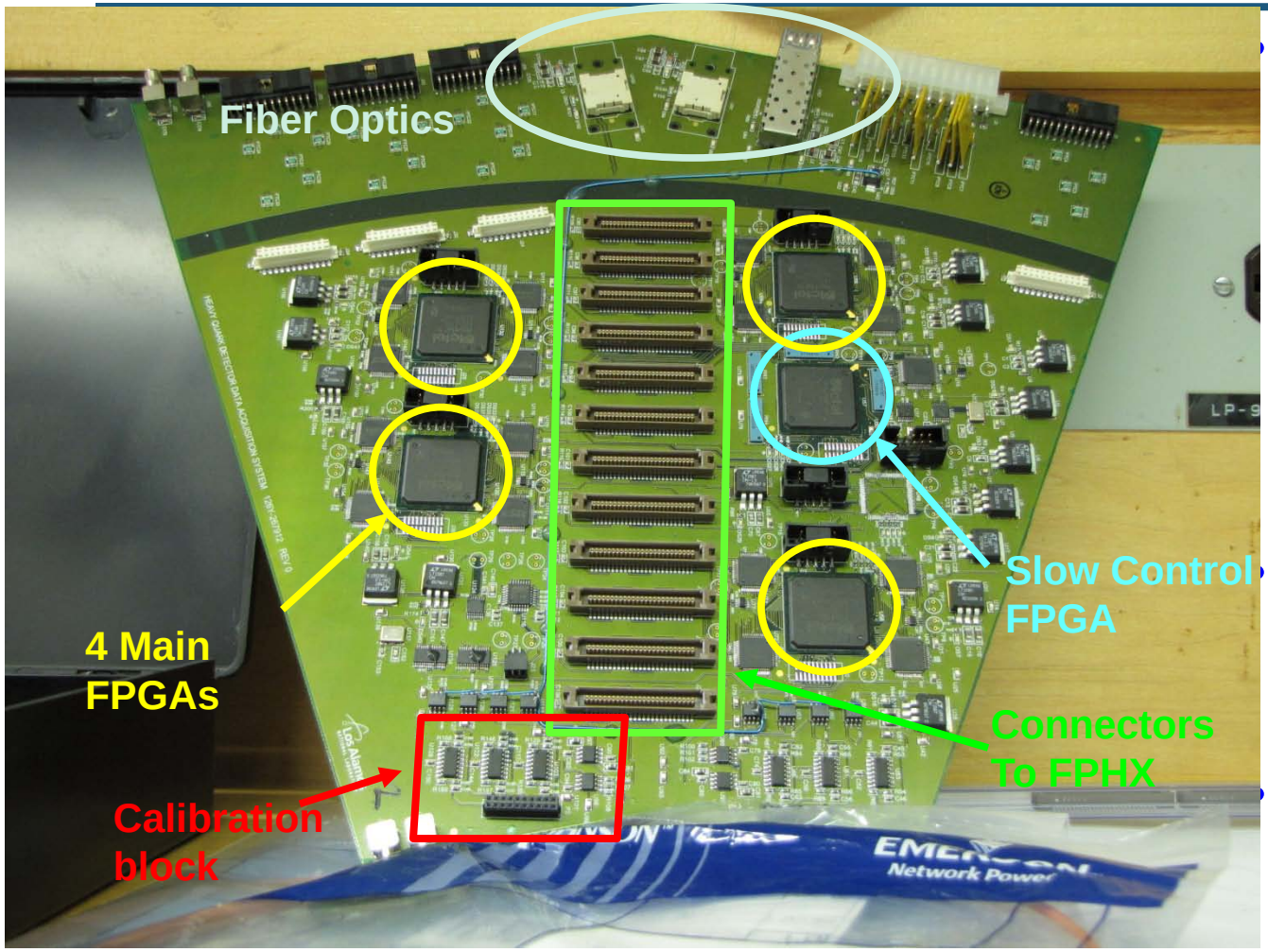
FEM design works in full timing simulation



3. ROC board 1st prototype testing

ROC Board 1st Prototype



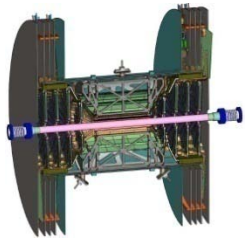


ROC Board 1st Prototype was developed for a slightly different detector readout (smaller FPGAs and different data connectors)

Design of the board is identical to that of the FVTX ROC

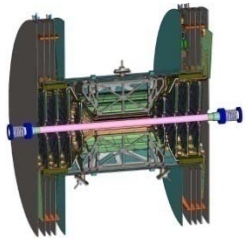
We used this board successfully to test the readout data of up to 18 chips/FPGA

ROC Board Utilization



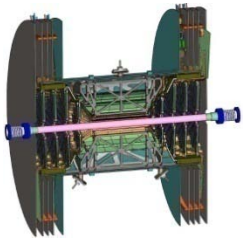
- Main blocks of the code are taken from real ROC FPGA design
- STD speed FPGA are used so 200 MHz operation is glazing the limit
- Main FPGA has 40 differential inputs so we can read up to 20 FPHX chips per design
- 15 chips on a real HDI was a maximum that was read out through a single FPGA. Also ran in 2 FPGA readout mode where each FPGA was reading data from 8 chips in 4 plane telescope mode
- Slow control communication algorithm was developed to communicate to multiple wedges and multiple FPGAs. PYTHON based GUI was developed for visualization
- EEPROM download routines had been successfully tested

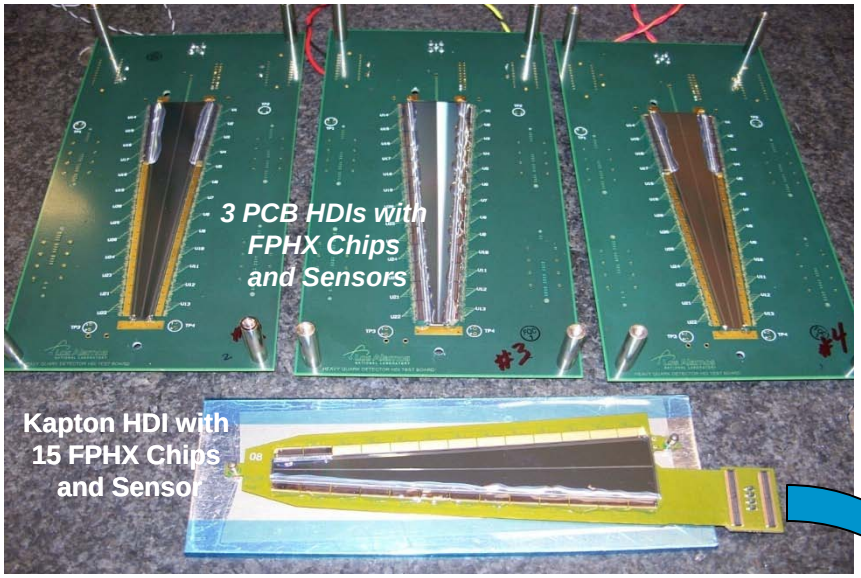
Fiber Optic interface was not tested yet. Currently in progress

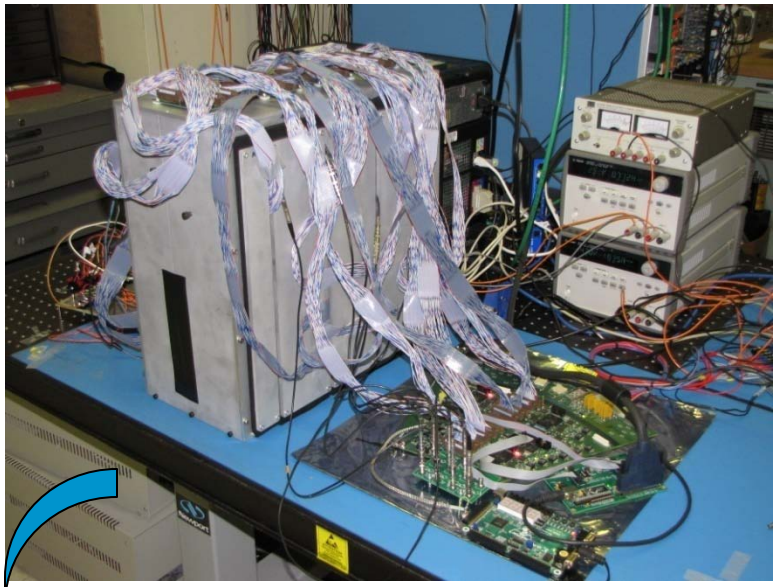


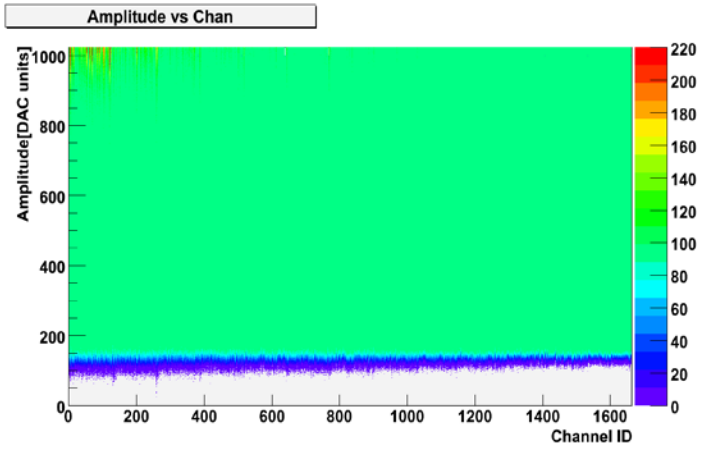
4. Extensive running of the ROC boards

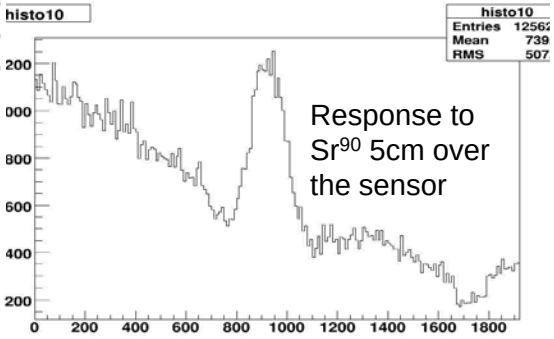
ROC DAQ Test Results

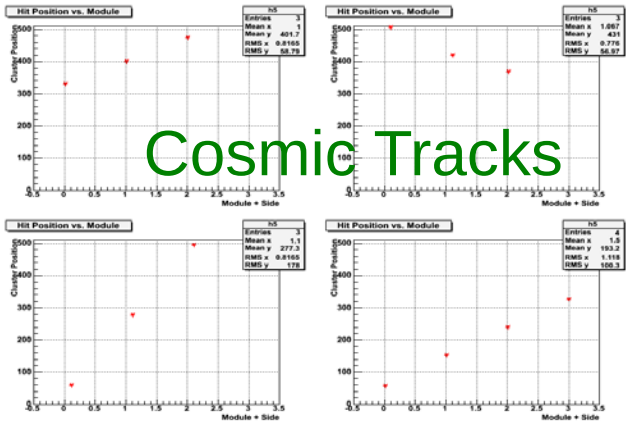


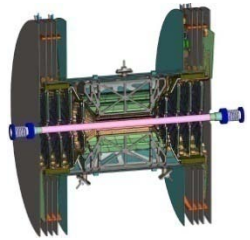






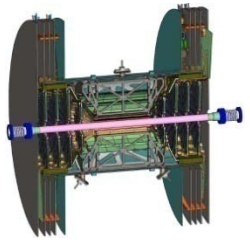






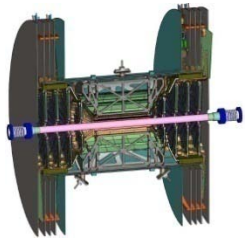
5. Pre-production Prototype Status

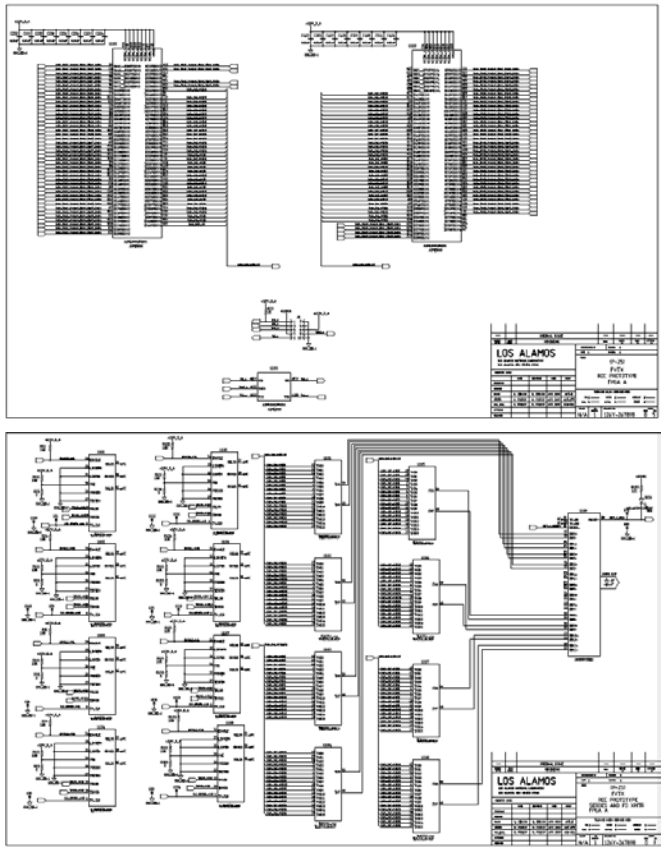
Prototype Schedule



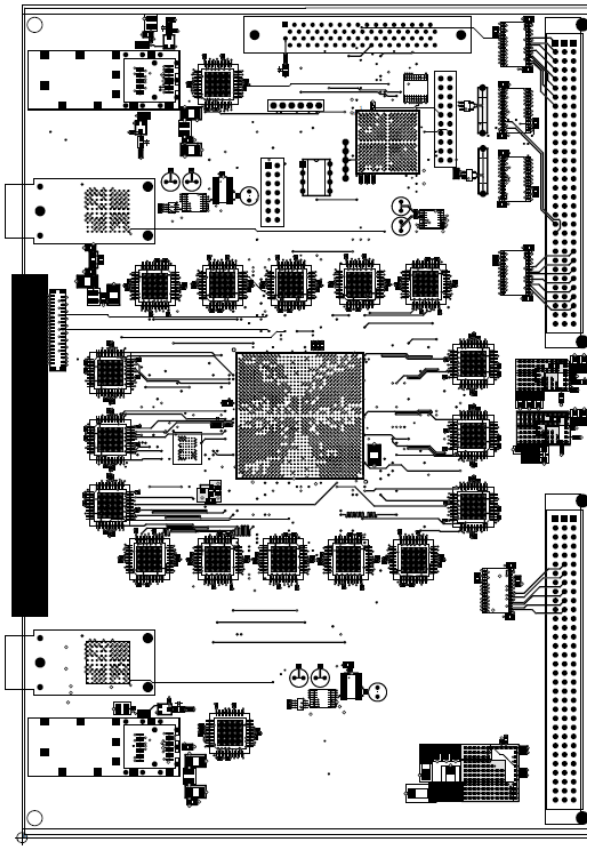
- Schedule for ROC and FEM prototype production slipped by at least 6 month
- We need to study as much as we can with LDRD ROC prototype in this case
- Plan to test Fiber Optics data readout next month
- Experienced ECAD designer's availability is critical for the success of the project and we seem to found the right person for the task
- We also attempt to optimize work load on the ECAD designers to work on both boards in parallel

Where Are We Now

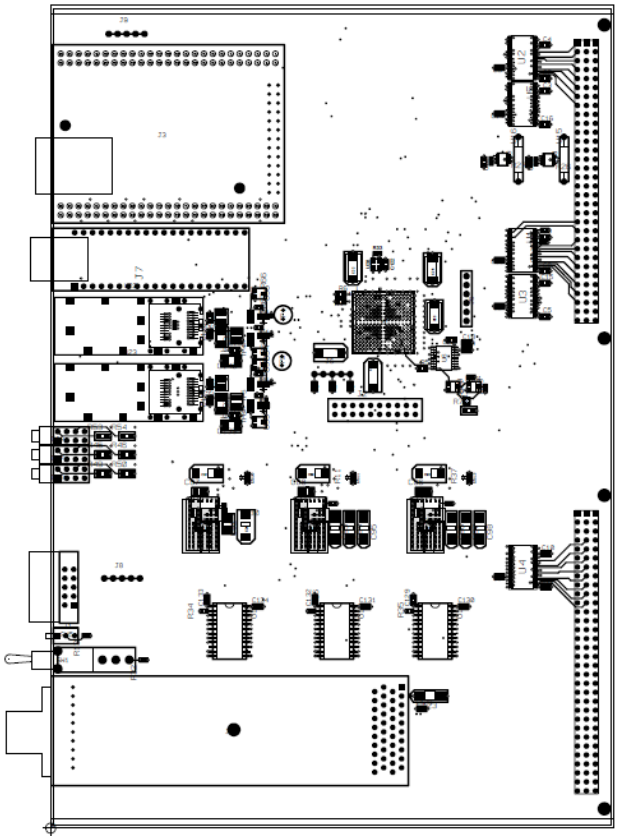




ROC board
(2 out of 81 pages)

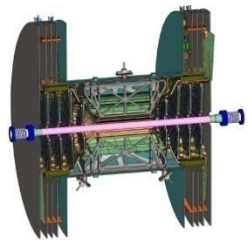


FEM board

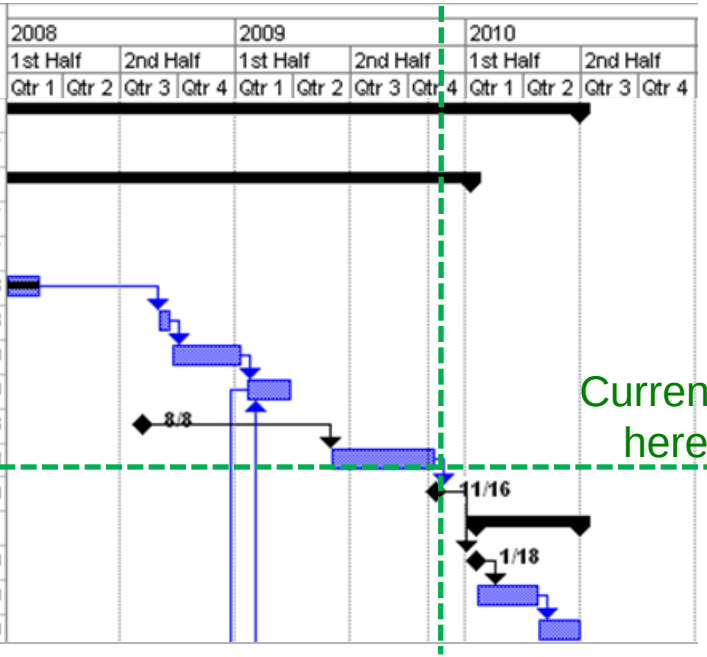


FEM Interface board

Schedule WBS 1.5.2

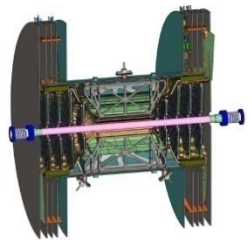


ID	WBS	Task Name	Start	Finish
67	**1.5.2**	**ROC Electronics**	**Tue 1/30/07**	**Thu 7/1/10**
68	1.5.2.1	design	Tue 1/30/07	Mon 3/19/07
69	**1.5.2.2**	**procure prototype**	**Tue 3/20/07**	**Fri 1/8/10**
70	1.5.2.2.1	prototype	Tue 3/20/07	Mon 5/21/07
71	1.5.2.2.2	test prototype	Tue 5/22/07	Mon 7/30/07
72	1.5.2.2.3	redesign	Tue 7/31/07	Mon 2/25/08
73	1.5.2.2.4	2nd prototype ldrd version	Mon 9/1/08	Fri 9/19/08
74	1.5.2.2.5	test second proto	Mon 9/22/08	Fri 1/9/09
75	1.5.2.2.6	PHENIX system test	Tue 1/20/09	Mon 3/30/09
76	1.5.2.2.9	internal design review	Fri 8/8/08	Fri 8/8/08
77	1.5.2.2.7	preproduction prototype FVTX version	Mon 6/1/09	Fri 11/13/09
78	1.5.2.2.8	test ROC	Mon 11/16/09	Fri 1/8/10
79	**1.5.2.3**	**procure production ROC**	**Mon 1/18/10**	**Thu 7/1/10**
80	1.5.2.3.3	final design review	Mon 1/18/10	Mon 1/18/10
81	1.5.2.3.1	production	Tue 1/19/10	Mon 4/26/10
82	1.5.2.3.2	Q/A - 28 units	Tue 4/27/10	Thu 7/1/10

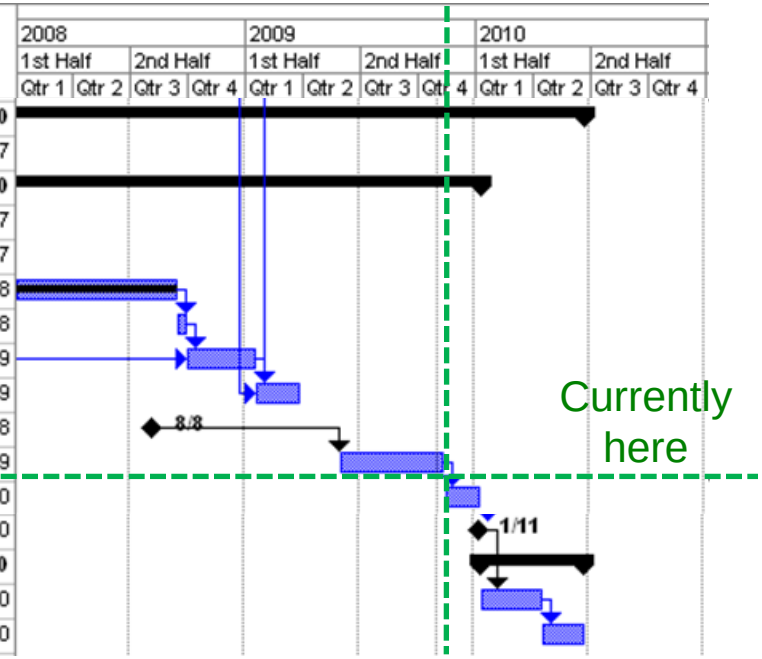


- Getting close to the deadline for ROC production start with prototype development
- Schedule for WBS 1.5.2.3 may slip by about a month
- This puts ROC production on a critical path
- Compensate by faster production turn around

Schedule WBS 1.5.3

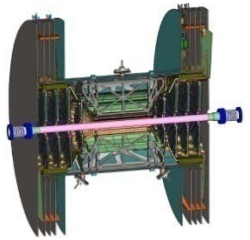


ID	WBS	Task Name	Start	Finish
83	**1.5.3**	**FEM Electronics**	**Tue 1/30/07**	**Thu 6/24/10**
84	1.5.3.1	design	Tue 1/30/07	Mon 3/19/07
85	**1.5.3.2**	**procure prototype FEM**	**Tue 3/20/07**	**Mon 1/11/10**
86	1.5.3.2.1	prototype	Tue 3/20/07	Mon 6/4/07
87	1.5.3.2.2	test prototype	Tue 6/5/07	Mon 8/13/07
88	1.5.3.2.3	redesign	Tue 8/14/07	Mon 9/15/08
89	1.5.3.2.4	2nd prototype	Tue 9/16/08	Mon 9/29/08
90	1.5.3.2.5	test second proto	Tue 9/30/08	Mon 1/19/09
91	1.5.3.2.6	PHENIX system test	Tue 1/20/09	Mon 3/30/09
92	1.5.3.2.9	internal design review	Fri 8/8/08	Fri 8/8/08
93	1.5.3.2.7	preproduction prototype FVTX version	Mon 6/1/09	Fri 11/13/09
94	1.5.3.2.10	Test FEM	Mon 11/16/09	Fri 1/8/10
95	1.5.3.2.8	review and approve FEM	Mon 1/11/10	Mon 1/11/10
96	**1.5.3.3**	**procure production FEM**	**Tue 1/12/10**	**Thu 6/24/10**
97	1.5.3.3.1	production	Tue 1/12/10	Mon 4/19/10
98	1.5.3.3.2	Q/A - 28	Tue 4/20/10	Thu 6/24/10



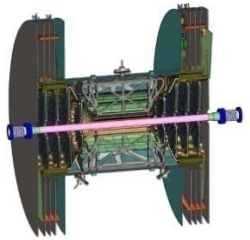
- FEM pre-production prototype will be submitted for production in 2 weeks
- Schedule for 1.5.3.3 may slip by about a month
- FEM production is not on a critical path

Summary and Outlook



- Recommendations from the last DOE 08 review had been implemented
- ROC and FEM prototype board design in progress, expect to receive pre-production prototypes by the end of 2009
- Expect about one month delay with production of ROC and FEM boards. Will try to compensate schedule with a faster procurement
- Experienced ECAD designer had been found at LANL for completion of ROC board layout

The Main Result for 2009



- Tested the full speed readout of several detector modules with 3 independent test stands:
  - calibration mode
  - regular data taking mode
    - particle beam
    - radioactive source
    - cosmic muons
- Demonstrated an **encouraging performance** of the overall readout concept
- Ensured a **reliable operation** of newly developed FPHX chip