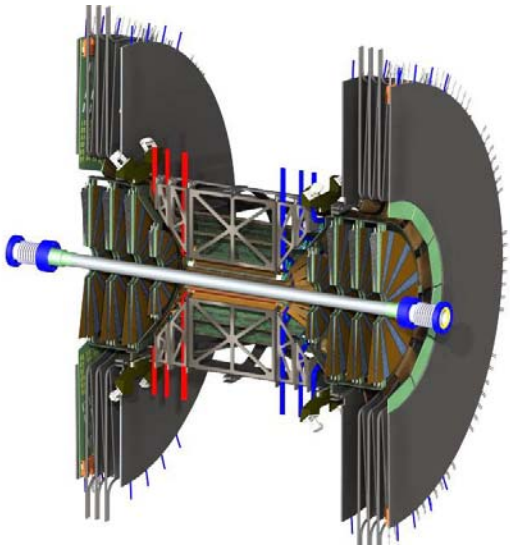

Management Plan
for the

Forward Silicon Vertex Tracker for PHENIX (FVTX)

at the
Brookhaven National Laboratory

For the U.S. Department of Energy
Office of Science
Office of Nuclear Physics

November 11, 2007

PHENIX FVTX Project Management Plan

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1 INTRODUCTION

We propose the construction of two Forward Silicon Vertex Trackers (FVTX) for the PHENIX experiment at RHIC. These would extend the vertex capability of the PHENIX Silicon Vertex Tracker (VTX) to forward and backward rapidities with secondary vertex capability in front of the PHENIX muon arms. The FVTX is shown in Figure 1.

The primary technical improvement provided by the FVTX (as well as the VTX) is to allow for the identification of secondary (also called "separated") vertices near the original event vertex. With an expected distance of closest approach (DCA) resolution of approximately < 200 μm at 5 GeV, we will see improvement in both tracking from the original vertex as well as through identifying the location of secondary vertices caused by the in-flight decay of particles.

The FVTX will be composed of two endcaps, with four silicon mini-strip planes each, covering angles (10 to 35 degrees) that match the two muon arms. Each silicon plane consists of 48 wedges of mini-strips with 75 μm pitch in the radial direction and lengths in the phi direction varying from 3.5 mm at small angles to 11.3 mm at 35 degrees. The maximum occupancy per strip reached in central Au-Au collisions is approximately 2.8%.

The FVTX will have about 0.53 million strips in each forward detector that will be read out with Fermi National Accelerator Laboratory (FNAL) FPHX chips, which are wire bonded directly to the mini-strips. This chip will provide analog and digital processing with zero-suppression and produces a digital output which is "data-pushed" at 200 Mbps to an intelligent readout board containing Field-Programmable Gate Arrays (FPGAs). There the data are extracted and sent via fiber-optic to another readout board in the counting house. On this board, the data are prepared in a standard PHENIX format and, in parallel, a fast "Level-1" trigger algorithm can be run to select interesting events.

The FPHX chip is a modified version of the FNAL FPIX2.1 front end ASIC developed for BTEV. The silicon mini-strip sensor will be a standard p-on-n silicon diode AC-coupled to the FPHX chip.

The FVTX detector will provide vertex tracking over a large coverage in rapidity ($1.2 < |\eta| < 2.2$) with full azimuthal coverage. This will allow for vertex cuts which separate prompt particles, decay particles from short-lived heavy quark mesons and decay particles from long-lived light mesons (pions and kaons). In addition, beauty measurements can be made directly via $B \rightarrow J/\psi+X$ by looking for a displaced J/ψ vertex, which will allow charm and beauty contributions to be separated in semi-inclusive single lepton measurements. Therefore, with this device significantly enhanced and qualitatively new data can be obtained. A more robust and accurate measurement of heavy-quark production over a wide kinematical range will be possible. This new reach to forward and backward rapidity complements that already planned for the central barrel vertex (VTX) silicon detector, which will cover $|\eta| < 1.2$.

The precision of the J/ψ and other di-muon measurements in Au-Au collisions are currently limited in part by the large amount of combinatorial background that must be subtracted from under the signal. With added rejection power for muons from pion and kaon decays, the significance of all di-muon measurements will greatly improve. Further improvement in these measurements results from the improved mass resolution, which will be attained because of the more accurate determination of the opening angles of the di-muons. All together, these will result in improvement of our current di-muon analyses as well as providing access to several new measurements: separation of ψ' from J/ψ, extraction of Drell-Yan from the di-muon continuum and measurement of upsilons at central rapidity.

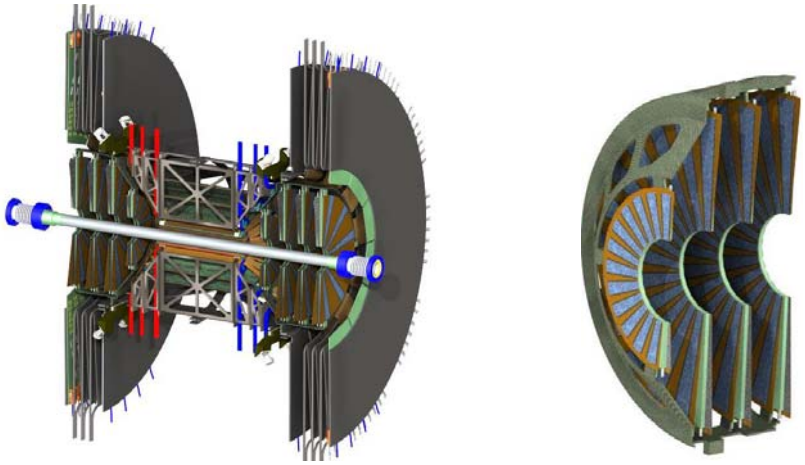


Figure 1 The complete VTX-FVTX detector is shown at left and one half of one arm of the FVTX is shown at the right. Visible at left is the central barrel VTX detector surrounded by the support structure with the cooling lines (red and blue) at each end of the support structure. The FVTX at the right shows each of the 4 disks with the sensor wedge assemblies mounted and all contained with in the FVTX support cage. The large radius sections at each end of the left panel contain the readout electronics for both the VTX and the FVTX.

2 FUNCTIONAL REQUIREMENTS

The principal functional requirement of the FVTX is to provide precise measurements of tracks back to the collision vertex with a transverse distance of closest approach (DCA) resolution on the order of 200 μm or better. The PHENIX FVTX project will be complete when the parameters in Table 1 have been demonstrated and the deliverables in Table 3 are satisfied.

Other general requirements:

- The system must fit into the integration envelope agreed to within PHENIX
- The system must be able to operate inside the PHENIX magnet.
- The system must be safe. The system must meet BNL Collider-Accelerator Department (C-AD) safety requirements.
- The system must not interfere with the VTX or other detector subsystems.

- Each sensor wedge must have a radiation length of less than 2.4 %.
- The system must operate in a temperature range of 0^o C to 20^o C.
- The noise hit rate for each FVTX endcap shall be less than 0.01% for a threshold of ~2000 electrons.
- Survive 200 krad integrated radiation dose over 10 years.
- The FVTX will function properly under all beam species.
- The FVTX system must work within the existing PHENIX readout scheme,
    - must store the data for the LVL1 latency (4 μs),
    - must have a 4-deep buffer of LVL1 accepted events,
    - must readout data within 100 μs to its front-end modules (FEMs) off the detector so as to not significantly reduce the maximum rate of PHENIX Level-1 triggers which is designed to be 10 kHz.

A subset of these requirements is summarized in Table 1 and represents the performance parameters that the project will be responsible for delivering at the project close-out

Table 1 PHENIX FVTX System Functional Requirements

Mini strips active	>90%
Hit efficiency	>95%
Radiation length per wedge	< 2.4 %
Detector hit resolution	< 25 μm
Noise hits/chip	<1%
LVL1 latency	4 μs
LVL1 Multi-Event buffer depth	4 events
Read-out time	< 100 μs
Read-out rate	> 10 kHz

3 TECHNICAL SCOPE

The PHENIX FVTX project is divided into three major subsystem groups: (a) Sensor, chip, High Density Interconnect (HDI) and cooling plate, collectively termed the sensor wedge assembly, (b) DAQ electronics, and (c) mechanical and infrastructure. A summary of the design parameters of the FVTX is given in Table 2.

Table 2 Summary of main design parameters of each FVTX

FVTX	Disk	Z1	Z2	Z3	Z4
Geometrical	Z (cm)	18.7.	25.1	31.5	37.9
Dimensions	R (cm) inner	4.5	4.5	4.5	4.5
	R (cm) outer	9.5	17.0	17.0	17.0
Unit Counts	# of wedges	48	48	48	48
	Sensors/wedge	1	1	1	1
	Readout Chips/wedge	10	26	26	26
	Readout Channels	61.4k	160k	160k	160k
Radiation Length (%) (Wedge)	Sensor (300 μm)	0.32	0.32	0.32	0.32
	glue	0..15	0.15	0.15	0.15
	Bus	0.36	0.36	0.36	0.36
	Ladder & cooling	0.6	0.3	0.3	0.3
	Total	1.46	1.46	1.46	1.46

3.1 Sensor Wedge Assembly

The sensor wedge assembly consists of a wedge shaped heat spreader (cooling plate), a sensor, readout chips called the FPHX, and a copper/kapton bus called the HDI. Shown in Figure 2 is a schematic of the proposed sensor wedge assembly.

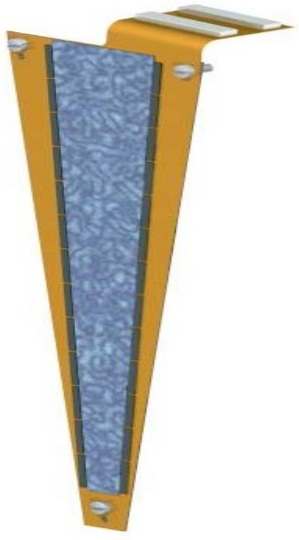


Figure 2 Silicon wedge assembly with the sensor shown in blue, the FPHX chips on the sides of the sensor in gray and the HDI in tan. The carbon cooling plate is not visible but is behind the HDI.

Definitions

- The mini-strip sensor is a single-sided wedge shaped p-n diode with two columns of mini-strips with spacing of 75 microns and lengths varying from 3.5 mm at the inner radius and 11.3 mm at the outer radius.

- The FPHX is an ASIC developed by FNAL and based on a modification of the FPIX2 chip. It has 128 channels of electronics.
- The HDI stands for High Density Interconnect and is a multilayer copper/kapton flat bus which transports the power and grounds and various input and output lines to and from the FPHX chips from the outer radius of the disks.
- The carbon cooling plate is a carbon-carbon composite structure 0.75 mm thick designed to provide mechanical support for the sensor assembly and conduct the heat from the FPHX chips to the outer radius.

Responsibilities

The sensors will be a joint responsibility between US and the Prague group from the Czech Republic, with the Prague group doing the bulk of the R&D. A collaboration has been formed with the FNAL Engineering Dept., headed by Ray Yarema, for development of the FPHX chip. The FNAL group has modified an existing operational FPIX2 chip to our specifications and will produce and test the new FPHX chips. Los Alamos National Laboratory (LANL) will oversee this effort. The HDI will be a joint US institutional responsibility with University of New Mexico (UNM) leading the effort. The sensor wedge assemblies are the responsibility of Columbia University. The cooling backplane will be purchased through an engineering firm, HYTEC.

3.1.1 Silicon Mini-strip Sensors

We will use existing technology for the silicon sensor. Standard p-on-n silicon strip technology, which has been the baseline detector technology for dozens of silicon trackers in Nuclear and High Energy physics experiments, will be used for the FVTX mini-strips. The sensor readout strips will operate at ground potential, and a positive bias voltage (< 100 V) will be applied to the backside of the sensor to fully deplete the sensor volume for efficient charge collection. The sensor design will provide AC coupling. The large sensor wedges for disks 2, 3, 4 are approximately 126.5 mm high, 8.7 mm wide at the inner radius, and 25.3 mm wide at the outer radius. The small sensor wedge for disk 1 is approximately 50 mm high, 8.7 mm at the inner radius, and 16.5 mm at the outer radius. Several, but not all vendors have 6-inch wafer processing capability. The others employ 4-inch wafer processing capability. The advantage to a 6-inch wafer is that an entire unit wedge sensor fits within the useable wafer boundary, whereas a 4-inch wafer forces us to design each full sensor wedge out of two component parts. We have chosen to proceed with a 6-inch wafer. Developing the masks for this effort will be done in concert with the vendors of the sensors. Some prototype sensors have already been produced and lengthy and costly R&D for the sensors is not necessary.

3.1.2 FPHX Chip

The FPHX is a custom IC being designed by Ray Yarema's group at FNAL. The chip design borrows heavily from previously successful IC designs. Each chip is a 128

channel package with an input pitch that is slightly less than 70 um. In a p-on-n detector, the output signal is generated by the collection of positive charge carriers. The FPHX chip is being designed to be compatible with positive charge collection. The design is optimized for the input capacitance range of the strips from the inner most to outer most radius of the sensor. The estimated capacitance range is 0.5 pF to 2 pF. The amplifier has a peaking time of 60 ns and the shaping time can be adjusted through a programmable shaper bias. The chip can accept signals from ac-coupled or dc-coupled sensors and provides leakage current compensation up to 100nA per strip. The noise floor of the analog section is 150e and the noise slope is 140 e/pF. The power consumption is 60-110 μW, depending on the transistor bias current that is set. The dynamic range is 50k electrons and charge gain is 50 mV/fC. A ~70 um pitch on the FPHX chip will allow us to wire bond directly from the sensor to the chip input without the need for an additional pitch adapter. The smaller pitch also allows for space between adjacent chips where bypass capacitors can be placed. One of the most important reasons that drove the design layout to locate the readout chips on each side of the sensor is to minimize possible noise problems associated with long signal return paths between the sensor and the chip. This mitigation is accomplished by locating a bias voltage bypass capacitor as close as possible to the readout chip ground reference and the silicon sensor bias.

The FPHX is designed to be a data-push architecture. It incorporates simultaneous read/write in a dead time free configuration. The FPHX output provides a 7 bit channel address, a 6 bit time stamp, and 3 bits of ADC for each hit and 4 extra bits of status. The chip will also output sync words comprised of 19 zeros followed by a one, which are used by the downstream acquisition to synchronize word boundaries. The functionality of the chip is separated into four distinct phases; analog process the hit, zero suppress, serialize1 and serialize2. The four-phase architecture assures that up to four hits from a single event can be processed and delivered within four beam crossover periods. If there are events in sequential beam crossings, the data will be output, but in greater than a four beam crossing time period. To allow for the possibility of a Level-1 trigger using the FVTX, the data will be read out of the chip within 4 beam clocks.

3.1.3 High Density Interconnect (HDI)

The HDI layers are shown in Figure 3. Indicated are two signal layers, one ground and one power layer. All control lines (which do not have activity during data taking) will be routed under the sensor and all output lines will be routed towards the edge of the wedge thus insuring that the output lines will not couple into the signal lines on the sensor. The number of lines required (8 pairs for the control lines and 2 signal pairs per chip for the output lines) will easily fit within the dimensions of the HDI and the line pitch of the HDI will be very modest allowing us to use conventional kapton PC techniques.

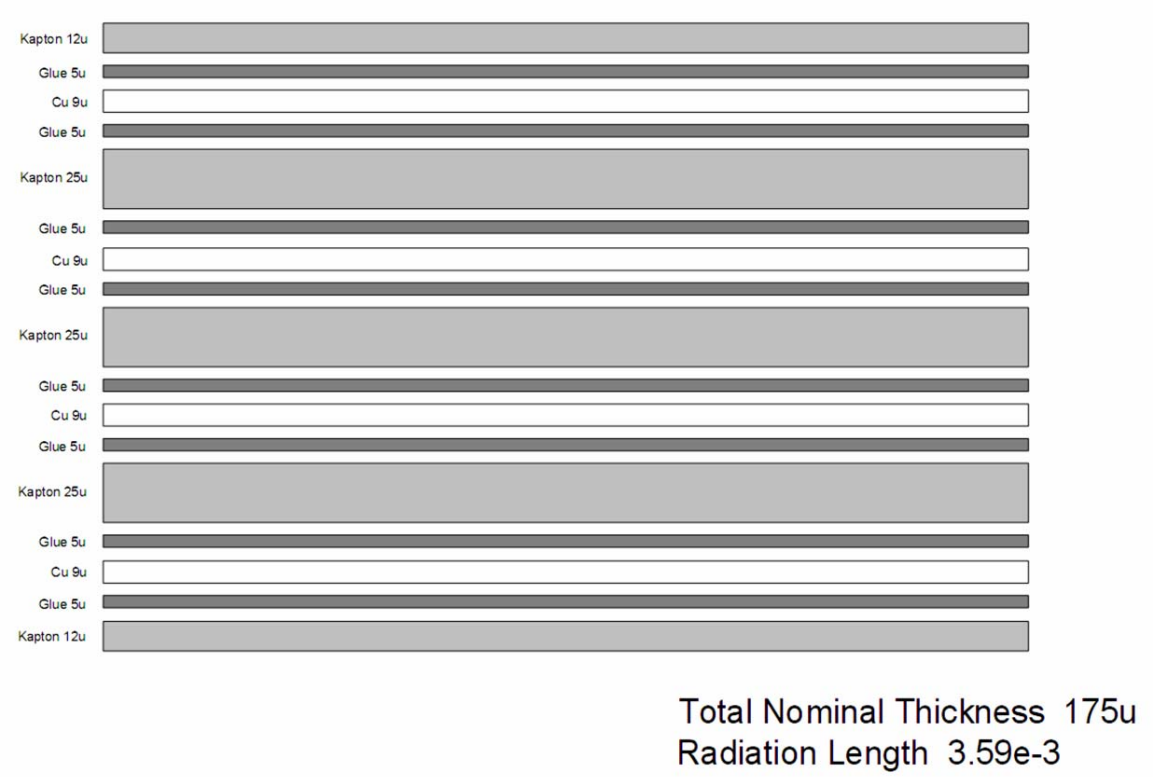


Figure 3 The HDI stack up showing the proposed 4 layer structure. The inner layers are for signals and the outer layers are for power and ground.

3.2 DAQ Electronics

The DAQ electronics take the data from the FPHX chips all the way to the PHENIX Data Acquisition System Data Collection Modules (DCMs). The data flow goes from the FPHX through a multilayer copper/kapton bus to the Readout Card (ROC) located inside and on the back face of the FVTX/VTX enclosure. From there it is transmitted by fiber to the Front End Module (FEM) located in the PHENIX rack room, and then to the PHENIX standard Data Collection Module (DCM).

Definitions

- The ROC is the Readout Card that takes the output from the FPHX chips, formats the data and transmits it via fiber optic cable to the FEM (Front End Module). The ROC also receives the timing and control logic and calibration commands from the FEM and distributes them to t he FPHX.
- The FEM receives the data from the ROC, processes it and sends it to the DCM. The FEM also sends the timing and controls to the ROC.

Responsibilities

The ROC and FEM are the responsibility of LANL. The interconnect bus between the ROC and FEM and fiber optic link are the responsibility of UNM.

3.2.1 Readout Card (ROC)

The FPHX chip will have the following connections to the ROC:

- One calibration line per chip
- One analog and one digital voltage supply and associated grounds
- 6 Low-Voltage-Differential-Signal (LVDS) lines required for downloading, clocking, and resetting the chip
- 2 LVDS data lines per chip sending the data out

The electronics transition module (ROC) will take the continuously streaming data (data-push) from 26 FPHX chips via flexible cables into a FPGA, strip the sync words from the data, combine the data of several chips, serialize it and send it out via fiber to the FEM and the LVL1 boards. The time to receive all of the data to pass to the Level-1 trigger is expected to be less than four beam clocks or 424 nsec. In addition to receiving the data, the ROC will provide calibration pulses, route analog and digital power to the FPHX chips, and provide 6 LVDS lines for downloading the chip configuration and providing clocks and resets. The location of the ROCs will be at the end of the silicon tracker enclosure in the "big wheel" area, as indicated in Figure 1. A block diagram of the ROC is shown in Figure 4. Twelve ROC boards will be required to service one endcap and these boards will hold a total of 84 FPGAs.

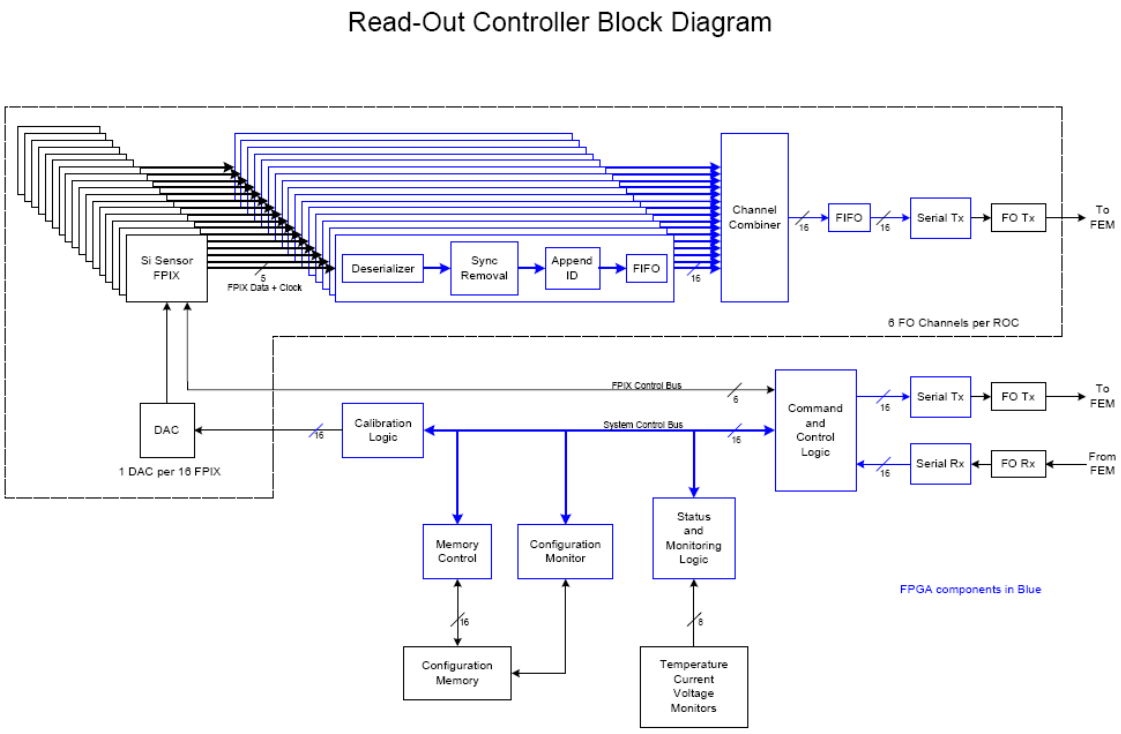


Figure 4 Block diagram of the ROC electronics board.

3.2.2 Front End Module (FEM)

The FEM will buffer the data for 64 beam clocks (emulating the 64 beam clock analog buffer of current PHENIX detectors), grab the data from the appropriate beam clock upon a Level-1 trigger and reformat the data before it is sent to the PHENIX DCMs. The FPHX data with the beam clock counter is routed by an FPGA chip to one of 64 buffers corresponding to the beam clock number. The FPGA then allows the data from the appropriate beam clock to be sent to the DCM if a LV1 trigger accept is received. The existing PHENIX DCMs can be used without modification to take the FEM output into the DAQ. The block diagram of the FEM module is shown in Figure 5.

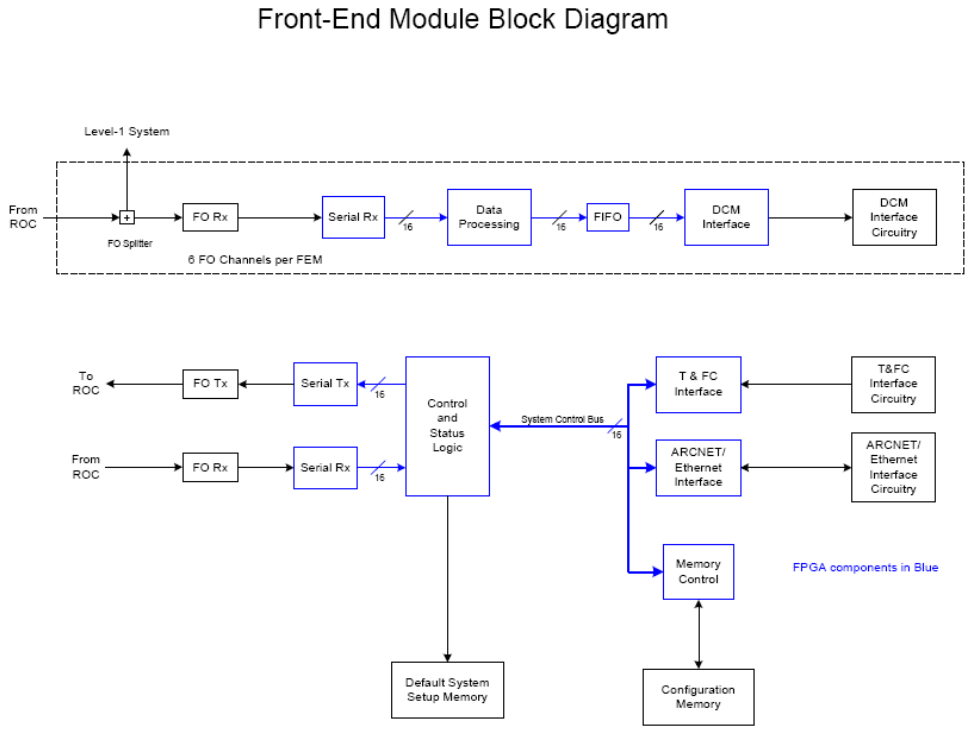


Figure 5 Block diagram of the FEM electronics.

3.3 Mechanics and Infrastructure

We are using the same engineering company (i.e., HYTEC) that is being used by the VTX group to design and produce all of the mechanical structures and wedges for the FVTX. The mechanical enclosure and support stands are being funded and constructed by the VTX project. Close cooperation between the VTX project and FVTX project has insured that the two systems will both fit into the enclosures without interference. The FVTX mechanical support system is composed of a support structure cage that holds 3 large 170 mm radius disks and one 94.4 mm radius disk. Mounted on each disk are 48 sensor wedge assemblies. The internal position tolerance for the wedge assemblies within the FVTX is 25 microns. The cooling system consists of a cooling tube imbedded in the outside diameter of the disk assembly and will be capable of removing ~0.17 Watts of heat from the wedge. The total heat load of each endcap is 54 Watts for the FPHX chips and < 300 Watts for the ROC. The whole FVTX/VTX will be in a dry gas environment of N_2.

The infrastructure for the FVTX includes power supplies, racks, cooling system, control and monitoring, mechanical support between the pole-tips as well as installation rigs.

The disk and cage structure are shown in Figure 6.

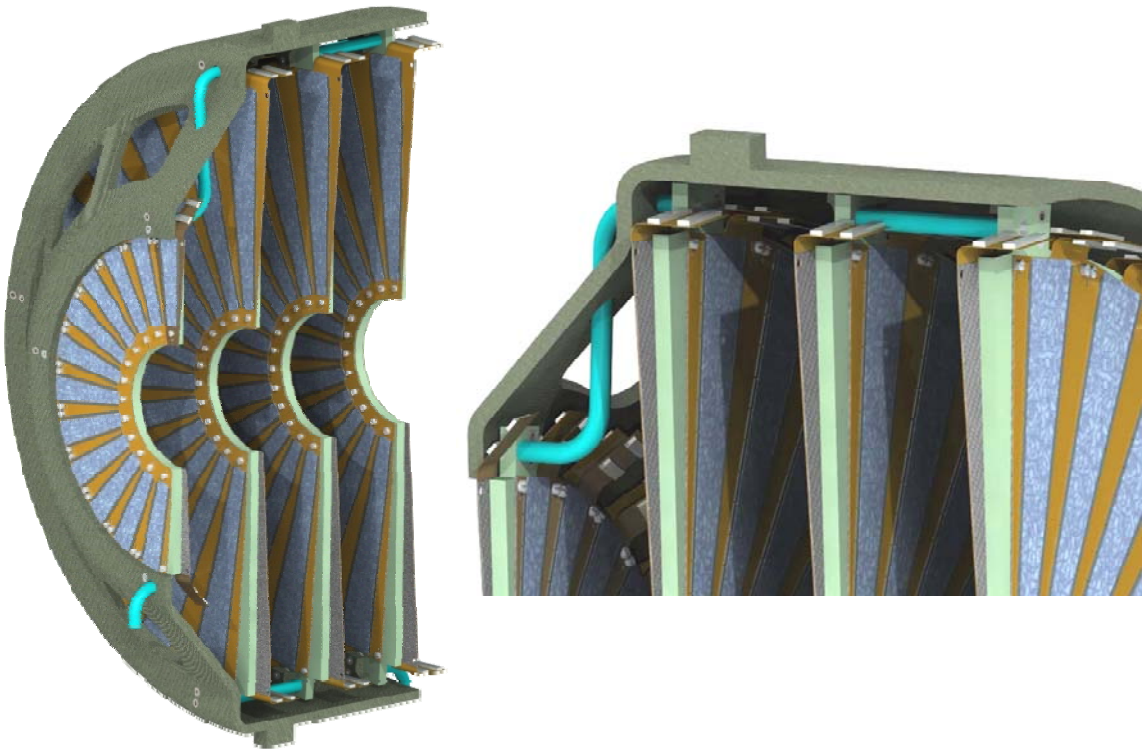


Figure 6 FVTX cage assembly showing the wedges on the disks in the left panel and a close up on the right of the top showing the cooling tube and the mounting tabs.

Definitions

- The sensor wedge assembly is the basic detector unit
- A cooling tube is ductwork containing cooling fluid to remove heat generated by FVTX electronics.
- The disk assembly is a structural unit that holds the individual wedge assemblies. The wedges are pinned to the disk assembly with an accuracy of 25 microns.
- The cage is a structural member that holds the individual disk assemblies to an accuracy of 25 microns. The cage is attached to the VTX support structure.
- The Dry gas enclosure is the outer housing designed to prevent condensation on FVTX/VTX electronics.
- The Suspension system connects the VTX/FVTX to the mechanical support system.
- The mechanical support system consists of support beams running between the PHENIX central magnet pole tips.
- Assembly and alignment fixtures are tools for fabrication of wedge assemblies. The fixtures align components (sensors, chips cooling plate) of a wedge assembly within the required mechanical tolerance and assemble them into a wedge.

- The power supply system includes all low voltage and bias voltage supplies and associated monitoring and control required for the FVTX electronics.
- A new beryllium beam-pipe with a 4 cm inner diameter and with 500 μm nominal thickness will replace the existing larger beam pipe.

Responsibilities

- The design, prototyping, manufacturing of the wedge support, cooling tubes, cage, suspension system, dry gas enclosure, cooling system, and fixtures for assembly and alignment will be contracted out to a mechanical design/fabrication company. The FVTX/VTX mechanical project engineer and FVTX/VTX integration subsystem manager will have oversight of the work performed at this company.
- The mechanical support system for the FVTX/VTX is the responsibility of the integration sub-system manager. It will be paid for by the VTX project, but designed and construction overseen by staff in the PHENIX operations group in consultation with the VTX/FVTX mechanical project engineer.
- The design and fabrication of the assembly and alignment fixtures is overseen by the FVTX mechanical project engineer with the integration manager.
- The installation fixtures to support the VTX/FVTX during installation are the responsibility of the VTX integration subsystem manager. It will be paid for by the VTX project, but designed and construction overseen by staff in the PHENIX operations group in consultation with the VTX mechanical project engineer.
- The infrastructure (racks, power, and cooling) for the power supply system, cooling system and the control systems to monitor operating conditions of the FVTX is the responsibility of the FVTX electronic project engineer. It will be paid for by the FVTX project, but designed and construction overseen by staff in the PHENIX operations group in consultation with the FVTX mechanical and electrical project engineers.
- The power-supply systems for both the sensors and the read-out electronics is the responsibility of the FVTX electrical project engineer.
- The design, fabrication, and installation of the beam-pipe is the responsibility of BNL and is not included in the scope of the FVTX project.

3.3.1 Disk

The wedges populate both sides of the disk. An exploded view of a disk is shown in Figure 7. Visible around the inner and outer radius are the alignment pins for the wedge assemblies. These pins locate the wedge assemblies to better than 25 μm. The assembly procedure will be to place the certified wedge assemblies onto the disk and fasten with nylon screws. A holding jig assembly will be fabricated that will allow the disk to be held while the wedges are placed. After assembly the disk assembly will be surveyed to accurately locate the sensors to ~10 μm.

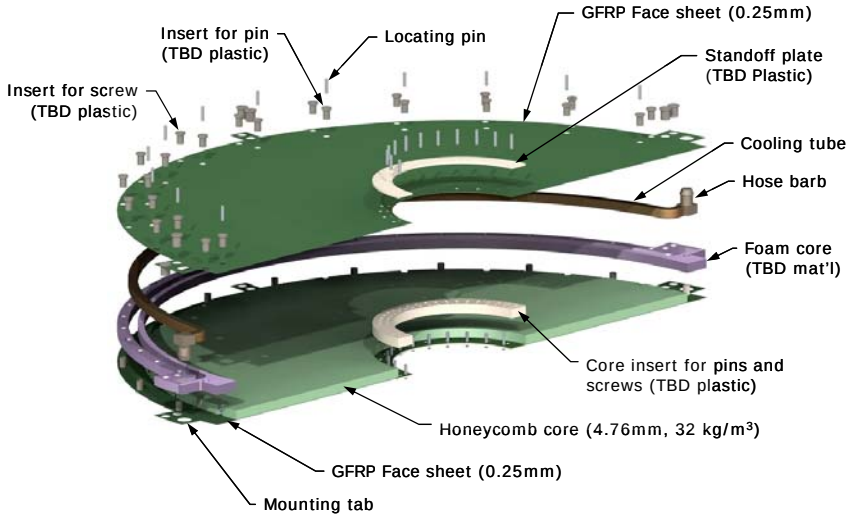


Figure 7 Exploded view of the disk showing the series of alignment pins on the outer and inner radius. The alignment pins accurately locate the wedges on the disk. The cooling tube is visible on the outside radius.

3.3.2 Cage

The assembly into the cage is reasonably straight forward owing to the simplicity of the disk assembly. The disk assembly has three tabs at the outer boundary for attachment to the cage assembly. The general procedure for the cage assembly will be to attach the disks starting with the disk closes to the interaction point and ending with the disk furthest from the interaction point. As each disk is mounted, route the cable with the cable extensions to the rear of the cage. The cable extensions will be connected to the FVTX back plate that holds the Readout Cards (ROC). It has not been determined whether the cage and back plate will be assembled as a unit (preferred) and then inserted into the enclosure or the cage is first inserted into the enclosure and then the back plate is attached.

3.4 Summary of Deliverables

The PHENIX FVTX project will be complete when all component deliverables as specified in Table 3 have been assembled, tested, and received at BNL, and perform to the specifications in Table 1. The performance specifications can be demonstrated either by cosmic rays while the FVTX is installed in the VTX enclosure. We expect that the entire enclosure will be fully tested with cosmic rays prior to beam when the complete tracker is installed in the IR and this will establish project complete. In the "working spares" column there is a hierarchy, i.e. some of the spare sensor modules are used to construct the spare wedges, the rest are kept separate as stand-alone spares.

Table 3 Component Deliverables of FVTX

Item	Number	Working Spares
Wedge assemblies		
Large Sensors	288	50 (25 in spare wedges)
Small Sensors	96	15 (8 in spare wedges)
Large Wedges	288	25
Small Wedges	96	8
ROC boards	24	4
FEM boards	24	4
Mechanical		
Large ½ Disks	12	2
Small ½ Disks	4	1
½ Cage Assembly	4	1
Suspension system	1 (VTX funded)	0
Dry gas enclosure	1 (VTX funded)	0
Cooling system	1 (VTX funded)	0
Power supply system	1	Spare components available
DCM	24	4

4 MANAGEMENT ORGANIZATION

This section describes the management organization and delineates responsibilities within the project. Figure 8 shows the management structure for the PHENIX FVTX project.

4.1 DOE Project Management

The DOE Office of Nuclear Physics (NP) has overall DOE responsibility for the project. Helmut Marsiske is the Federal Program Manager for the project. The NP Program Manager serves as the primary point of contact within SC-26 with the following responsibilities:

- Provides programmatic direction.
- Functions as DOE headquarters point of contact for the project.
- Oversees development of project definition, scope and budget.
- Prepares, defends, and provides project budget with support from the field organizations.
- Approves Level-1 baseline changes.
- Participates in Quarterly Reviews and project reviews.
- Ensures ES&H requirements are implemented by the project.

4.2 BNL Project Oversight

The BNL Project Oversight Manager is Thomas Ludlam, BNL.
He will be administratively and fiscally responsible for the project. In particular he will:

- Provide overall management oversight for all aspects of the project.
- Responsible and accountable for the successful execution of the project.
- Approve key personnel appointments made by the project manager.
- Approve major subcontracts recommended by the project manager.
- Manage the distribution of contingency funds for the project.
- Ensure that the project has demonstrated that it meets the functional requirements.
- Review quarterly status reports.
- Schedule and organize external reviews of the project.
- Ensure the work is performed safely and in compliance with the ISM rules.

The BNL Project Oversight Manager will keep the BNL management and the DOE informed about the technical goals and progress of the project. He will conduct periodic reviews to insure that the project proceeds on budget and on schedule.

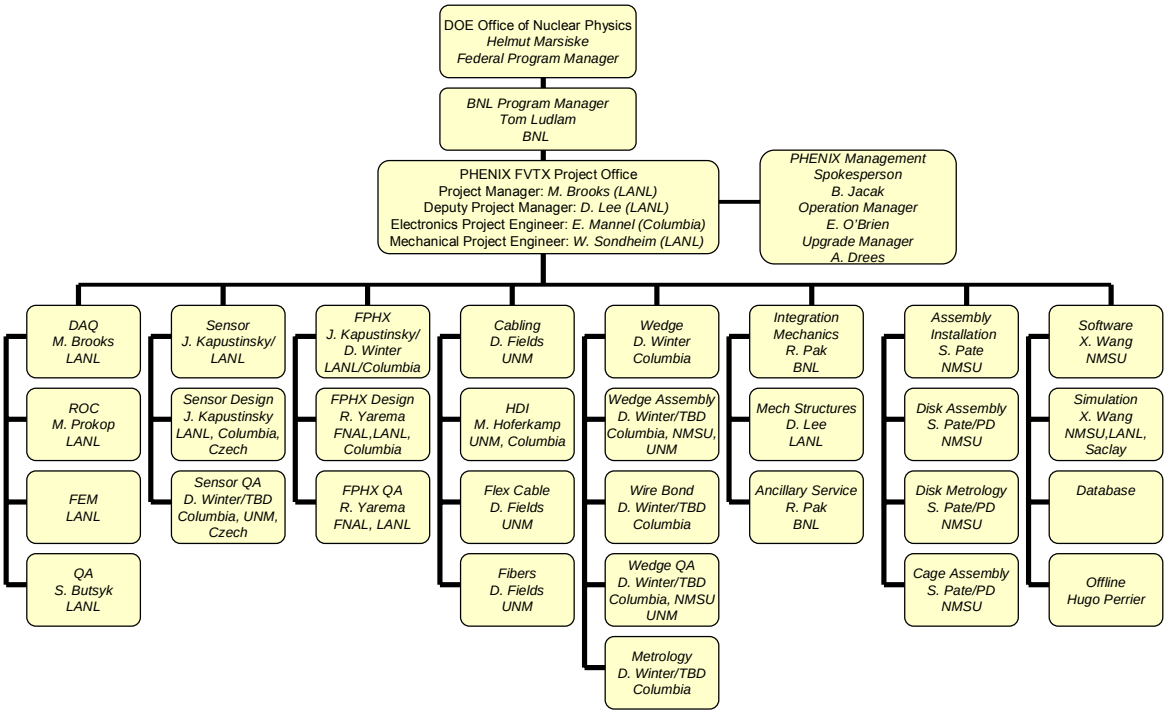


Figure 8 Management chart for the PHENIX FVTX construction project.

4.3 PHENIX Collaboration Management

The PHENIX Collaboration Management has overall responsibility for the successful execution of the scientific operation of the PHENIX detector. Barbara Jacak (Stony Brook) is the PHENIX Spokesperson. Axel Drees (Stony Brook) is the PHENIX Upgrades Manager, and has direct responsibility within PHENIX for oversight of the FVTX project. Edward O'Brien (BNL) is the PHENIX Operations Manager, and has responsibility of the operation of PHENIX and for oversight of all subsystems/detectors in PHENIX. Don Lynch (BNL) is the chief engineer of PHENIX and is responsible for the engineering and technical support, and Yousef Makdisi is the PHENIX safety officer. The PHENIX Management is responsible for the integration of the FVTX detector into PHENIX, and provides the technical support for the commissioning and operation of the completed detector. The PHENIX Management reviews and approves any changes to the baseline performance parameters of the FVTX, in accordance with the change control procedures in Chapter 7.

4.4 Project Management Office

The FVTX project office consists of the project manager and the deputy project manager, along with the project electrical and mechanical engineers. In general, the project manager is responsible for the overall management and the successful execution of the project and delivering all project deliverables including the project scope. The deputy project manager is responsible for tracking the performance of the project, and the project engineers are responsible for the electrical and mechanical oversight of the subsystems.

The full FVTX project office will meet regularly as a group as well as with the PHENIX management to assure that the project meets the performance, budget, and schedule goals.

The **project manager** is Melynda Brooks, LANL.

Responsibilities

The project manager reports to the BNL project oversight manager. The project manager has the following responsibilities:

- With the BNL Oversight Manager, responsible and accountable for the successful execution of the project.
- Delivers project deliverables.
- Keeps the PHENIX management and Executive Council informed on the progress of the project.
- With the project engineers and PHENIX operations manager, ensures that the project integrates properly into the PHENIX detector and with existing subsystems.
- Identifies and ensures timely resolution of critical issues.
- Allocates funds with deputy project manager with consultation with subsystem managers.
- Allocates the contingency funds following approved procedures.

- Appoints subsystem managers with the approval of PHENIX management.
- Organizes and holds regular meetings (weekly and quarterly) of the FVTX group, with the deputy project manager.
- Chairs the FVTX group meetings.
- Submits quarterly status reports, with the deputy project manager.
- Ensures the work is performed safely and provides necessary ES&H documentation, with the deputy project manager and PHENIX safety manager.
- Responsible with the project engineers and subsystem managers for the technical direction of the project.
- Controls changes in the system design requirements, including interfaces between subsystems, with the project engineers.
- Responsible with the deputy project manager and subsystem managers for providing documentation and presentations for project reviews.
- Responsible with the deputy project manager and subsystem managers for developing and maintaining project documentation meeting PHENIX documentation standards.

The **deputy project manager** is David Lee, LANL.

Responsibilities

The deputy project manager and the project manager report to the BNL project oversight manager. The deputy project manager reports to the project manager and will have the following responsibilities:

- With the project manager, responsible and accountable for the successful execution of the project.
- Under the direction of the project manager, delivers project deliverables.
- Supervises the electrical and mechanical project engineers.
- Implements a performance measurement system.
- Develops functional requirements with the project engineers and subsystem managers.
- Identifies and ensures timely resolution of critical issues.
- Chairs the FVTX group meetings when the project manager is not available.
- Develops with the subsystem managers quarterly status reports. The report includes time schedule and spending report.
- Ensures the work is performed safely and provides necessary ES&H documentation, with the PHENIX safety manager.
- Responsible with the project manager and subsystem managers for providing documentation and presentations for project reviews.
- Responsible with the project manager and subsystem managers for developing and maintaining project documentation meeting PHENIX documentation standards.

The **electronic project engineer** is Eric Mannel, Columbia University.

Responsibilities

- Responsible for electronic integration of the FVTX detector into PHENIX.
- Provides electrical oversight for the pixel and strip subsystems.
- Responsible with the subsystem managers for developing and maintaining the documentation of the electronics and electric system meeting PHENIX documentation standards.
- Approves with subsystem managers Q/A procedures and benchmarks for components before they are assembled into ladders.
- Approves with subsystem managers Q/A procedures and benchmarks for assembled ladders.
- Responsible for grounding plan and implementation.
- Responsible for power supply system.
- Under the direction of the project and deputy project managers, delivers project deliverables.
- Identifies and ensures timely resolution of critical issues.
- Responsible with the project and deputy project managers for providing documentation and presentations for project reviews.

The **mechanical project engineer** is Walter Sondheim, LANL.

Responsibilities

- Together with the integration subsystem manager, responsible for mechanical integration of the FVTX detector with PHENIX.
- Develops with the integration subsystem manager the specifications of the FVTX, including position requirements and cooling requirements.
- Responsible for oversight of external contractors for procurement of mechanical components.
- Provides mechanical oversight for each of the pixel and strip subsystems.
- Responsible with the subsystem managers for developing and maintaining the documentation of the mechanical system meeting PHENIX documentation standards.
- Develops with subsystem managers assembly and alignment procedures for assembling components into ladders.
- Approves with subsystem managers Q/A procedures and benchmarks for assembled ladders.
- With the project and deputy project managers, delivers project deliverables.
- Identifies and ensures timely resolution of critical issues.
- Responsible with the project and deputy project managers for providing documentation and presentations for project reviews.

Each of the **subsystem managers** is responsible for one of the major subsystems. The subsystem managers and deputy subsystem managers are:

- Sensors: J. Kapustinsky, LANL
- DAQ: M. Brooks, LANL
- FPHX: J. Kapustinsky, LANL and D. Winter, Columbia
- Flex Cables and HDI: D. Fields, UNM
- Wedge: D. Winter, Columbia
- Assemblies / Installation: S. Pate, NMSU
- Integration: Robert Pak (BNL)
- Software: X. Wang, NMSU

The subsystem managers report directly to the FVTX project office and will be responsible for the design, construction, installation, and testing of their subsystem in accordance with the performance requirements, schedule, and budget.

Responsibilities

- Assemble the staff and resources needed to complete the subsystem in collaboration with the project and deputy project managers
- Develop and follow the system design requirements
- Ensure that subsystems meet the system design requirements, including interfaces
- Responsible for carrying out the design, construction and assembly of the subsystem in accordance with the scope, schedule and budget
- Provide monthly reports on the status of the subsystem to the deputy project manager
- Ensure the work is performed safely and provide necessary ES&H documentation
- Responsible with the project and deputy project managers for providing documentation and presentations for project reviews
- Develop and maintain the documentation of the subsystem.

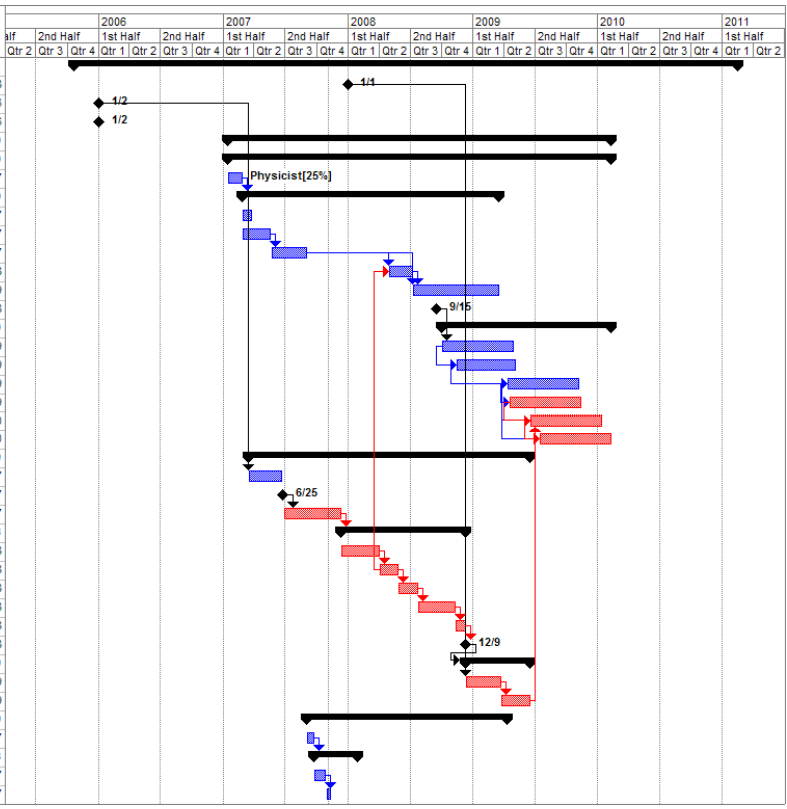
5 SCHEDULES AND BUDGET

The PHENIX FVTX project has been organized into a work breakdown structure (WBS) for purposes of planning, managing and reporting project activities. Work elements are defined to be consistent with discrete increments of project work.

5.1 Schedule

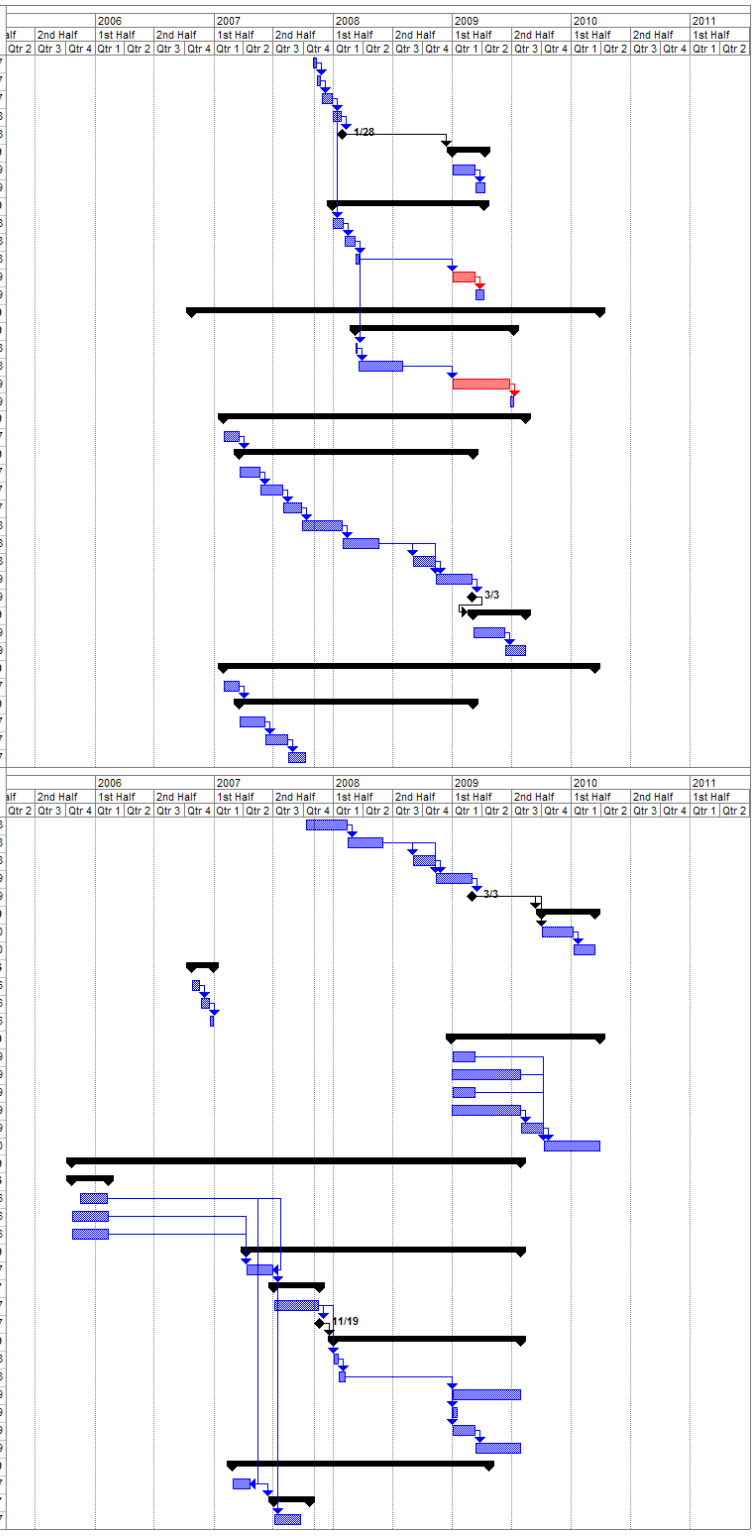
Figure 9 is a Gantt chart of the project schedule, consistent with the WBS. The project begins in Q2FY08 and ends in Q3FY10 with installation into the VTX enclosure. The full VTX/FVTX system is installed and ready for beam by June 2011. Commisioning lasts for 8 months after installation in VTX enclosure and includes initial beam in run 11.

ID	WBS	Task Name	Start	Finish
1	1	**FVTX Project**	**Fri 10/21/05**	**Tue 2/15/11**
2	1.1	**Start Construction**	Tue 1/1/08	Tue 1/1/08
3	1.2	**Start R&D BNL**	Mon 1/2/06	Mon 1/2/06
4	1.3	**Start R&D LANL**	Mon 1/2/06	Mon 1/2/06
5	1.4	**Wedge Components**	**Mon 1/15/07**	**Tue 2/9/10**
6	1.4.1	**Wedge sensors**	**Mon 1/15/07**	**Tue 2/9/10**
7	1.4.1.1	design sensors	Mon 1/15/07	Fri 2/23/07
8	1.4.1.2	**procure prototype sensor**	**Mon 2/26/07**	**Mon 3/16/09**
9	1.4.1.2.1	mask set	Mon 2/26/07	Fri 3/23/07
10	1.4.1.2.2	sensor manufacture	Mon 2/26/07	Fri 5/18/07
11	1.4.1.2.3	test prototype sensor	Mon 5/21/07	Fri 8/31/07
12	1.4.1.2.4	wire bond FPHX	Tue 4/29/08	Mon 7/7/08
13	1.4.1.2.5	test wedge assembly(system test)	Tue 7/8/08	Mon 3/16/09
14	1.4.1.2.6	review and approve sensor design	Mon 9/15/08	Mon 9/15/08
15	1.4.1.3	**procure sensors**	**Wed 10/1/08**	**Tue 2/9/10**
16	1.4.1.3.1	procure sensor	Wed 10/1/08	Tue 4/28/09
17	1.4.1.3.2	Sensor Q/A	Wed 11/12/08	Tue 5/5/09
18	1.4.1.3.3	Attach flex cable	Fri 4/10/09	Thu 11/5/09
19	1.4.1.3.4	Attach sensor	Fri 4/17/09	Thu 11/12/09
20	1.4.1.3.5	wire bond assembly	Wed 6/17/09	Tue 1/12/10
21	1.4.1.3.6	test chip,sensor + cable assemblies	Wed 7/15/09	Tue 2/9/10
22	1.4.2	**FPHX Chip**	**Thu 3/15/07**	**Tue 6/16/09**
23	1.4.2.1	design(FNAL)	Thu 3/15/07	Wed 6/20/07
24	1.4.2.2	Review design	Mon 6/25/07	Mon 6/25/07
25	1.4.2.3	layout	Tue 6/26/07	Mon 12/10/07
26	1.4.2.4	**procure prototype chip**	**Tue 12/11/07**	**Tue 12/9/08**
27	1.4.2.4.1	First MOSIS run	Tue 12/11/07	Mon 3/31/08
28	1.4.2.4.2	test prototype(FNAL)	Tue 4/1/08	Mon 5/26/08
29	1.4.2.4.3	redesign	Tue 5/27/08	Mon 7/21/08
30	1.4.2.4.4	submit 2nd MOSIS run	Tue 7/22/08	Mon 11/10/08
31	1.4.2.4.5	test 2nd proto	Tue 11/11/08	Mon 12/8/08
32	1.4.2.4.6	review and approve	Tue 12/9/08	Tue 12/9/08
33	1.4.2.5	**procure production chips**	**Wed 12/10/08**	**Tue 6/16/09**
34	1.4.2.5.1	engineering run	Wed 12/10/08	Tue 3/24/09
35	1.4.2.5.2	test chips(FNAL)	Wed 3/25/09	Tue 6/16/09
36	1.4.3	**Kapton flex cables HDI**	**Mon 9/3/07**	**Thu 4/9/09**
37	1.4.3.1	design	Mon 9/3/07	Fri 9/21/07
38	1.4.3.2	**procure prototype HDI**	**Mon 9/24/07**	**Mon 1/28/08**
39	1.4.3.2.1	prototype	Mon 9/24/07	Fri 10/26/07
40	1.4.3.2.2	test	Mon 10/29/07	Fri 11/9/07



ID	WBS	Task Name	Start	Finish
40	1.4.3.2.2	test	Mon 10/29/07	Fri 11/9/07
41	1.4.3.2.3	redesign	Mon 11/12/07	Fri 11/23/07
42	1.4.3.2.4	prototype	Mon 11/26/07	Fri 12/28/07
43	1.4.3.2.5	test 2nd prototype	Mon 12/31/07	Fri 1/25/08
44	1.4.3.2.6	review and approve HDI	Mon 1/28/08	Mon 1/28/08
45	**1.4.3.3**	**procure production HDI**	**Fri 1/2/09**	**Thu 4/9/09**
46	1.4.3.3.1	procure	Fri 1/2/09	Thu 3/12/09
47	1.4.3.3.2	test cable	Fri 3/13/09	Thu 4/9/09
48	**1.4.4**	**Kapton HDI to ROC interconnect**	**Mon 12/31/07**	**Wed 4/8/09**
49	1.4.4.1	design	Mon 12/31/07	Fri 2/1/08
50	1.4.4.2	prototype	Mon 2/4/08	Fri 3/7/08
51	1.4.4.3	test prototype	Mon 3/10/08	Fri 3/21/08
52	1.4.4.4	procure	Thu 1/1/09	Wed 3/11/09
53	1.4.4.5	test cable	Thu 3/12/09	Wed 4/8/09
54	**1.5**	**DAQ**	**Mon 10/23/06**	**Mon 3/29/10**
55	**1.5.1**	**Fiber output ROC-FEM**	**Mon 3/10/08**	**Wed 7/8/09**
56	1.5.1.1	design	Mon 3/10/08	Fri 3/14/08
57	1.5.1.2	prototype	Mon 3/17/08	Fri 8/1/08
58	1.5.1.3	procure	Thu 1/1/09	Wed 6/24/09
59	1.5.1.4	test cable	Thu 6/25/09	Wed 7/8/09
60	**1.5.2**	**ROC Electronics**	**Tue 1/30/07**	**Fri 8/14/09**
61	1.5.2.1	design	Tue 1/30/07	Mon 3/19/07
62	**1.5.2.2**	**procure prototype**	**Tue 3/20/07**	**Tue 3/3/09**
63	1.5.2.2.1	prototype	Tue 3/20/07	Mon 5/21/07
64	1.5.2.2.2	test prototype	Tue 5/22/07	Mon 7/30/07
65	1.5.2.2.3	redesign	Tue 7/31/07	Mon 9/24/07
66	1.5.2.2.4	2nd prototype	Tue 9/25/07	Mon 1/28/08
67	1.5.2.2.5	test second proto	Tue 1/29/08	Mon 5/19/08
68	1.5.2.2.6	PHENIX system test	Tue 9/2/08	Mon 11/10/08
69	1.5.2.2.7	preproduction prototype	Tue 11/11/08	Mon 3/2/09
70	1.5.2.2.8	review and approve ROC	Tue 3/3/09	Tue 3/3/09
71	**1.5.2.3**	**procure production ROC**	**Wed 3/4/09**	**Fri 8/14/09**
72	1.5.2.3.1	production	Wed 3/4/09	Tue 6/9/09
73	1.5.2.3.2	Q/A - 28 units	Wed 6/10/09	Fri 8/14/09
74	**1.5.3**	**FEM Electronics**	**Tue 1/30/07**	**Mon 3/15/10**
75	1.5.3.1	design	Tue 1/30/07	Mon 3/19/07
76	**1.5.3.2**	**procure prototype FEM**	**Tue 3/20/07**	**Tue 3/3/09**
77	1.5.3.2.1	prototype	Tue 3/20/07	Mon 6/4/07
78	1.5.3.2.2	test prototype	Tue 6/5/07	Mon 8/13/07
79	1.5.3.2.3	redesign	Tue 8/14/07	Mon 10/8/07

ID	WBS	Task Name	Start	Finish
80	1.5.3.2.4	2nd prototype	Tue 10/9/07	Mon 2/11/08
81	1.5.3.2.5	test second proto	Tue 2/12/08	Mon 6/2/08
82	1.5.3.2.6	PHENIX system test	Tue 9/2/08	Mon 11/10/08
83	1.5.3.2.7	preproduction prototype	Tue 11/11/08	Mon 3/2/09
84	1.5.3.2.8	review and approve FEM	Tue 3/3/09	Tue 3/3/09
85	**1.5.3.3**	**procure production FEM**	**Thu 10/1/09**	**Mon 3/15/10**
86	1.5.3.3.1	production	Thu 10/1/09	Wed 1/6/10
87	1.5.3.3.2	Q/A - 28	Thu 1/7/10	Mon 3/15/10
88	**1.5.4**	**Calibration**	**Mon 10/23/06**	**Fri 12/29/06**
89	1.5.4.1	Design Pulse injection	Mon 10/23/06	Fri 11/17/06
90	1.5.4.2	prototype	Mon 11/20/06	Fri 12/15/06
91	1.5.4.3	test prototype	Mon 12/18/06	Fri 12/29/06
92	**1.5.5**	**Ancillary**	**Tue 12/30/08**	**Mon 3/29/10**
93	1.5.5.1	Racks	Thu 1/1/09	Wed 3/11/09
94	1.5.5.2	LV,HV,crates,etc	Tue 12/30/08	Mon 7/27/09
95	1.5.5.3	DCM-24	Thu 1/1/09	Wed 3/11/09
96	1.5.5.4	Slow controls	Tue 12/30/08	Mon 7/27/09
97	1.5.5.5	Misc lab equip	Tue 7/28/09	Mon 10/5/09
98	1.5.5.6	install	Tue 10/6/09	Mon 3/29/10
99	**1.6**	**Mechanics**	**Fri 10/21/05**	**Wed 7/29/09**
100	**1.6.1**	**specifications**	**Fri 10/21/05**	**Thu 2/9/06**
101	1.6.1.1	endcaps - specify heat load	Tue 11/15/05	Mon 2/6/06
102	1.6.1.2	specify mechanical tolerances/distortions	Fri 10/21/05	Thu 2/9/06
103	1.6.1.3	specify disassembly/configuration options	Fri 10/21/05	Thu 2/9/06
104	**1.6.2**	**Support structure cage**	**Mon 4/9/07**	**Wed 7/29/09**
105	1.6.2.1	design	Mon 4/9/07	Fri 6/29/07
106	**1.6.2.2**	**procure prototype cage**	**Mon 7/2/07**	**Mon 11/19/07**
107	1.6.2.2.1	prototype	Mon 7/2/07	Fri 11/16/07
108	1.6.2.2.2	Review and approve cage design	Mon 11/19/07	Mon 11/19/07
109	**1.6.2.3**	**procure**	**Wed 1/2/08**	**Wed 7/29/09**
110	1.6.2.3.1	final design	Wed 1/2/08	Tue 1/15/08
111	1.6.2.3.2	detail drawings	Wed 1/16/08	Tue 2/5/08
112	1.6.2.3.3	laison	Thu 1/1/09	Wed 7/29/09
113	1.6.2.3.4	tooling	Thu 1/1/09	Wed 1/14/09
114	1.6.2.3.5	material	Thu 1/1/09	Wed 3/11/09
115	1.6.2.3.6	Fabrication	Thu 3/12/09	Wed 7/29/09
116	**1.6.3**	**wedge backplane**	**Mon 2/26/07**	**Wed 4/22/09**
117	1.6.3.1	design	Mon 2/26/07	Fri 4/20/07
118	**1.6.3.2**	**procure prototype wedge backplane**	**Mon 7/2/07**	**Fri 10/19/07**
119	1.6.3.2.1	prototype	Mon 7/2/07	Fri 9/21/07



ID	WBS	Task Name	Start	Finish
121	**1.6.3.3**	**procure**	**Wed 1/2/08**	**Wed 4/22/09**
122	1.6.3.3.1	final design	Wed 1/2/08	Tue 1/15/08
123	1.6.3.3.2	constr drawings	Wed 1/16/08	Tue 2/5/08
124	1.6.3.3.3	liason	Thu 1/1/09	Wed 4/22/09
125	1.6.3.3.4	tooling	Thu 1/1/09	Wed 1/14/09
126	1.6.3.3.5	material	Thu 1/1/09	Wed 3/11/09
127	1.6.3.3.6	fabrication	Thu 3/12/09	Wed 4/8/09
128	**1.6.4**	**support disk**	**Thu 1/4/07**	**Wed 7/29/09**
129	1.6.4.1	R&D design	Thu 1/4/07	Wed 5/23/07
130	**1.6.4.2**	**procure prototype disk**	**Mon 10/22/07**	**Fri 12/14/07**
131	1.6.4.2.1	prototype	Mon 10/22/07	Fri 12/14/07
132	**1.6.4.3**	**Procure**	**Wed 1/2/08**	**Wed 7/29/09**
133	1.6.4.3.1	final design	Wed 1/2/08	Tue 1/15/08
134	1.6.4.3.2	Review wedge,disk,cage	Mon 2/4/08	Mon 2/4/08
135	1.6.4.3.3	construction drawings	Tue 2/5/08	Mon 2/25/08
136	1.6.4.3.4	liason	Thu 1/1/09	Wed 7/29/09
137	1.6.4.3.5	tooling	Thu 1/1/09	Wed 1/14/09
138	1.6.4.3.6	material	Thu 1/1/09	Wed 3/11/09
139	1.6.4.3.7	fabrication	Thu 3/12/09	Wed 7/29/09
140	**1.6.5**	**Alignment and assembly jigs**	**Thu 4/23/09**	**Wed 6/17/09**
141	1.6.5.1	design wedge jig	Thu 4/23/09	Wed 5/6/09
142	1.6.5.2	procure wedge jig	Thu 4/23/09	Wed 6/3/09
143	1.6.5.3	design cool plate jig	Thu 4/23/09	Wed 5/6/09
144	1.6.5.4	procure cool plate ass jig	Thu 5/7/09	Wed 6/17/09
145	1.6.5.5	design cage ass jig	Thu 4/23/09	Wed 5/6/09
146	1.6.5.6	procure cage ass jig	Thu 5/7/09	Wed 6/17/09
147	**1.7**	**Endcap Assembly**	**Wed 9/9/09**	**Tue 2/15/11**
148	**1.7.1**	**Assemble ladders onto cooling plate**	**Wed 9/9/09**	**Tue 4/20/10**
149	1.7.1.1	place wedges on cooling plate	Wed 9/9/09	Tue 4/6/10
150	1.7.1.2	optically survey wedges	Wed 9/23/09	Tue 4/20/10
151	**1.7.2**	**Install into cage enclosure**	**Wed 4/21/10**	**Tue 5/11/10**
152	1.7.2.1	place cooling plates in cage	Wed 4/21/10	Tue 5/11/10
153	1.7.2.2	optically survey	Wed 4/21/10	Tue 5/11/10
154	1.7.3	Test and Install into VTX enclosure	Wed 5/12/10	Tue 7/6/10
155	1.7.4	COMMISION	Wed 7/7/10	Tue 2/15/11
156	**1.8**	**System Integration**	**Wed 1/2/08**	**Tue 11/16/10**
157	1.8.1	Mechanical egineer	Wed 1/2/08	Tue 11/16/10
158	1.8.2	Electrical Engineer	Wed 1/2/08	Tue 11/16/10
159	1.9	FVTX Management	Wed 1/2/08	Tue 11/16/10

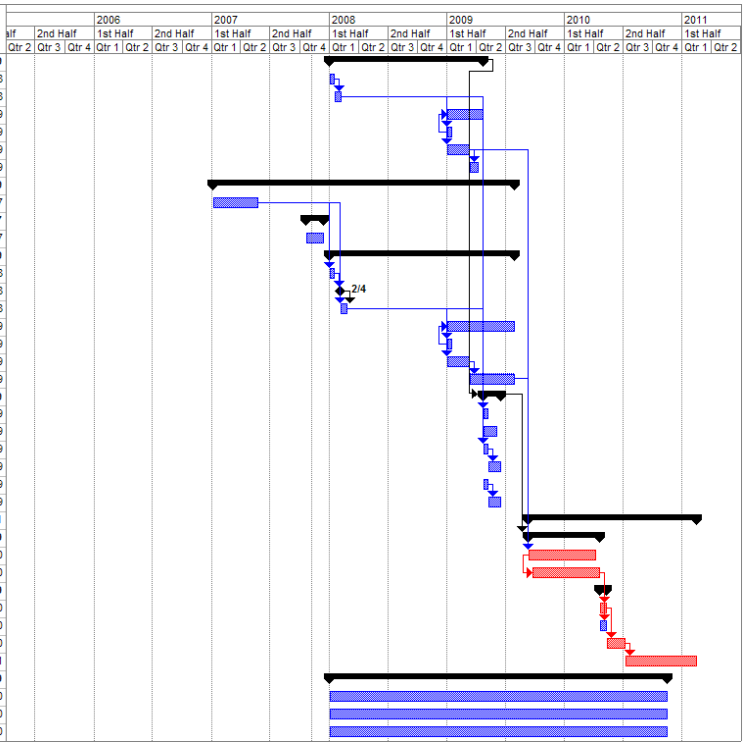


Figure 9 High level schedule of the PHENIX FVTX project.

5.1.1 Control Milestones

WBS 1.1 DOE construction funds received	**2nd Q FY08**
Accounts open	**2nd Q FY08**
WBS 1.4.2.4.6 Sensor, HDI, Chip review	**1st Q FY08**
WBS 1.6.2.2.2 Review and Approve wedge, disk, cage design	**2nd Q FY08**
WBS 1.4.2.5.1 FPHX engineering run	**1st Q FY09**
WBS 1.4.1.3.1 Sensor Procurement	**1st Q FY09**
WBS 1.4.1.3.2 Sensor QA starts	**1st Q FY09**
WBS 1.5.2.2.8 Review and Approve FEM and ROC	**1st Q FY09**
WBS 1.4.1.3.3Wedge Assembly Begins	**3rd Q FY09**
WBS 1.7.1.1 Disk Assembly begins	**3rd Q FY10**
WBS 1.7.2.1 Cage Assembly finished	**3rd Q FY10**
WBS 1. 5.3.3.1 FEM production Complete	**2nd Q FY10**
WBS 1.7.3 Install into VTX enclosure	**3rd Q FY10**
WBS 1.7.3 Project Complete	**4rd Q FY10**

5.2 Budget

The budget summary for the FVTX project is shown in Figure 10 and Figure 11. The inflation adjusted costs of the FVTX project is $ 4.66 M

Forward Endcap Cost Estimate - FVTX

FY2007 dollars

2 endcaps	WBS	Base Cost Total	Base Cost M&S	Workforce	comments	total contingency	Cost with Contingency	2008	2009	2010
Mechanics	1.6									
Mechanical ladder and support structure	1.6.2-1.6.4	352	275	77	HYTEC Estimate	0.27	446		446	
Alignment and Assembly jigs	1.6.5	60	30	30	engineering estimate	0.25	75		75	
	totals	412	305	107			521		521	
Sensor										
Silicon Sensor	1.4.1									
prototype sensor and test	1.4.1.2	85	85		mask,prototype,wire bond,te	0.22	104	104		
purchase	1.4.1.3	410	410		Vendor quotes	0.26	517	100	417	
sensor Q/A and testing	1.4.1.3.2	50		50	University students + engine	0.16	58		58	
	totals	545	495	50			678	204	475	
Readout Chip	1.4.2									
PHX chip, tested	1.4.2									
2 nd Mosis run and test	1.4.2.4.4	95	50	45	FNAL esimate	0.29	122	122		
engineering run	1.4.2.5.1	240	240		FNAL estimate	0.48	355		355	
testing	1.4.2.5.2	50		50		0.16	58		58	
attach HDI to backplane	1.4.1.3.3	30		30	engineering estimate	0.22	37		37	
attach sensor	1.4.1.3.4	30		30	engineering estimate	0.22	37		37	
wire bond assembly	1.4.1.3.5	188	188		Promex quote	0.26	237		237	
test wedge assembly	1.4.1.3.6	40		40	engineering estimate	0.22	49		49	
HDI bus	1.4.3	98	80	18	440 HDI, 10% spares, $250	0.24	122		122	
flex cables, sensor to ROC	1.4.4	56	38	18	784 flex, 10% spares, $42 e	0.16	65		65	
	totals	827	596	231			1081	122	959	
Readout Electronics										
ROC electronics	1.5.2									
preproduction proto	1.5.5.2	71	14	57	engineering estimate	0.36	97	97		
production	1.5.5.3.1	337	282	55	engineering estimate	0.33	449		449	
Q/A	1.5.5.3.2	14		14	engineering estimate	0.14	16		16	
	totals	422	296	126			561	97	465	
FEM electronics	1.5.3									
preproduction	1.5.3.2	80	22	57	engineering estimate	0.36	108	108		
production	1.5.3.3.1	301	260	42	engineering estimate	0.33	401			401
Q/A	1.5.3.3.2	14		14	engineering estimate	0.14	16			16
fibercables, ROC-FEM	1.5.1	17	11	6	440 ea. 54 units	0.16	20		20	
lab equipment	1.5.5.5	100	100		probe, test equipment	0.10	110	110		
	totals	512	393	119			655	218	20	417
Ancillary Systems	1.5.5									
Racks,LV,HV,DCM,crates,install	1.5.5.1-1.5.5.6	99	84	15	existing designs	0.12	111			111
slow controls	1.5.5.4	5		5	existing designs	0.18	6			6
calibration system	1.5.4									
	totals	104	84	20			117	0	0	117
Assembly										
Assemble endcap	1.7	30		30	techs and students	0.26	38			38
Integration										
Electronics Integration	1.8.2	165		165	Engineer	0.14	188	63	63	63
Mechanical Integration	1.8.1	250		250	Engineer	0.14	285	95	95	95
	totals	415		415			473	158	158	158
Management										
Management	1.9	200		200		0.14	228	76	76	76
	total	3468	2169	1298		0.26	4353	874	2673	805
					Inflation adjusted(.035 per year)		**4661**	**905**	**2863**	**893**
BNL overhead 18%					DOE Guidence		4950	900	3000	1050
LANL overhead and GRT 19.5%										
All labor fully burdened										

Figure 10 Summary of the R&D and fabrication costs of the FVTX project.

WBS level 2 Costs By Year in At Year Dollars

WBS No.	Name	FY08	FY09	FY10	TPC
	DOE Budget Guidence	900	3000	1050	
	FVTX project Expenditure				
WBS 1.0	Profile	$905	$2,887	$893	$4,685
WBS 1.4	Wedge Components	$337	$1,560		$1,897
WBS 1.5	DAQ	$326	$519	$592	$1,437
WBS 1.6	Mechanics		$558		$558
WBS 1.7	Endcap Assembly			$42	$42
WBS 1.8	Integration	$163	$169	$175	$507
WBS 1.9	Management	$79	$81	$84	$244

Figure 11 Rolled up costs to WBS level 2 in At Year Dollars.

5.2.1 Risk-based Contingency

The BNL oversight manager manages the contingency funds according to the approved procedures. Contingency is allocated under the change control procedures described in the next section. This section describes how the contingency for a given WBS element is to be calculated. The average contingency for the FVTX is 25.2 %.

This section describes how the contingency for a given WBS element was calculated. Risk is a function of the following factors: the sophistication of the technology, the maturity of the design effort, the accuracy of the cost sources and the impact of delays in the schedule. Risk analysis is performed for each WBS element at the lowest level estimated. Results of this analysis are related to a contingency, which is listed for each WBS element. The goal is to make the method of contingency determination uniform for all project WBS elements.

Definitions

Base Cost Estimate – The estimated cost of doing things correctly the first time. Contingency is not included in the base cost.

Cost Contingency – The amount of money, above and beyond the base cost, that is required to ensure the project's success. This money is used only for omissions and unexpected difficulties that may arise. Contingency funds are held by the Project Manager.

Risk Factors

Technical Risk – Based on the technical content or technology required to complete the element, the technical risk indicates how common the technology is that is required to accomplish the task or fabricate the component. If the technology is so common that the element can be bought "off-the-shelf", i.e., there are several vendors that stock and sell the item, it has very low technical risk, therefore a risk factor of 1 is appropriate. On the opposite end of the scale are elements that extend the current "state-of-the-art" in this technology. These are elements that carry technical risk factors of 10 or 15. Between these are: making modifications to existing designs (risk factor 2-3), creating a new design which does not require

state-of-the-art technology (risk factors 4 or 6), and creating a design which requires R&D, and may advance the state-of-the-art slightly (risk factors 8).

Cost Risk – Cost risk is based on the data available at the time of the cost estimate. It is subdivided into 4 categories.

The first category is for elements for which there is a recent price quote from a vendor or a recent catalog price. If the price of the complete element, or the sum of its parts, can be found in a catalog, the appropriate risk factor to be applied is 1. If there is an engineering drawing or specification for the element, and a reliable vendor has recently quoted a price based on these, the cost risk factor to be applied is 2. Similarly, if a vendor has quoted a price based on a sketch that represents the element, and the element's design will not change prior to its fabrication, the appropriate cost risk factor would be 3.

The second category is for elements for which there exists some relevant experience. If the element is similar to something done previously with a known cost, the cost risk factor is 4. If the element is something for which there is no recent experience, but the capability exists, the cost risk is 6. If the element is not necessarily similar to something done before, and is not similar to in-house capabilities, but is something that can be comfortably estimated, the risk factor is 8.

The third category is for elements for which there is information that, when scaled, can give insight into the cost of an element or series of elements. The cost risk factor for this category is 10.

The fourth category is for elements for which there is an educated guess, using the judgment of engineers or physicists. If there is experience of a similar nature, but not necessarily designing, fabricating or installing another device, and the labor type and quantity necessary to perform this function can be estimated comfortably, a cost risk factor of 15 is appropriate.

Schedule Risk – If a delay in the completion of the element could lead to a delay in a critical path or near critical path component, the schedule risk is 8. If a delay in the completion of the element could cause a schedule slip in a subsystem which is not on the critical path, the schedule risk is 4. Only elements where a delay in their completion would not affect the completion of any other item have schedule risks of 2.

Design Risk – is directly related to the maturity of the design effort. When the element design is nearly complete, quantity counts and parts lists finished, the risk associated with design is nearly zero; therefore a risk factor of 0 is applied. This is also the case when the element is an "off-the-shelf" item and the parts counts and quantities are finalized. When the element is still just an idea or concept, with crude sketches the only justification for the cost estimate, the risk associated with design state is high or 15. Between these two extremes are the stages of conceptual design and preliminary design. In conceptual design, when layout drawings of the entire element are approaching completion, some preliminary scoping analyses have been completed, and parts counts are preliminary, the design risk factor is 8. During preliminary design, when there are complete layout drawings, some

details worked out, complete parts counts, and some analysis for sizing and showing design feasibility, the appropriate design risk is 4.

Weighting Factors

The weight applied to the risk factors depends on whether there are multiple or single risks involved in completing an element.

The weights applied to technical risk depend upon whether the element requires pushing the current state-of-the-art in design, manufacturing, or both. If the element requires pushing both, the weight to be applied is high, or 4; if either the design or manufacturing are commonplace, the weighting factor is 2.

For weights applied to cost risk, the two factors are material costs and labor costs. If either of these are in doubt, but not both, the weight to be applied to cost risk is 1. If they are both in doubt, the weight applied is 2.

The weight factor given to schedule risk is always 1.

The weight factor given to design risk is always 1 and so is not shown explicitly.

Procedure

The following procedure is used for estimating contingency.

Step 1 – The conceptual state of the element is compared with Table 4 to determine risk factors. A technical risk factor is assigned based on the technology level of the design. A design risk factor is assigned based upon the current state (maturity) of the design. A cost risk factor is assigned based on the estimating methodology used to arrive at a cost estimate for that element. Similarly, a schedule risk factor is identified based on that element's criticality to the overall schedule.

Step 2 – The potential risk within an element is compared with Table 5 to determine the appropriate weighting factors.

Step 3 – The individual risk factors are multiplied by the appropriate weighting factors and then summed to determine the composite contingency percentage.

Step 4 – This calculation is performed for each element at its lowest level.

Step 5 – The dollar amount of contingency for an element is calculated by multiplying the base cost by the composite contingency percentage.

Table 4 - Technical, cost and schedule risk factors

Risk Factor	Technical	Cost	Schedule	Design
0	Not used	Not used	Not used	Detail design > 50% done
1	Existing design and off-the-shelf H/W	Off-the-shelf or catalog item	Not used	Not used
2	Minor	Vendor quote	No schedule	Not used

	modifications to an existing design	from established drawings	impact on any other item	
3	Extensive modifications to an existing design	Vendor quote with some design sketches	Not used	Not used
4	New design; nothing exotic	In-house estimate based on previous similar experience	Delays completion of non-critical subsystem item	Preliminary design >50% done; some analysis done
6	New design; different from established designs or existing technology	In-house estimate for item with minimal experience but related to existing capabilities	Not used	Not used
8	New design; requires some R&D but does not advance the state-of-the-art	In-house estimate for item with minimal experience and minimal in-house capability	Delays completion of critical path subsystem item	Conceptual design phase; some drawings; many sketches
10	New design of new technology; advances state-of-the-art	Top-down estimate from analogous programs	Not used	Not used
15	New design; well beyond current state-of-the-art	Engineering judgment	Not used	Concept only

Table 5 Summary cost estimate for the FVTX project

Risk Factor	**Condition**	**Weighting Factor**
Technical	Design OR Manufacturing	2
	Design AND Manufacturing	4
Cost	Material Cost OR Labor Rate	1
	Material Cost AND Labor Rate	2
Schedule	Same for all	1
Design	Same for all	1

6 CHANGE CONTROL

All changes to the technical, cost and schedule baselines shall be identified, controlled, and managed through a traceable, documented change control process using the thresholds described in Table 6.

Items that fall under this Change Control Procedure include the following:

FVTX Engineering Drawings and Schematics with revision "A" or higher.
Controlled FVTX Notes with revision "A" or higher.
Statements of Work.
Specifications.
Memoranda of Understanding.
Requirements Documents.
Lists of Deliverables.
WBS Dictionary.
Project Schedule.
Interface/Integration Specifications.
Integration Envelopes.
Documented Work Procedures.
Rigging Procedures.
Operations Procedures.
VTX Detector Baseline Configuration.

FVTX change control will follow a graded approach with three (3) levels of project impact. All changes are reportable to the FVTX Project Management Office for tracking, but it is only Levels 1, 2, & 3 which requires project office approval. Changes which only affect a single subsystem, do not impact the subsystems interfaces, overall performance, cost, or schedule goals, will be managed and controlled by the subsystem managers. Level 1, 2, &3 changes affect one or more of the following attributes:

- Physical interface: the envelope within which the element will be contained.
- Utilities interface: the location, size, or rate of "flow" of utilities supplied.
- Signal interface: the location, number or size of input/output signal cabling.
- Structural interface: the location, number, shape, size, hole pattern, etc., of the element component from which the subsystem is supported or aligned.
- Parameters, function, and requirements which are used to define the technical scope and specification of the element component.
- Significant cost or schedule changes for a subsystem.

Table 6 defines the three change control levels and the method of review and approval required for each.

Table 6 Change control levels

Level	Cost, Schedule, and Technical Impact	Review/Approval
1	Any deviation from total project cost, or cumulative allocation of contingency > $500k; WBS level-1 milestone delay > 1 month; technical deviation that significantly impacts	Below, plus DOE NP Program

	other PHENIX subsystems, or impacts functional requirements (Table 1) or component deliverables (Table 3).	
2	Deviation from WBS level-2 project cost, or cumulative allocation of contingency > $250k; WBS level-2 milestone delay > 3 months; technical deviation with impact on other PHENIX subsystems but no effect on functional requirements (Table 1) or component deliverables (Table 3).	Below, plus BNL Project Oversight Manager, PHENIX Management
3	Deviation from WBS level-2 project cost, or cumulative allocation of contingency > $50k; WBS level-2 milestone delay > 1 month; technical deviation with minor impact on other subsystems and no effect on functional requirements (Table 1) or component deliverables (Table 3).	FVTX Project Office

7 RISK

The project manager and the deputy project manager will mitigate risk through routine monitoring of the progress and performance of the project, including weekly FVTX teleconferences, quarterly full-day FVTX meetings, bi-weekly meetings of the subsystem managers and monthly meetings with PHENIX and BNL management, and the DOE program office. The final responsibility for risk management will rest with the project and deputy project managers. However, effective risk management requires the involvement of all project members.

The risks associated with the FVTX are generally moderate to low. The highest-risk item is associated with the new ASIC, the FPHX chip, that is being designed by Fermi National Accelerator Lab electronic design group headed by Ray Yarema. The FPHX design incorporates many design features of an existing chip, FPIX2, but there are sufficient differences to make this a moderate risk. The design specifications are modest and fall well within the designs that this group has successfully implemented in the past. A conceptual design has been completed. Simulations of the design demonstrate that it meets all of our design requirements. Previous experience of the FNAL group has shown that their simulations of the chip designs are an excellent predictor of the actual chip.

The sensor design risk is quite low since we have baselined a standard p-n diode that has been the “industry standard” for more than two decades. The risks associated with the sensor are in working with a good manufacturer and getting good yields. We will use all of the accumulated experience to keep this risk low. We have just recently purchased a large number of pixel sensors and had a yield of > 95% although we have not planned for this high a yield.

The DAQ risk is considered moderate. An R&D effort has been underway for the past year on the ROC/FEM system. We have demonstrated that we can operate the ROC at the design specification and deliver event data to the FEM within 4 beam clocks, a specification imposed by the Level-1 trigger. While the Level-1 trigger is not part of this proposal, the implementation of a displaced vertex trigger or an energy loss trigger in the future is deemed important enough to warrant that capability to be designed into the DAQ electronics. In addition, a complete ROC/FEM prototype without the optical fiber that takes the data from the FPHX chips, formats it, and presents it to the DCM has been successfully implemented.

The design of the mechanical system has advanced since it was important to keep in lock step with the VTX mechanical design so that effective integration of the two systems could be maintained. Therefore, based on the R&D done so far the risk associated with the mechanical system is estimated to be moderate to low since we will use a design, analysis, and engineering firm, HYTEC, which has ample experience and expertise on the design of silicon detector mechanics and similarly challenging mechanical systems, including work for the ATLAS silicon tracker. Our low power levels and room temperature operation has greatly simplified the mechanical design. The largest risk is that changes in VTX specifications and design could force a redesign of the FVTX mechanics. Since members of the FVTX team are also involved with the FVTX mechanics, we will attempt to mitigate any serious adverse effects on the FVTX.

The remaining system and the infrastructure consist of a mix of conventional and commercially available components, with low risks. The highest-risk item is the custom installation rigging and support structure from the IR. We are mitigating this risk by having these items designed by the chief PHENIX mechanical engineer.

8 ASSESSMENTS

8.1 Environment, Safety and Health

Environment, safety and health (ES&H) will be integrated into all phases of planning and implementation through to the final design and production processes of the project. The project engineers and mechanical subsystem managers will interface through the PHENIX safety manager to BNL C-AD safety management. The project will conform to BNL's Integrated Safety Management policies.

8.2 Quality Assurance

"Quality" is defined as the "fitness of an item or design for its intended use" and Quality Assurance (QA) as "the set of actions taken to avoid known hazards to quality and to detect and correct poor results." The project and deputy project managers will work with the subsystem managers and the PHENIX operations manager to assure that performance goals are met.

9 PROJECT CONTROLS AND REPORTING SYSTEMS

Technical performance will be monitored throughout the project to insure conformance to approved functional requirements. Monthly and quarterly reports will be compiled and sent to the DOE Office of Nuclear Physics in accordance with their reporting requirements. Design reviews and performance testing of the completed systems will be used to ensure that the equipment meets the functional requirements. For each main system of the FVTX project: there will be the following reviews:

- Design review including detailed concept for the system, detailed cost and schedule.
- Pre-production review, all details settled. A small number of units will be produced and tested, and the performance reported.
- Final design review, final cost and schedule, production QA and testing procedures.
- PHENIX and BNL safety reviews.
- PHENIX operations readiness review.

Technical information concerning the project that is of interest to the FVTX collaboration and the PHENIX collaboration will be published and archived in the existing PHENIX Technical Note system. In general, PHENIX Technical Notes are documents about a topic of a technical subject. These documents should be of an archival nature. PHENIX Technical Notes concerning FVTX can document requirements, specifications, procedures or policies, and are controlled and approved by the FVTX Project Office. The reason for issuing a PHENIX Technical Note is to insure that members of the collaboration and project are aware of its content and are made aware of changes when they occur. This is accomplished by the project office announcing to the collaboration/project that a new PHENIX Technical Note has been issued.

10 INSTITUTIONAL PARTICIPATION

At this point, 16 institutions participate in the FVTX project. The institutions and their anticipated project responsibilities are listed in Table 7.

Table 7 FVTX Project Institutional Participation

Institution	**Project Responsibility and participation**
BARC, Mumbai, India	Simulations
Brookhaven National Laboratory (BNL physics, C-AD)	FVTX detector integration to PHENIX, E,S,H&Q
CEA Saclay, Gif-sur-Yvette, France	Offline
Charles University, Prague, Czech Republic	Sensor, software
Czech Technical University, Prague, Czech	Sensor, software

Republic	
Columbia University	Wedge and sensor QA
University of New Mexico	Cabling and HDI, sensor QA
High Energy Accelerator Research Organization (KEK), Tsukuba, Japan	TBD
Iowa State University	Level-1
Institute of Physics, Academy of Science, Prague (Czech)	Sensor, software
Kyoto University, Kyoto 606, Japan	TBD
Los Alamos National Laboratory	Project Management, DAQ electronics, mechanical system, oversight of the mechanical system
New Mexico State University	Simulation study, wedge, disk, cage assembly
University of Jyvaskyla, Finland	TBD
University of New Mexico	Sensor QA and testing
Yonsei University, Seoul, Korea	TBD