FPHX Specifications and Quality Assurance

FPHX Chip

The ASIC development Group at FNAL, led by Ray Yarema is designing a readout chip that is specifically tailored to the FVTX sensor. Within the Group, Tom Zimmerman is leading the analog section design, and Jim Hoff is leading the digital data acquisition design function of the chip. The data acquisition architecture borrows heavily from Jim's previous design experience on the FPIX chips that were developed for previously successful IC designs, FPIX2, FSSR, SVX4, etc.. The FVTX custom IC has been named the FPHX chip. Each chip is a 128 channel package with an input pitch that that is

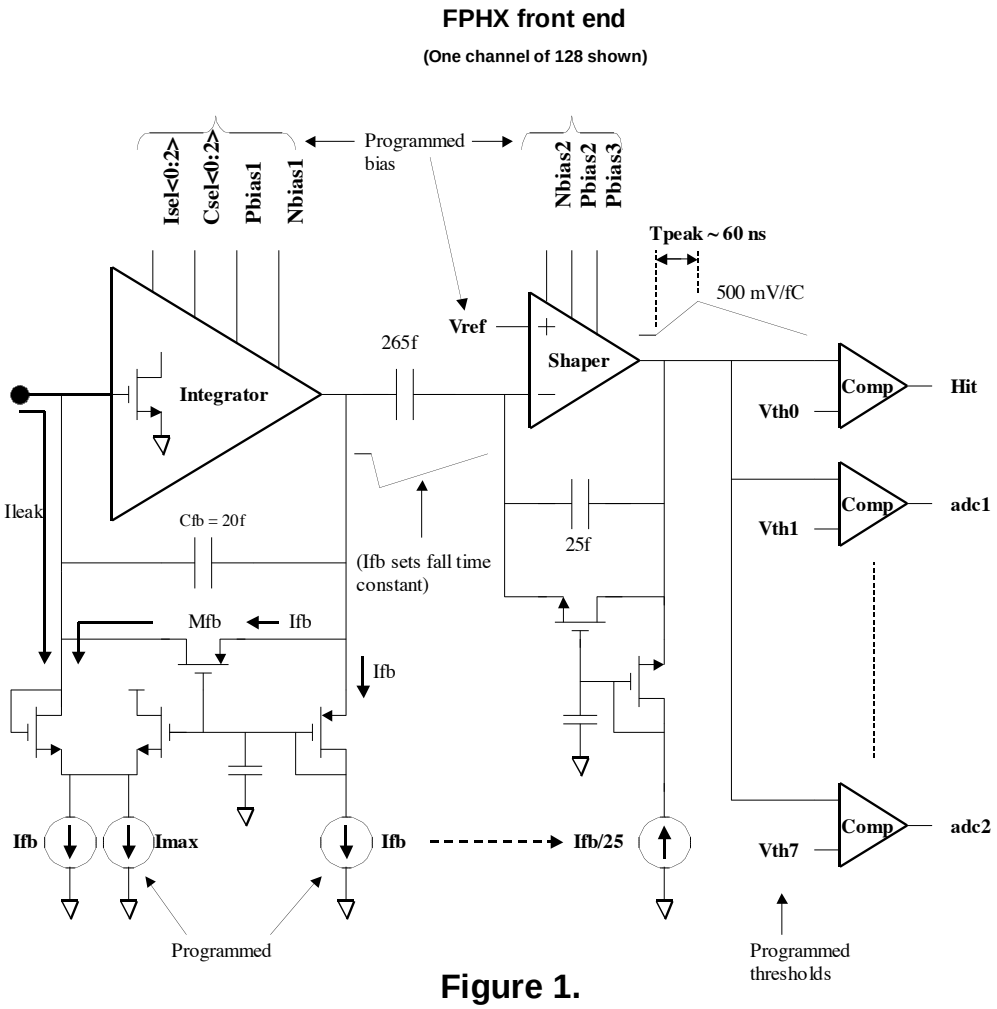

Figure 1.

slightly less than the 75 μm sensor strip pitch.

The schematic for one channel is shown in figure 1. The front end amplifier is designed to accept positive charge input from the p-on-n silicon sensor. It is optimized for the input

capacitance range of the strips from the innermost to outermost radius of the sensor. The estimated capacitance range is 0.5 pF to 1.5 pF. The integrator charge gain is 50 mV/fC and the dynamic range of the front end is 50,000 electrons, corresponding to 4X the average charge deposited per strip per hit (particles hit the strips at an angle so the average charge deposited in a strip is a fraction of the 24,000 electrons generated at normal incidence).The CR-RC shaper has a peaking time of 60 ns (see figure 3), and the shaping time can be adjusted through a programmable shaper bias. The chip works with either ac or dc coupled input, and provides leakage current compensation up to 100nA per strip in dc-coupled mode. The noise floor of the analog section is 150e and the noise slope is 140 e/pF (figure 4.) Based on these specifications, we will be able to set discriminator threshold at more than a factor of 5 above noise, and less than ¼ of the average expected charge per strip per hit. The power consumption is 60-110 uW, depending on the transistor bias current that is set. The simulated performance of the FPHX chip is shown in figures 3 and 4.

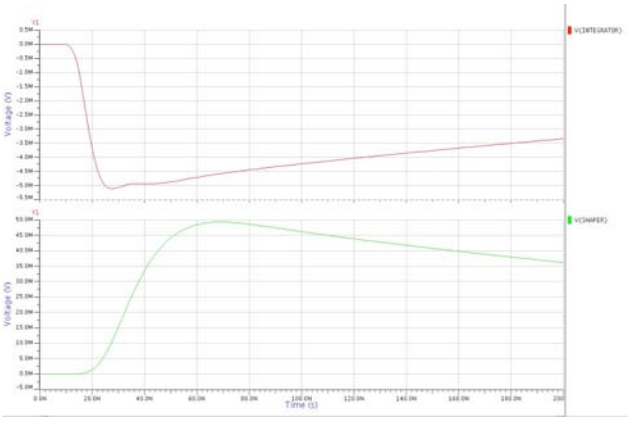

Figure 3. Pulse Shape before and after shaper.

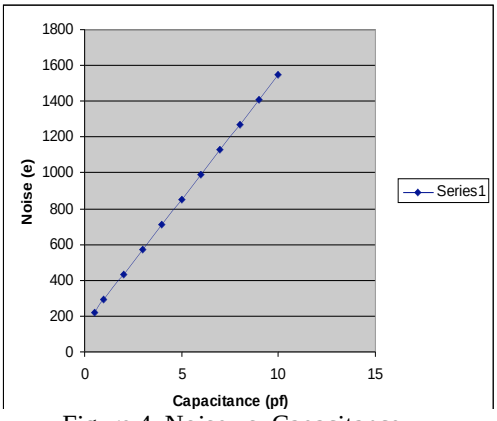

Figure 4. Noise vs. Capacitance.

The approximate dimensions of the FPHX are 9.0mm H X 2.5mm W. The pitch on the FPHX chip will allow us to wire bond directly from the sensor to the chip input without an additional pitch adapter. The smaller pitch also may allow for space between adjacent chips where bypass capacitors can be placed. One of the most important consequences of the design layout is to locate the readout chips on each side of the sensor, where decoupling between the analog ground and the sensor bias can be made with short electrical connections. This minimizes possible noise problems associated with long signal return paths between the sensor and the chip.

The output, clock and control pads are all located on the side of the chip opposite from the inputs and they are wire bonded to a high density interconnect cable. The digital connections are arranged to minimize their effect on the analog inputs.

The FPHX is designed to be data push architecture. It incorporates simultaneous read/write in a dead time free configuration. The FPHX output provides a 7 bit address, a 6 bit time stamp, and 3 bits of ADC for each hit. The ADC DACs are independently programmable to allow for a non-linear ADC. The chip will also output sync words comprised of 19 zeros followed by a one, which are used by the downstream acquisition

to synchronize word boundaries. The functionality of the chip is separated into four distinct phases; analog processing of the hit, zero suppression, serialize1 and serialize2. The four-phase architecture assures that up to four hits from a single event can be processed and delivered within four beam crossover periods. In the rare case that there are events in sequential beam crossings, all the data will be output, but in more than four beam crossings.

QA

The design layout of the FPHX chip will be qualified using software tools that verify correct process and performance design criteria. Additional simulations will be performed to model various input data patterns to evaluate performance of the chip. Before the design is released to the foundry, there will be a design review. The participants will include the FNAL design team, appropriate representation from the FVTX collaboration, and an external reviewer.

The first submission will be made to MOSIS to fabricate prototype quantities of FPHX die. FNAL has committed to develop the software and hardware necessary to probe and test the die on their probe station. FVTX personnel, led by Jon Kapustinsky, LANL,and David Winter, Columbia, will participate in all aspects of the die testing at FNAL. Following the probe tests, the die will be extensively tested in the lab using test boards and wire bonding test die to prototype sensors. All the analog and digital functions of the die will be exercised. Lab bench tests will be carried out in parallel at FNAL, UNM and Nevis Labs using a common test stand design. If design problems are identified in the FPHX, there is schedule contingency for a design correction, and a second prototype submission to MOSIS, and a subsequent round of testing. In total, eight months have been scheduled for all FPHX prototyping and testing. Prior to submitting the engineering run for production quantities, a review will be held to include the FNAL design team, appropriate representation from the FVTX collaboration, and an external reviewer.

The engineering run submission will be made to TSMC on a 0.25 μm process line. The wafers will be probe tested at FNAL with the participation of FVTX personnel. The majority of QA testing for production lots will be done on the probe station by measuring reference parameters. Assuming an historical average 80% yield, the total number of production wafers needed is 15, which represents 1 ½ submissions (1088 die per wafer). The minimum follow-on submission is ½ lot. If the production yield is 90%, we will only need 10 wafers. A total of 3 months is scheduled for production QA.

Facilities and Manpower

FNAL has automated probe stations equipped with electronic characterization equipment. The electronics department head, Ray Yarema, has agreed to commit FNAL engineers and technicians to develop FVTX specific probe station software and hardware to QA the

FPHX chip. In addition, Ray has agreed that FVTX personnel will participate in all aspects of the QA at FNAL. An office and workstation is being set up in the electronics department to accommodate FVTX personnel during the QA.

There are test labs at UNM, LANL, Columbia-Nevis, and in Prague. FPHX die, especially at the prototype stage, will be distributed to these Labs for parallel evaluation.

The probe station at FNAL can be operated by a single student for the production run QA. A UNM student has recently become proficient on the FNAL probe station, testing several FPIX wafers for a LANL-LDRD project.