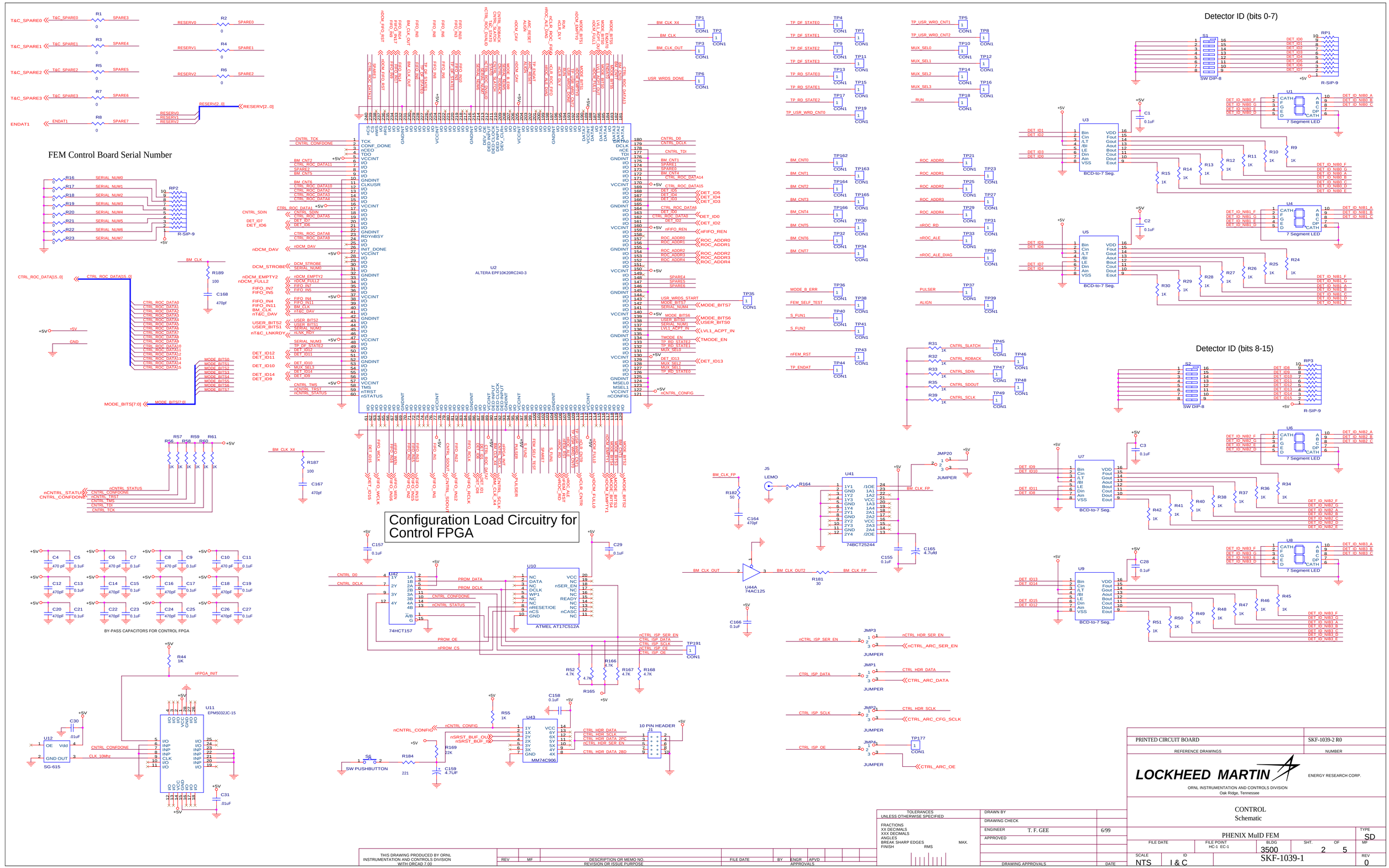

PRINTED CIRCUIT BOARD		SKF-1039-2 R0	
REFERENCE DRAWINGS		NUMBER	

LOCKHEED MARTIN — ENERGY RESEARCH CORP.

ORNL INSTRUMENTATION AND CONTROLS DIVISION
Oak Ridge, Tennessee

CONTROL
Schematic

PHENIX MuID FEM

FILE DATE	FILE POINT HC-1 EC-1	BLDG	SHT.	OF	TYPE	MF
		3500	2	5	SD	

SCALE	ID		REV
NTS	I & C	SKF-1039-1	0

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS
XX DECIMALS
XXX DECIMALS
ANGLES
BREAK SHARP EDGES MAX.
FINISH RMS

DRAWN BY		
DRAWING CHECK		
ENGINEER	T. F. GEE	6/99
APPROVED		
DRAWING APPROVALS		DATE

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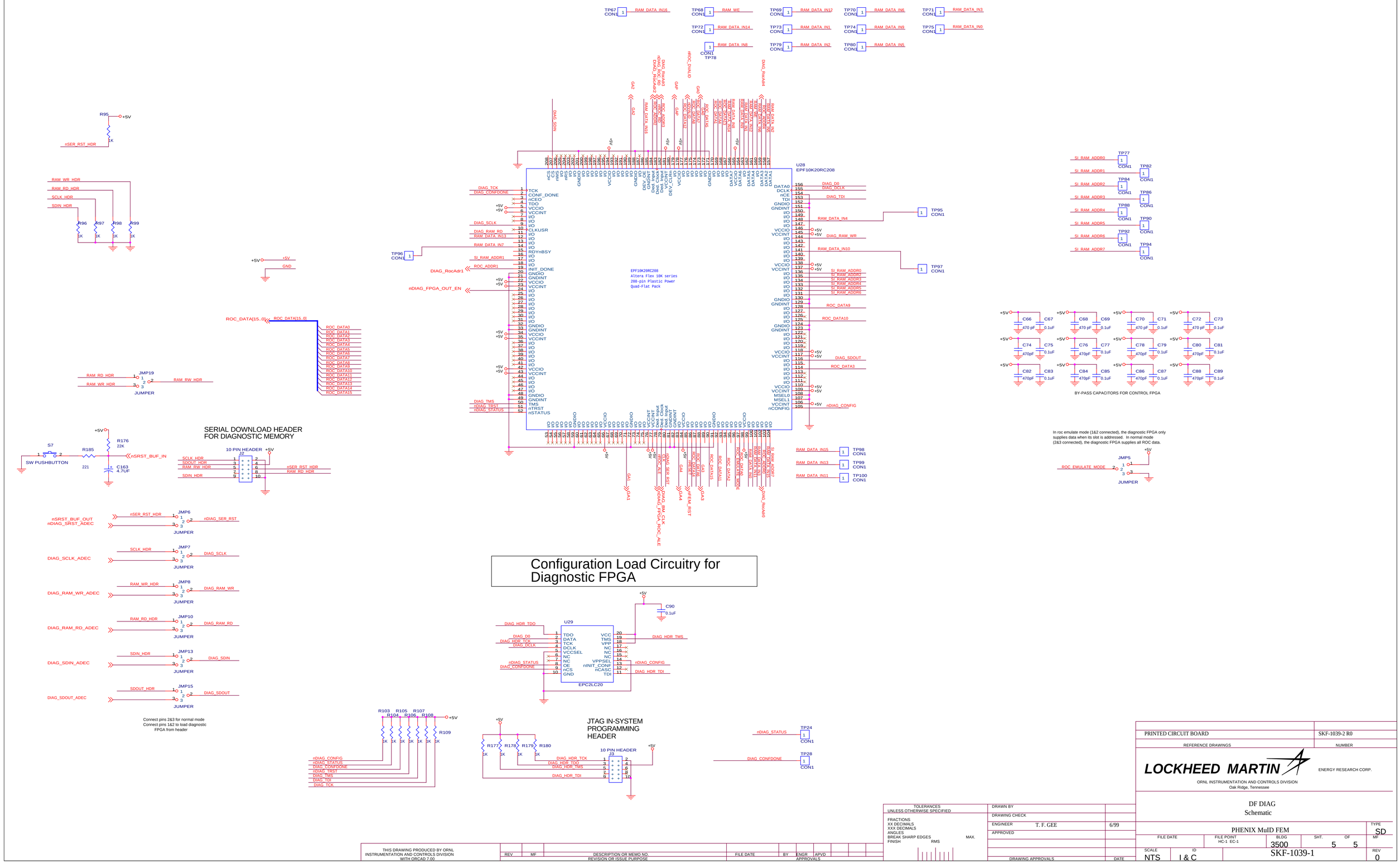
REV	MF	DESCRIPTION OR MEMO NO. REVISION OR ISSUE PURPOSE	FILE DATE	BY	ENGR	APVD
					APPROVALS	


Configuration Load Circuitry for Diagnostic FPGA
U28
EPF10K20RC208
EPF10K20RC208
Altera Flex 10K series
208-pin Plastic Power
Quad-Flat Pack
SERIAL DOWNLOAD HEADER FOR DIAGNOSTIC MEMORY
10 PIN HEADER
JTAG IN-SYSTEM PROGRAMMING HEADER
10 PIN HEADER
U29
EPC2LC20
BY-PASS CAPACITORS FOR CONTROL FPGA
In roc emulate mode (1&2 connected), the diagnostic FPGA only supplies data when its slot is addressed. In normal mode (2&3 connected), the diagnostic FPGA supplies all ROC data.
Connect pins 2&3 for normal mode
Connect pins 1&2 to load diagnostic FPGA from header
SW PUSHBUTTON
JUMPER
PRINTED CIRCUIT BOARD
SKF-1039-2 R0
REFERENCE DRAWINGS
NUMBER
LOCKHEED MARTIN
ENERGY RESEARCH CORP.
ORNL INSTRUMENTATION AND CONTROLS DIVISION
Oak Ridge, Tennessee
DF DIAG
Schematic
PHENIX MuID FEM
TYPE
SD
FILE DATE
FILE POINT
HC-1 EC-1
BLDG
3500
SHT.
5
OF
5
MF
SCALE
NTS
ID
I & C
SKF-1039-1
REV
0
TOLERANCES
UNLESS OTHERWISE SPECIFIED
FRACTIONS
XX DECIMALS
XXX DECIMALS
ANGLES
BREAK SHARP EDGES
FINISH
RMS
MAX.
DRAWN BY
DRAWING CHECK
ENGINEER
T. F. GEE
6/99
APPROVED
DRAWING APPROVALS
DATE
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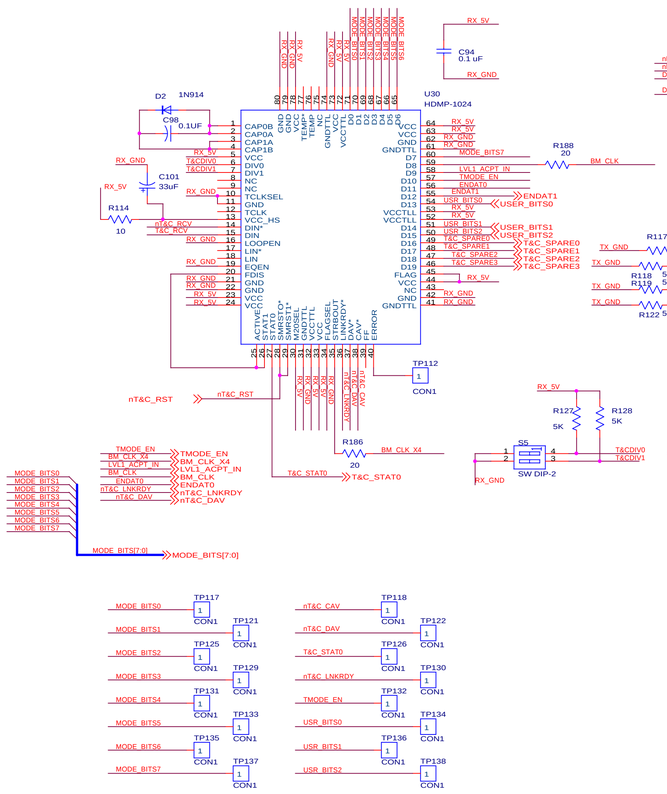
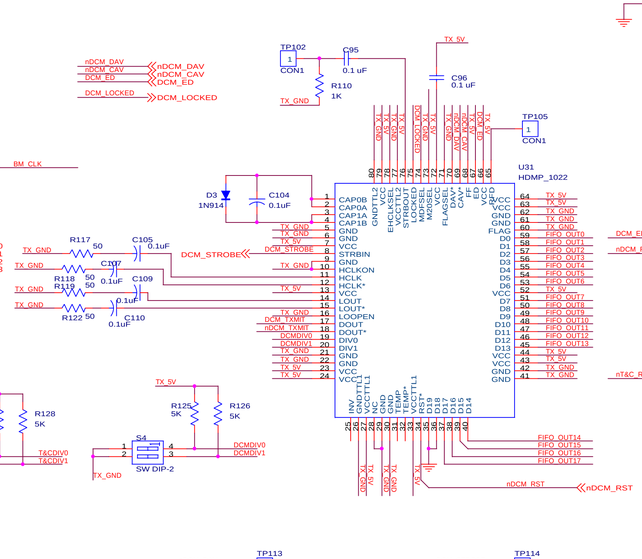
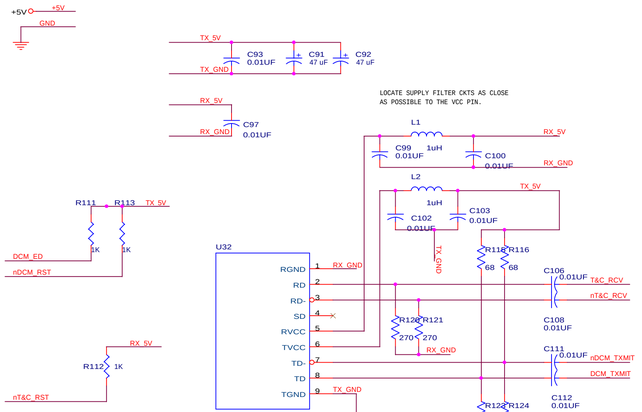
MF
DESCRIPTION OR MEMO NO.
REVISION OR ISSUE PURPOSE
FILE DATE
BY
ENGR
APVD
APPROVALS

TIMING and CONTROL GLINK

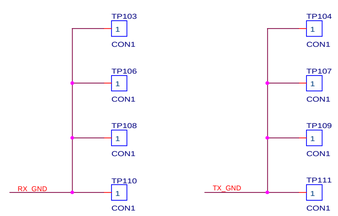


DCM GLINK

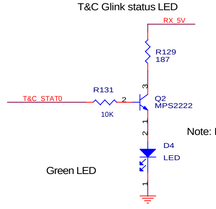




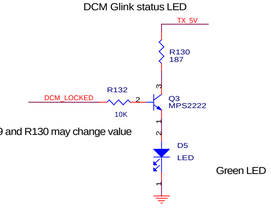
Ground Test Points



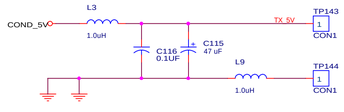
T&C Glink status LED

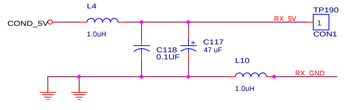


DCM Glink status LED



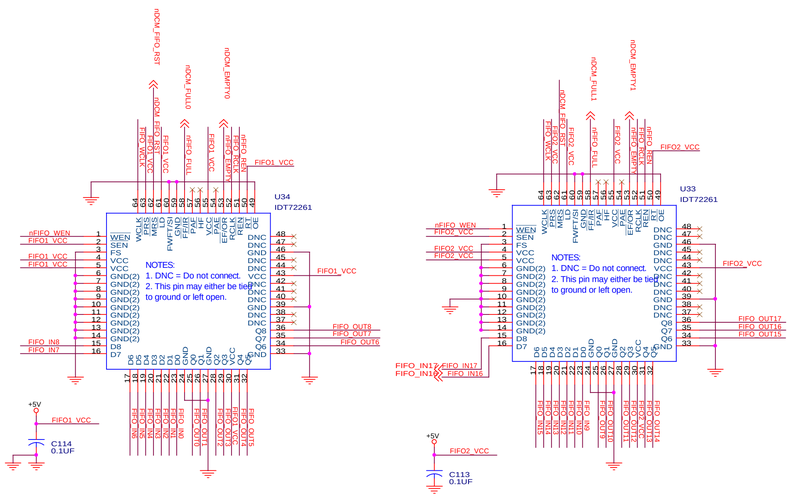
Note: R129 and R130 may change value





CONTROL FROM HEAP MANAGER

DCM Data FIFOs



PRINTED CIRCUIT BOARD	SKF-1039-2 R0
REFERENCE DRAWINGS	NUMBER

LOCKHEED MARTIN — ENERGY RESEARCH CORP.

ORNL INSTRUMENTATION AND CONTROLS DIVISION
Oak Ridge, Tennessee

GLINKs
Schematic

PHENIX MuID FEM — TYPE: SD

FILE DATE	FILE POINT	BLDG	SHT.	OF	MF
	HC-1 EC-1	3500	3	5	

SCALE	ID		REV
NTS	I & C	SKF-1039-1	0

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS
XX DECIMALS
XXX DECIMALS
ANGLES
BREAK SHARP EDGES MAX.
FINISH RMS

DRAWN BY		
DRAWING CHECK		
ENGINEER	T. F. GEE	6/99
APPROVED		
DRAWING APPROVALS		DATE

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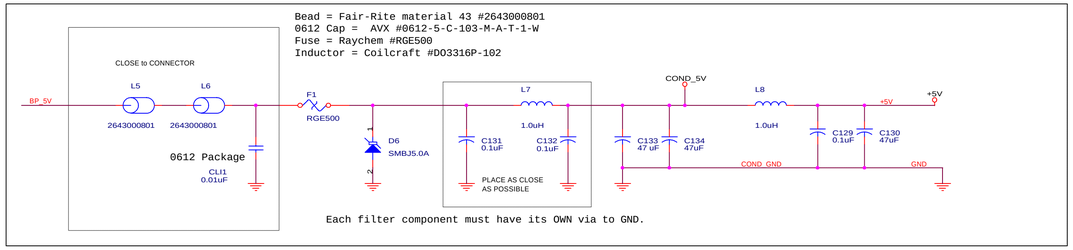
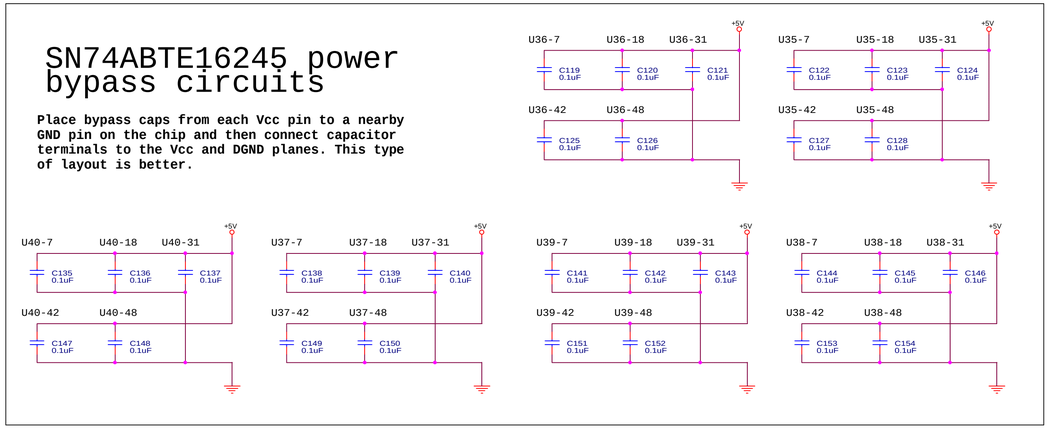
REV	MF	DESCRIPTION OR MEMO NO. / REVISION OR ISSUE PURPOSE	FILE DATE	BY	ENGR	APVD

Digital Power Conditioning

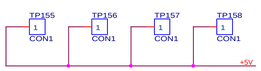


SN74ABTE16245 power bypass circuits

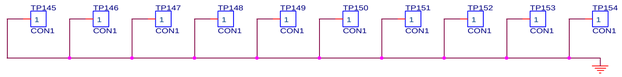
Place bypass caps from each Vcc pin to a nearby GND pin on the chip and then connect capacitor terminals to the Vcc and DGND planes. This type of layout is better.



Power Test Points



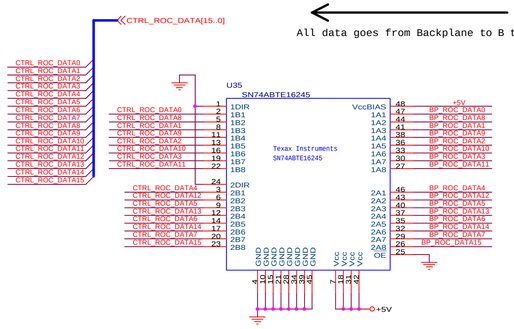
Ground Test Points

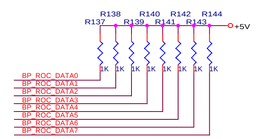


Make traces from Backplane Connector about 1 inch long. This means that the chips have to be fairly close to the connector.

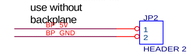
VME Bus Receivers

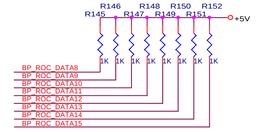
All data goes from Backplane to B to A.

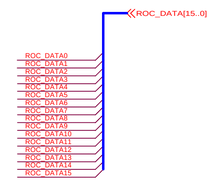




Power connector for use without backplane





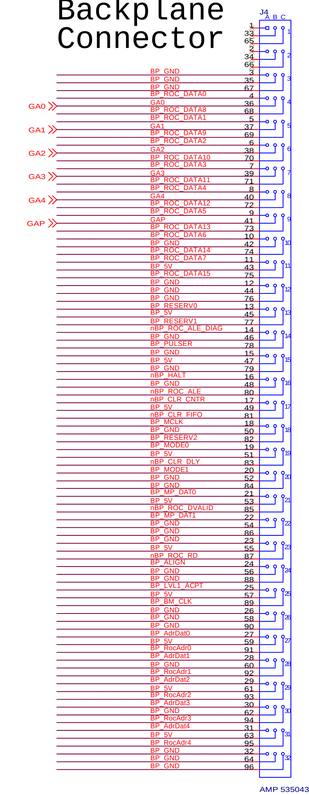


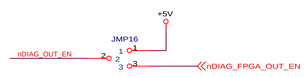
Make traces from Backplane Connector about 1 inch long. This means that the chips have to be fairly close to the connector.

VME Bus Drivers

All data goes from B to A to Backplane.

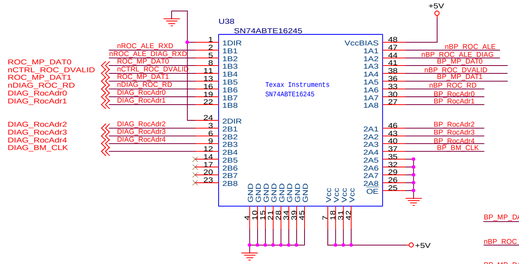
Digital Backplane Connector

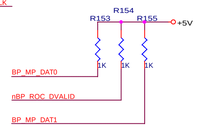


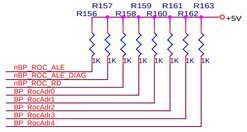


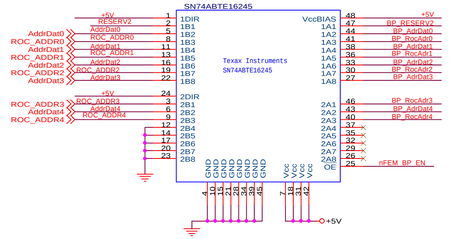
Place jumper across the following pairs to achieve the following action:
1&2) disable diagnostic output onto backplane
2&3) enable diagnostic output in diagnostic mode
- normal mode

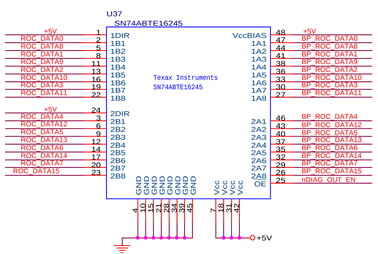
Place jumper across the following pairs to achieve the following action:
1&2) make diagnostic FPGA active during normal ROC read operations. This may be used in future mode in which a FEM is used as a pseudo-ROC for testing
2&3) enable diagnostic output in diagnostic mode (diagnostic data may be read by control FPGA on this board or another FEM board) - Normal mode

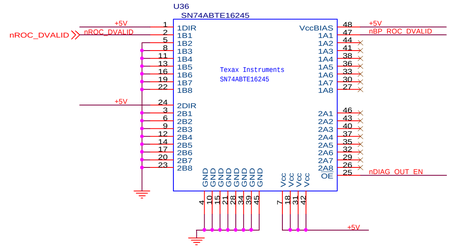


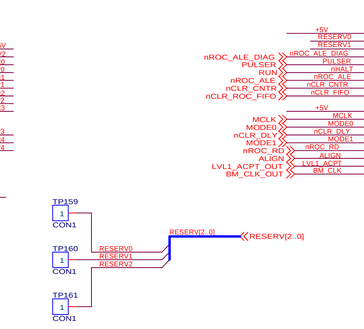


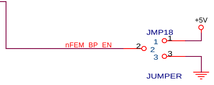












Place jumper across the following pairs to achieve the following action:
1&2) disable backplane outputs (use when this when this FEM is a slave to another FEM on the backplane. This slave FEM will only produce ROC diagnostic data.)
2&3) enable backplane outputs - Normal mode

PRINTED CIRCUIT BOARD	SKF-1039-2 R0
REFERENCE DRAWINGS	NUMBER

LOCKHEED MARTIN — ENERGY RESEARCH CORP.
ORNL INSTRUMENTATION AND CONTROLS DIVISION
Oak Ridge, Tennessee

BACKPLANE
Schematic

PHENIX MuID FEM				TYPE SD
FILE DATE	FILE POINT HC-1 EC-1	BLDG 3500	SHT. 4	OF 5
SCALE NTS	ID I & C	SKF-1039-1		REV 0

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS
XX DECIMALS
XXX DECIMALS
ANGLES
BREAK SHARP EDGES MAX.
FINISH RMS

DRAWN BY		
DRAWING CHECK		
ENGINEER	T. F. GEE	6/99
APPROVED		
DRAWING APPROVALS		DATE

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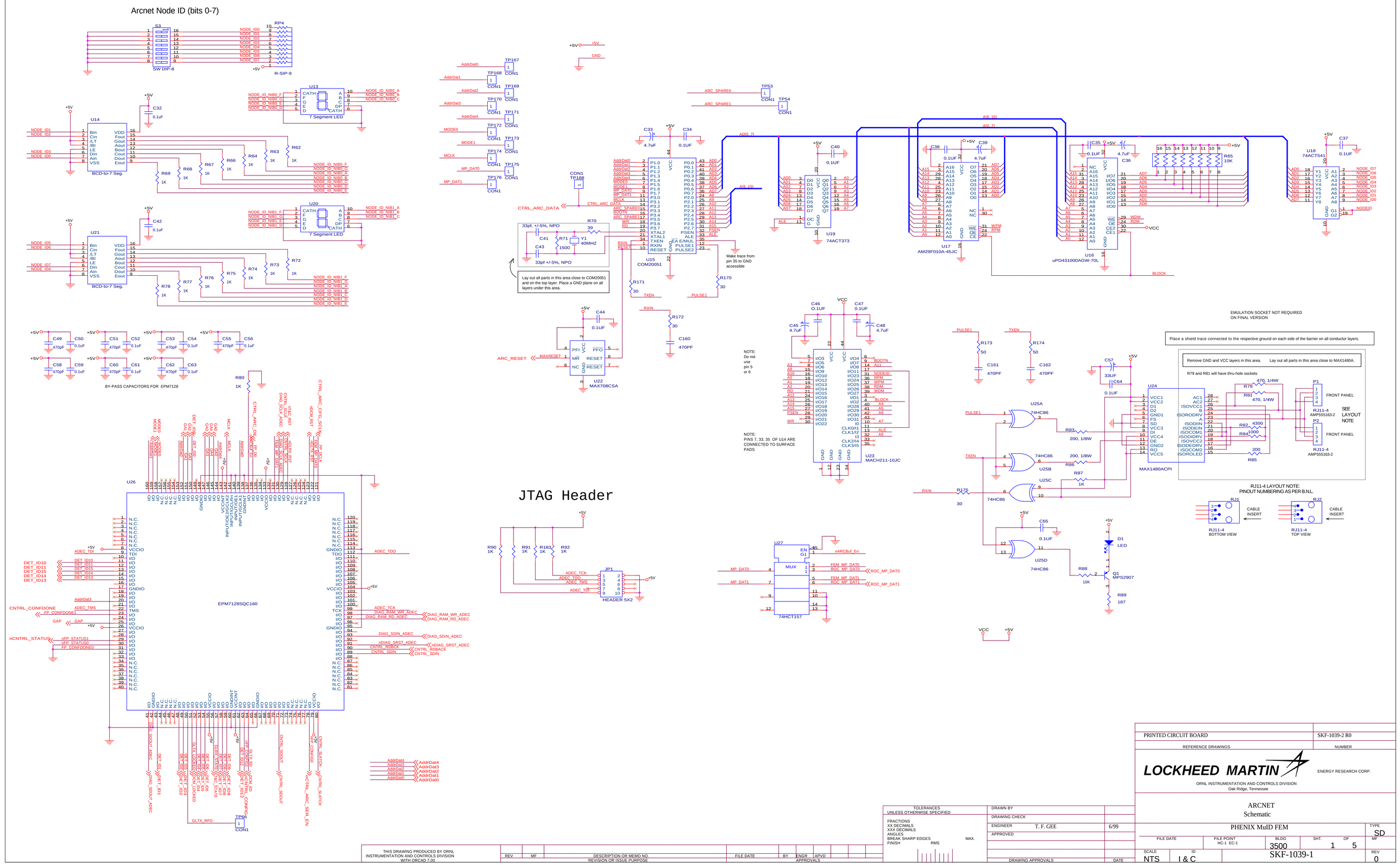
REV	MF	DESCRIPTION OR MEMO NO. / REVISION OR ISSUE PURPOSE	FILE DATE	BY	ENGR	APVD


Arcnet Node ID (bits 0-7)
JTAG Header
EMULATION SOCKET NOT REQUIRED ON FINAL VERSION
Place a shield trace connected to the respective ground on each side of the barrier on all conductor layers.
Remove GND and VCC layers in this area.
Lay out all parts in this area close to MAX1480A.
R79 and R81 will have thru-hole sockets
Lay out all parts in this area close to COM20051 and on the top layer. Place a GND plane on all layers under this area.
Make trace from pin 35 to GND accessible
NOTE: Do not use pin 5 or 6
NOTE: PINS 7, 33, 35 OF U14 ARE CONNECTED TO SURFACE PADS
BY-PASS CAPACITORS FOR EPM7128
RJ11-4 LAYOUT NOTE: PINOUT NUMBERING AS PER B.N.L
FRONT PANEL
SEE LAYOUT NOTE
PRINTED CIRCUIT BOARD
SKF-1039-2 R0
LOCKHEED MARTIN
ENERGY RESEARCH CORP.
ORNL INSTRUMENTATION AND CONTROLS DIVISION
Oak Ridge, Tennessee
ARCNET
Schematic
PHENIX MuID FEM
SKF-1039-1
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