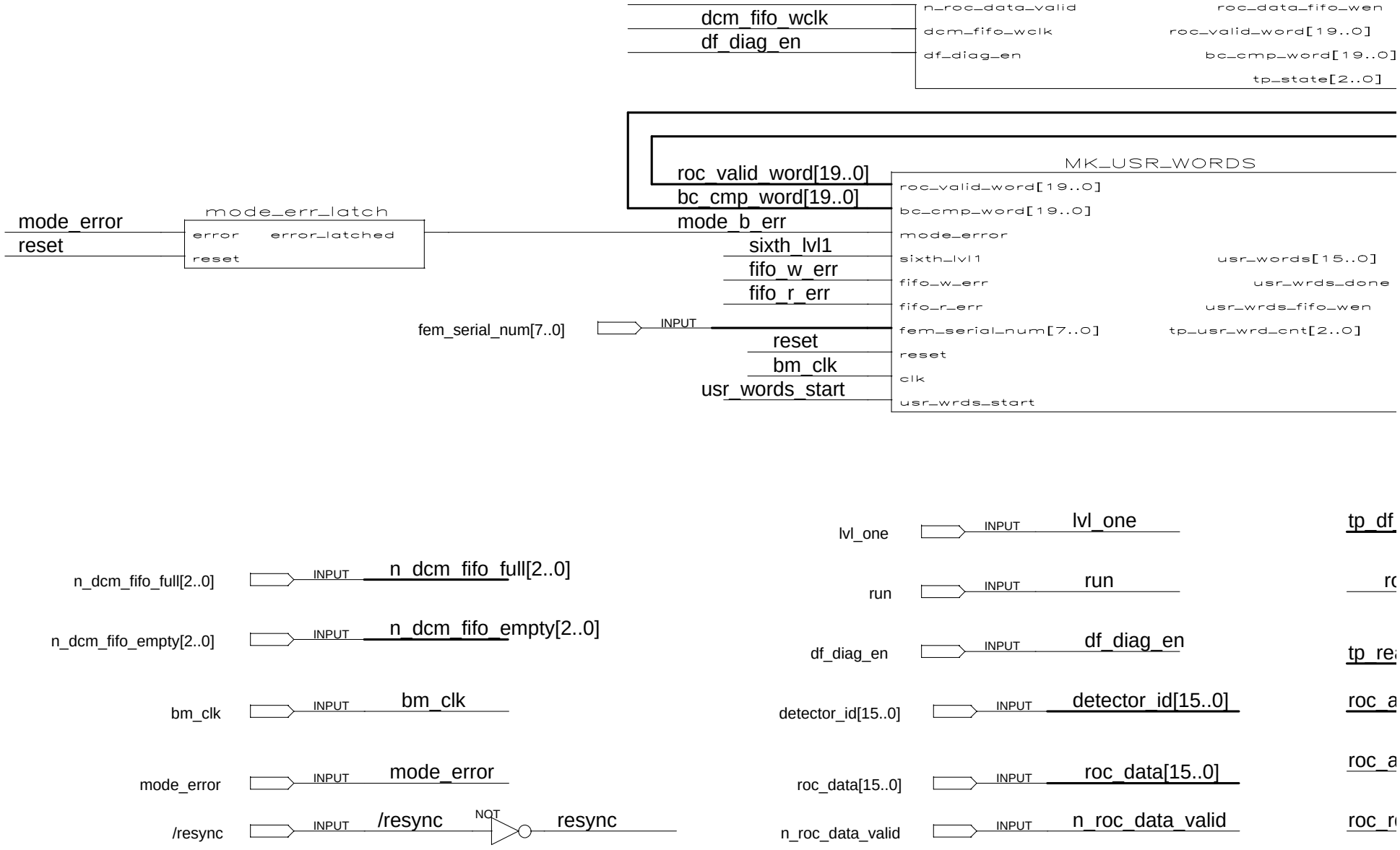
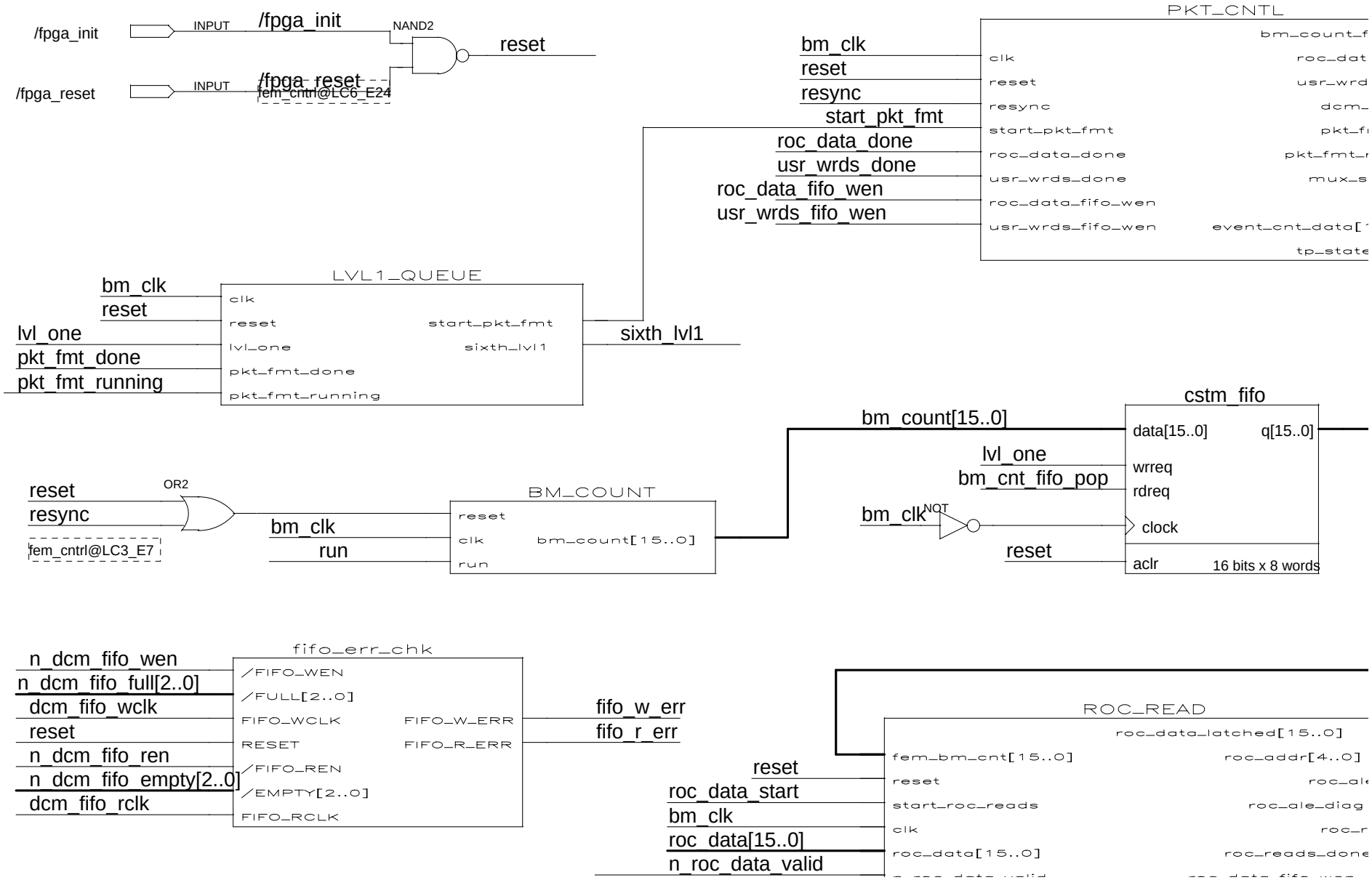
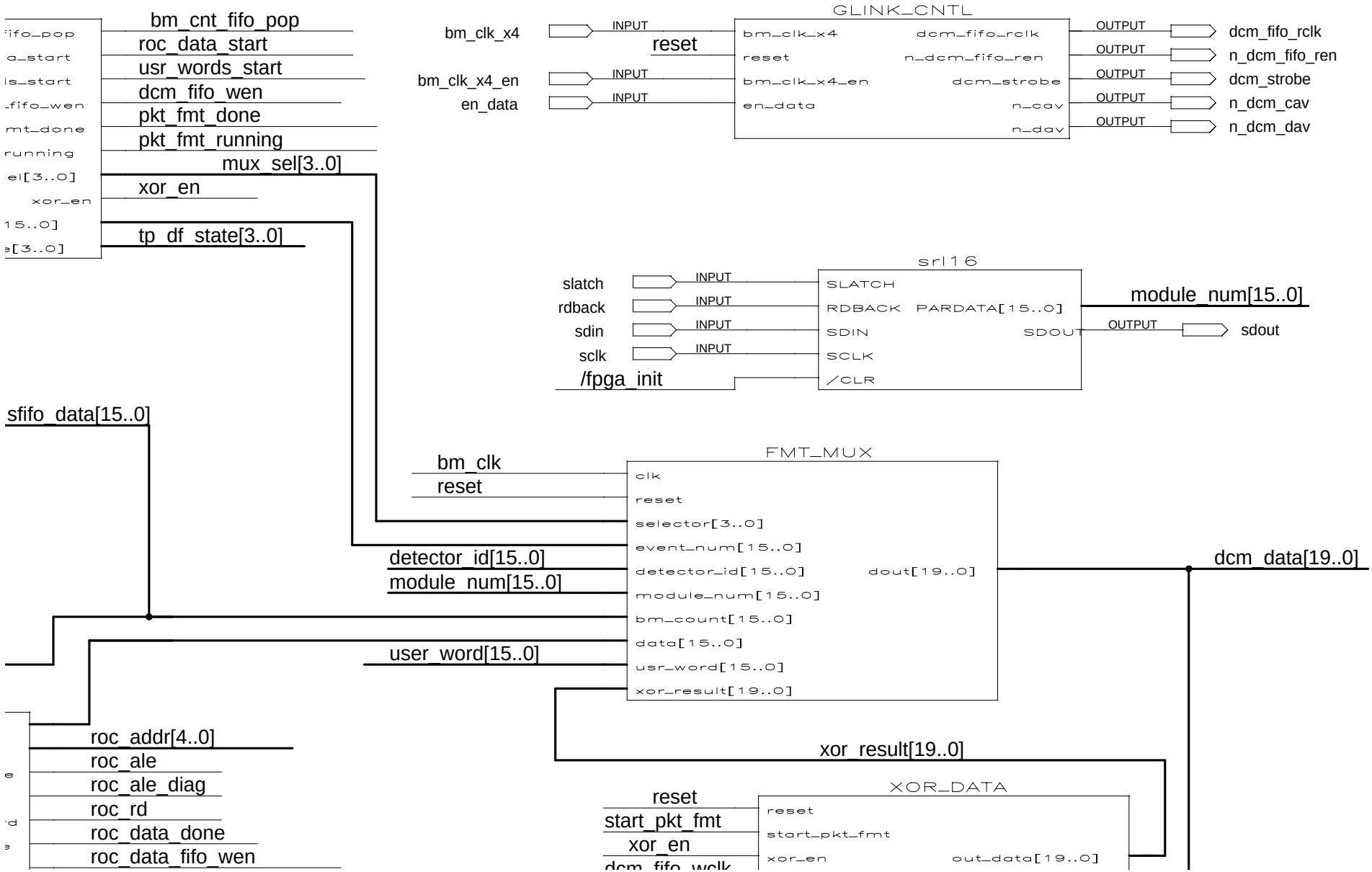
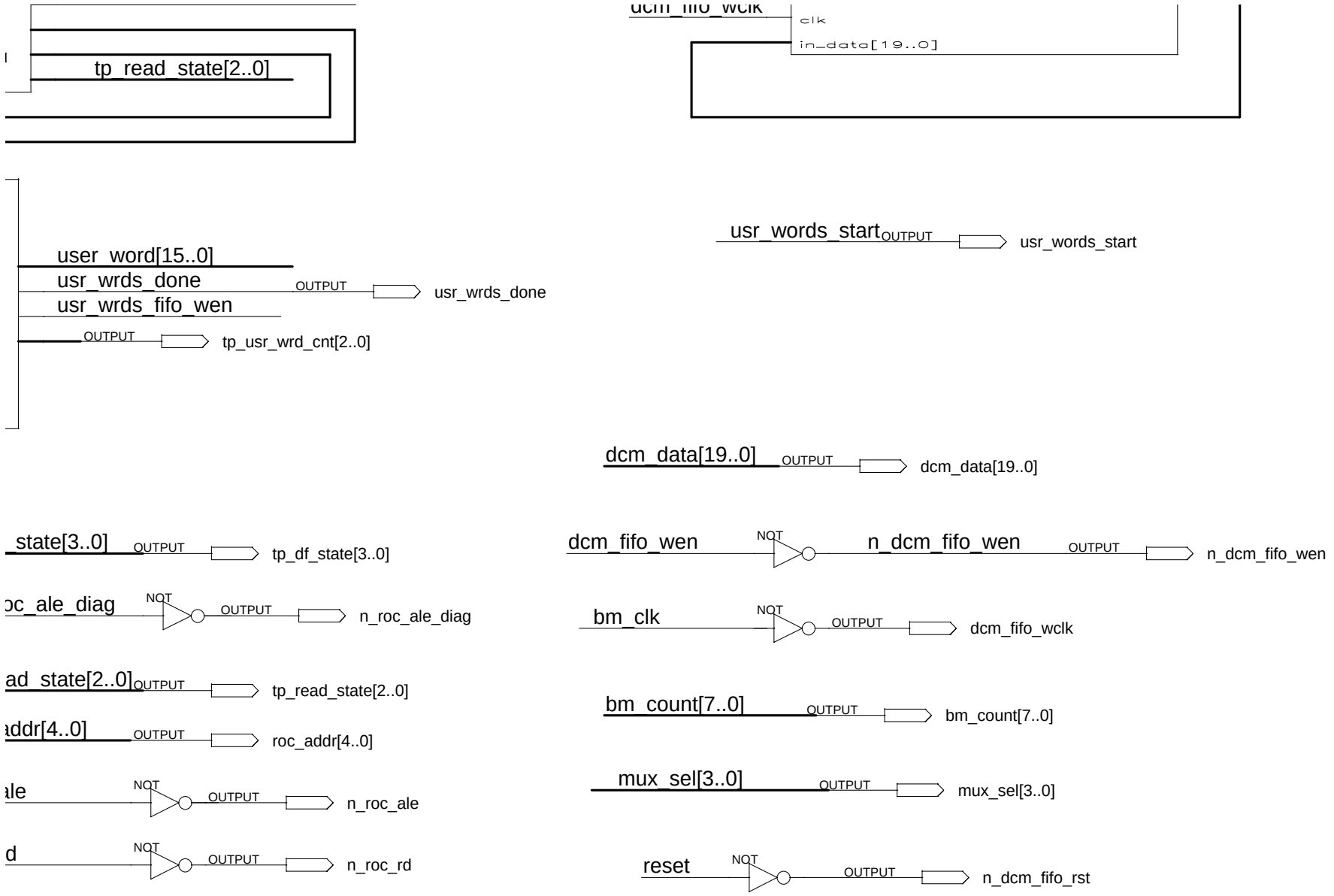

dcm_fifo_wclk
df_diag_en
n_roc_data_valid
dcm_fifo_wclk
df_diag_en
roc_data_fifo_wen
roc_valid_word[19..0]
bc_cmp_word[19..0]
tp_state[2..0]
MK_USR_WORDS
roc_valid_word[19..0]
bc_cmp_word[19..0]
mode_error
sixth_lvl1
fifo_w_err
fifo_r_err
fem_serial_num[7..0]
reset
clk
usr_wrds_start
usr_words[15..0]
usr_wrds_done
usr_wrds_fifo_wen
tp_usr_wrd_cnt[2..0]
mode_error
reset
mode_err_latch
error
error_latched
reset
roc_valid_word[19..0]
bc_cmp_word[19..0]
mode_b_err
sixth_lvl1
fifo_w_err
fifo_r_err
fem_serial_num[7..0]
reset
bm_clk
usr_words_start
INPUT
lvl_one
INPUT
lvl_one
tp_df
n_dcm_fifo_full[2..0]
INPUT
n_dcm_fifo_full[2..0]
run
INPUT
run
n_dcm_fifo_empty[2..0]
INPUT
n_dcm_fifo_empty[2..0]
df_diag_en
INPUT
df_diag_en
tp_rea
bm_clk
INPUT
bm_clk
detector_id[15..0]
INPUT
detector_id[15..0]
roc_a
mode_error
INPUT
mode_error
roc_data[15..0]
INPUT
roc_data[15..0]
roc_a
/resync
INPUT
/resync
NOT
resync
n_roc_data_valid
INPUT
n_roc_data_valid
roc_r


/fpga_init
INPUT
/fpga_init
NAND2
reset
/fpga_reset
INPUT
/fpga_reset
fem_cntrl@LC6_E24
PKT_CNTL
bm_clk
reset
resync
start_pkt_fmt
roc_data_done
usr_wrds_done
roc_data_fifo_wen
usr_wrds_fifo_wen
clk
reset
resync
start_pkt_fmt
roc_data_done
usr_wrds_done
roc_data_fifo_wen
usr_wrds_fifo_wen
LVL1_QUEUE
bm_clk
reset
lvl_one
pkt_fmt_done
pkt_fmt_running
clk
reset
lvl_one
pkt_fmt_done
pkt_fmt_running
start_pkt_fmt
sixth_lvl1
sixth_lvl1
cstm_fifo
bm_count[15..0]
data[15..0]
q[15..0]
lvl_one
bm_cnt_fifo_pop
wrreq
rdreq
bm_clk
NOT
clock
reset
aclr
16 bits x 8 words
reset
resync
OR2
fem_cntrl@LC3_E7
bm_clk
run
BM_COUNT
reset
clk
run
bm_count[15..0]
n_dcm_fifo_wen
n_dcm_fifo_full[2..0]
dcm_fifo_wclk
reset
n_dcm_fifo_ren
n_dcm_fifo_empty[2..0]
dcm_fifo_rclk
fifo_err_chk
/FIFO_WEN
/FULL[2..0]
FIFO_WCLK
RESET
/FIFO_REN
/EMPTY[2..0]
FIFO_RCLK
FIFO_W_ERR
FIFO_R_ERR
fifo_w_err
fifo_r_err
ROC_READ
reset
roc_data_start
bm_clk
roc_data[15..0]
n_roc_data_valid
fem_bm_cnt[15..0]
reset
start_roc_reads
clk
roc_data[15..0]
roc_data_latched[15..0]
roc_addr[4..0]
roc_ale_diag
roc_reads_done


bm_cnt_fifo_pop
roc_data_start
usr_words_start
dcm_fifo_wen
pkt_fmt_done
pkt_fmt_running
mux_sel[3..0]
xor_en
tp_df_state[3..0]
GLINK_CNTL
bm_clk_x4
reset
bm_clk_x4_en
en_data
INPUT
bm_clk_x4
reset
bm_clk_x4_en
en_data
dcm_fifo_rclk
n_dcm_fifo_ren
dcm_strobe
n_cav
n_dav
OUTPUT
dcm_fifo_rclk
n_dcm_fifo_ren
dcm_strobe
n_dcm_cav
n_dcm_dav
srl16
slatch
rdback
sdin
sclk
/fpga_init
SLATCH
RDBACK
SDIN
SCLK
/CLR
PARDATA[15..0]
SDOUT
module_num[15..0]
sdout
sfifo_data[15..0]
FMT_MUX
bm_clk
reset
clk
reset
selector[3..0]
event_num[15..0]
detector_id[15..0]
module_num[15..0]
bm_count[15..0]
data[15..0]
usr_word[15..0]
xor_result[19..0]
dout[19..0]
dcm_data[19..0]
user_word[15..0]
roc_addr[4..0]
roc_ale
roc_ale_diag
roc_rd
roc_data_done
roc_data_fifo_wen
xor_result[19..0]
XOR_DATA
reset
start_pkt_fmt
xor_en
out_data[19..0]


tp_read_state[2..0]
dcm_fifo_wclk
clk
in_data[19..0]
usr_words_start
OUTPUT
usr_words_start
user_word[15..0]
usr_wrds_done
OUTPUT
usr_wrds_done
usr_wrds_fifo_wen
OUTPUT
tp_usr_wrd_cnt[2..0]
dcm_data[19..0]
OUTPUT
dcm_data[19..0]
_state[3..0]
OUTPUT
tp_df_state[3..0]
dcm_fifo_wen
NOT
n_dcm_fifo_wen
OUTPUT
n_dcm_fifo_wen
oc_ale_diag
NOT
OUTPUT
n_roc_ale_diag
bm_clk
NOT
OUTPUT
dcm_fifo_wclk
ad_state[2..0]
OUTPUT
tp_read_state[2..0]
bm_count[7..0]
OUTPUT
bm_count[7..0]
addr[4..0]
OUTPUT
roc_addr[4..0]
mux_sel[3..0]
OUTPUT
mux_sel[3..0]
ale
NOT
OUTPUT
n_roc_ale
d
NOT
OUTPUT
n_roc_rd
reset
NOT
OUTPUT
n_dcm_fifo_rst