

DRAFT
MuID FEM Mode Control Design Document
 JSHicks

Inputs: From T&C Glink (~40 Mhz)

BIT #	Signal	
0	Mode Bit 0	
1	Mode Bit 1	
2	Mode Bit 2	
3	Mode Bit 3	
4	Mode Bit 4	
5	Mode Bit 5	
6	Mode Bit 6	
7	Mode Bit 7	(Alignment Bit)
8	Beam Clk (9.4Mhz)	
9	LVL1 Accept	
10	Timing Mode Enable	
11	EnDat0	
12	EnDat1	
13	User Bit 0	(0 0 1 – Reset ARCNET)
14	User Bit 1	(0 1 0 – FEM Self-test)
15	User Bit 2	
16	Endat2	
17	Endat3	
18	Reserved	
19	Reserved	

Other Inputs:

/CLR	Sets all outputs to low state - Halt state
/DAV	Data Available from GLINK
/LINKRDY	GLINK signal indicating locked operation
STAT0	GLINK signal indicating correct state machine recovery of the clk strobe

Outputs:

MODE_B_ERR
 B_CLK
 RUN
 CLR_CNTR
 CLR_FIFO
 CLR_DLY
 S_FUN1
 S_FUN2
 PULSER
 ALIGN
 LVL1_ACPT
 EN_DAT
 FEM_RST
 FEM_SELF_TEST
 ARCNET_RST

Design assumptions:

DAV* and LINKRDY* are used to determine if the GLINK is finished with its startup procedure and running in locked mode with valid data.

STAT0 is used to gate the Beam-Clock mode bit.

The Beam-Clock, B_CLK, mode bit is used to clock the mode-bit control logic. It is also assumed that the mode bit data D0-D7 and D9-D19 change on the rising edge of the B_CLK data bit D8. The input latch for mode control accepts the data from the GLINK and latches it on the falling edge of B_CLK. This ensures stable data for input to the mode-bit decoder block. Data is processed by the decoder asynchronously and then re-synchronized with B_CLK at the output register, which is triggered on the rising edge of B_CLK.

MODES of Operation:

Modes should be decoded and used only if Mode Enable is high. Else the FEM should be placed in the **HALT** state (RUN low state). Power up in the Halt state.

Run

Run is for normal operation, FEM is running & collecting data. Default to RUN mode when invalid mode combinations are received.

HALT (complement of RUN)

Halt is used to Stop all operations including data formatting & transmission to the DCM. This should allow a new serial data stream from ARCnet to be loaded without problems - for FEM configuration, monitoring and diagnostics.

Initialize Reset (CLR_CNTR, CLR_FIFO)

The Initialization Reset is used to place the FRM in an initialized state. This is the same state that the FEM should be in at power concerning counters and data FIFOs. All counters, FIFOs, etc. are reset to zero. Configure information should be saved. Data is lost – even LVL1 qualified data is lost if it has not been completely sent.

Resysnc Reset (CLR_CNTR)

Reset the BCLK & Event counters. This should take effect at the next valid LVL1_ACPT to avoid data loss.

Special Reset

Special Reset provides sub-system specific reset options. This function may require multiple beam clocks for execution. *For this and other commands requiring more than one beam clk cycle for execution, the scheduler should output the commands the appropriate number of beam clock cycles.*

Analog FE & FIFO are also re-settable & can have separate cmds (special reset group Listed as S_FUN1 and S_FUN2 for MuID – not yet defined).

Table 1.

mB7	mB6	mB5	mB4	mB3	mB2	mB1	mB0	
0	0	0	0	0	0	0	0	HALT
0	0	0	1	0	0	0	0	RUN Assuming D10 = 1 (Mode Enable)
0	0	0	1	0	0	0	1	Resync Reset BCLK & Event counters LVL1_ACPT
0	0	0	1	0	0	1	0	Init Reset Zero all counters May Flush Data
0	0	0	1	0	0	1	1	Special Reset - (Delay MUX outputs)
0	0	0	1	0	1	0	0	Special Function - 1 (not implemented yet for MuID)
0	0	0	1	1	0	0	0	Special Function - 2 (not implemented yet for MuID)
0	0	0	1	1	1	0	0	Special Function - 3 (Fire local test Pulser)
	X	X						Extra bits – No current assignment
1	0	0	1	0	0	0	0	Alignment Bit
X	X	X	X	X	X	X	X	RUN

USER_BITS	
0 0 0	No function
0 0 1	Arcnet Reset
0 1 0	FEM Self Test
X X X	No function