



# **PHENIX TRIGGER SYSTEM**

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# Short Trigger Systems History

## Self-triggering devices

(Geiger counter, bubble chamber, emulsion)



## Level 0 Trigger

(some other device signals that event has happened)



## Blue logic

(combination of devices defines trigger condition)



## Level 1 Trigger. Event rejection

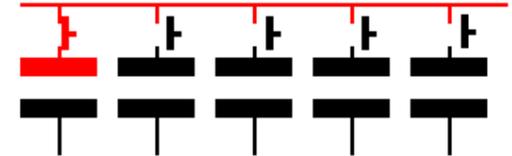
(Event processing is started by Level 0 trigger, then Level 1 trigger issues fast clear if event is not good)



# Short Trigger History (continued)

## Level 1 Trigger. Analog Memory Units.

Signal samples are stored in analog memory units. On Level 1 trigger signal from corresponding unit is digitized.



**Level 1 Trigger electronics use FPGA** to make sophisticated pipelined signals preprocessing. Dead-time free procedure.

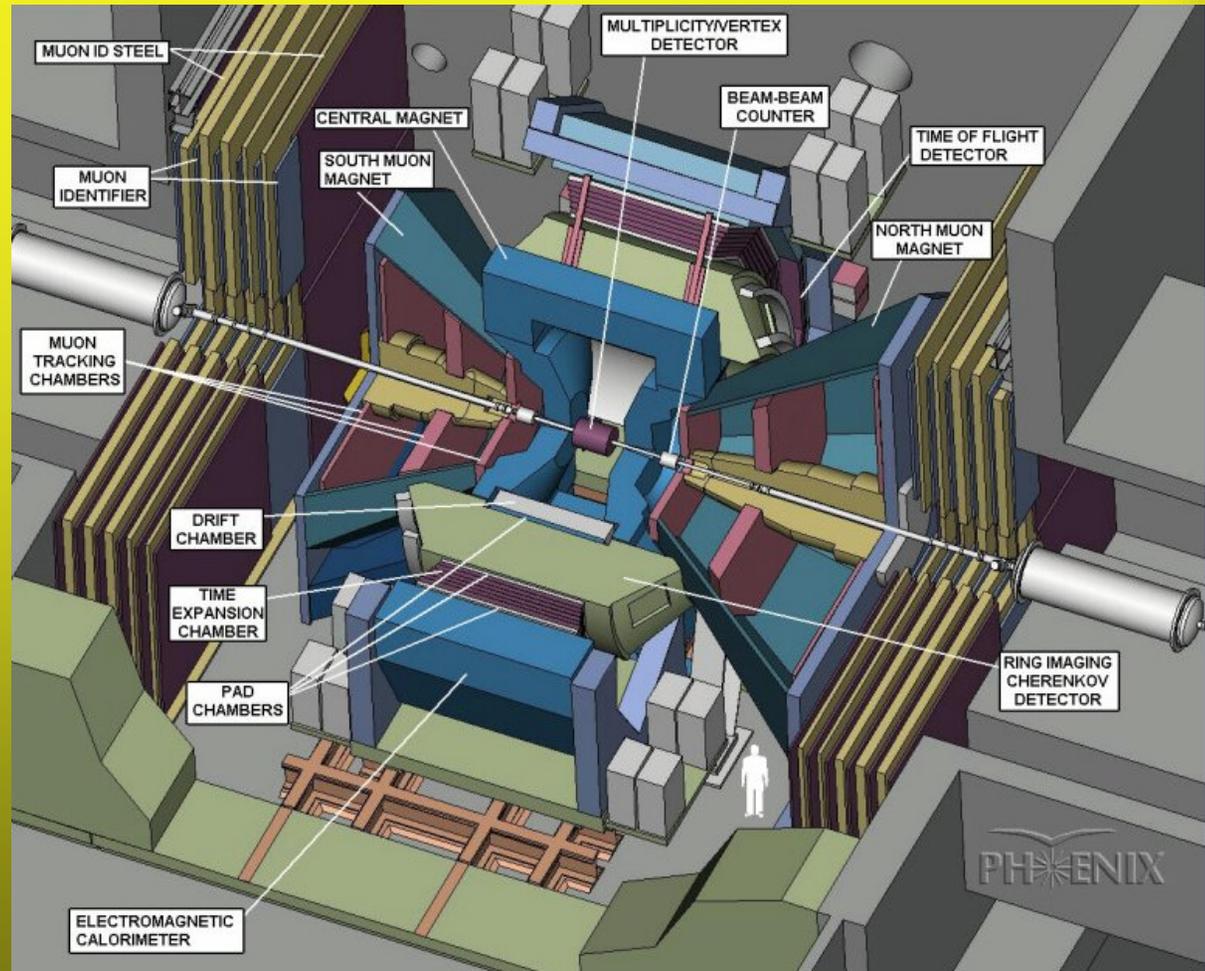


**Level 2 Trigger.** Fast software analysis of the data. Only worthy events are stored.



# PHENIX Subsystems

Today PHENIX consists of 14 subsystems. Each subsystem must be able to operate as part of PHENIX detector, working in sync with all other subsystems, and at the same time it must be able to make some specific measurements (calibration, time tuning, etc.) independently or as part of a smaller group of detectors.



# What we expected from the Trigger System

- **It must permit us to work independently with any combinations of detector subsystems.**
- **Be able to configure and deliver many different kinds of trigger signals.**
- **Must help us to enrich one kind of events (rare events) by reducing the rate of the other ones**
- **Must have no dead time**
- **Be able to record its data for each accepted event**
- **Trigger System must be easily configured**
- ✓ **Trigger System can handle up to 32 groups (partitions) of PHENIX “granules”**
- ✓ **In PHENIX Trigger System we can program up to 128 triggers**
- ✓ **Triggers scale down mechanism**
- ✓ **LL1s and GL1 are pipelined FPGA systems with programmed dead time**
- ✓ **Pipelined data stream with a buffer for 5 events**
- ✓ **Can be done by just clicking buttons on GL1 configuration GUI**

# Granules and Partitions

- Here is the main idea of this approach.

For example, before the Run some subsystem(s) would like to tune their detectors. They may like to work with a part of their detector (for example, only with Muon Identifier North Arm (MUID.N)), with a detector as a whole (MUID.N + MUID.S), or with a group of the detectors (MUID.N + MUID.S + MUTR.N + MUTR.S). So we have to be able to “disassemble” PHENIX into some small parts (we call them **Granules**) that are able to operate independently, and then to be able to combine some or all of those granules into independently operating groups (we call them **Partitions**). To better understand Granule/Partition conception of the PHENIX, try to imagine PHENIX as an object assembled out of kid’s LEGO bricks. The same way as in LEGO you may disassemble one shape down to individual bricks, and then reassemble different shape or shapes out of those bricks, with PHENIX you may disassemble detector into Granules and recombine them into Partitions.

The main LEGO law is as well applied to the PHENIX DAQ system: **in each taken moment each brick (Granule) may be constituent of only one shape (Partition), while one shape (Partition) may consist of any amount of bricks (Granules).**

The Global Level 1 (GL1) system defines the granules to partitions assignment, as well as triggers to partitions assignment.

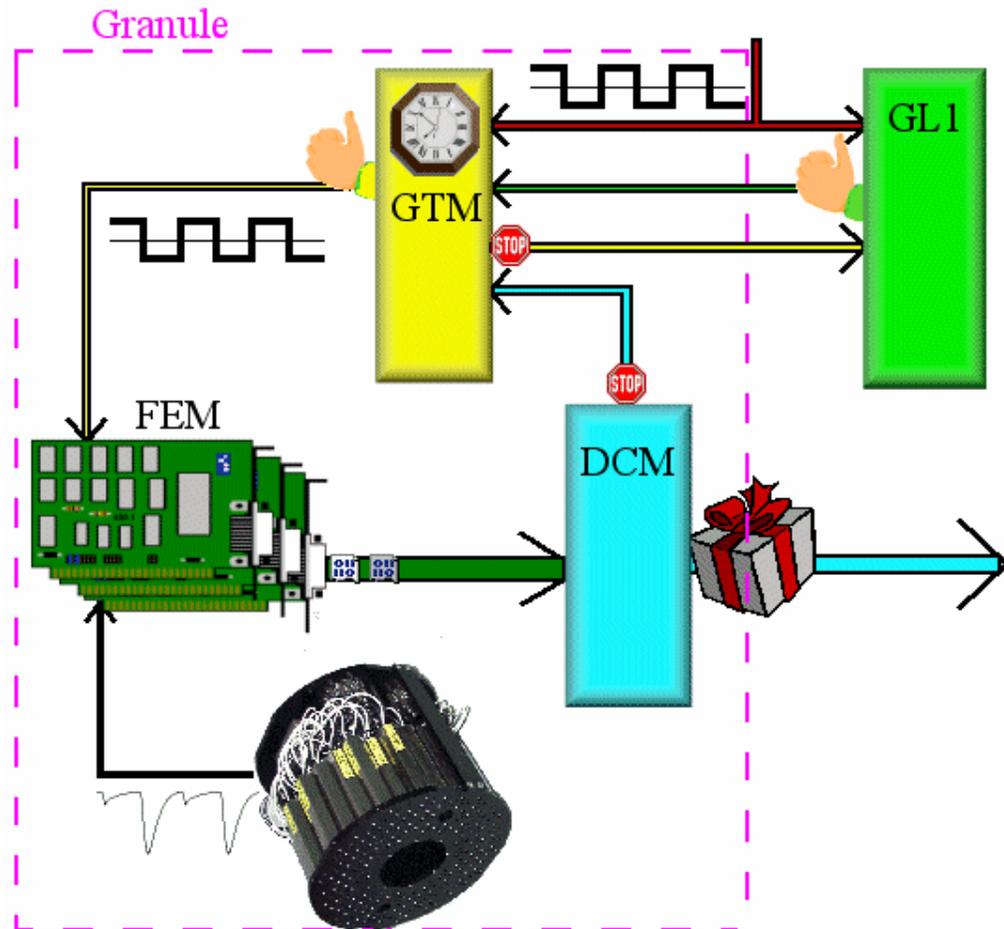


# Granules

- **Granule** is the minimal combination of DAQ hardware sufficient for data production.

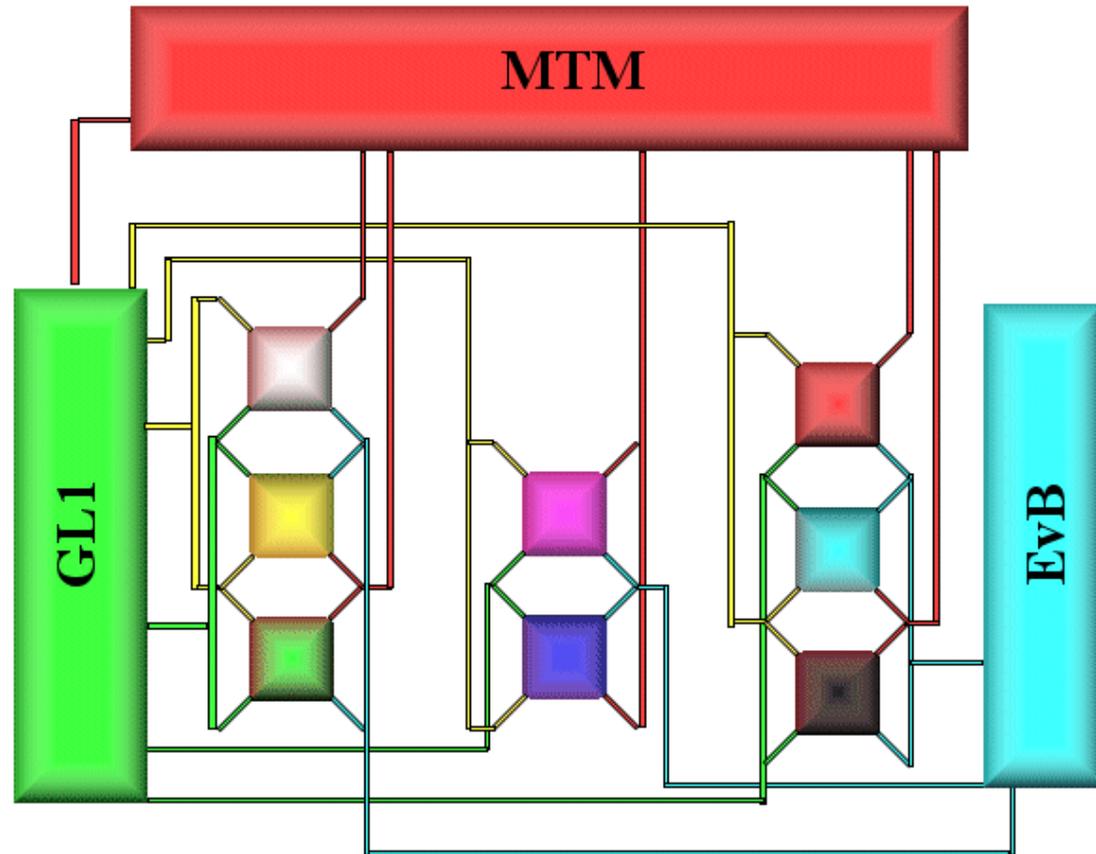
In PHENIX it consists of:

1. **F**ront **E**nd **M**odule(s)
2. **D**ata **C**ollection **M**odule
3. **G**ranule **T**iming **M**odule

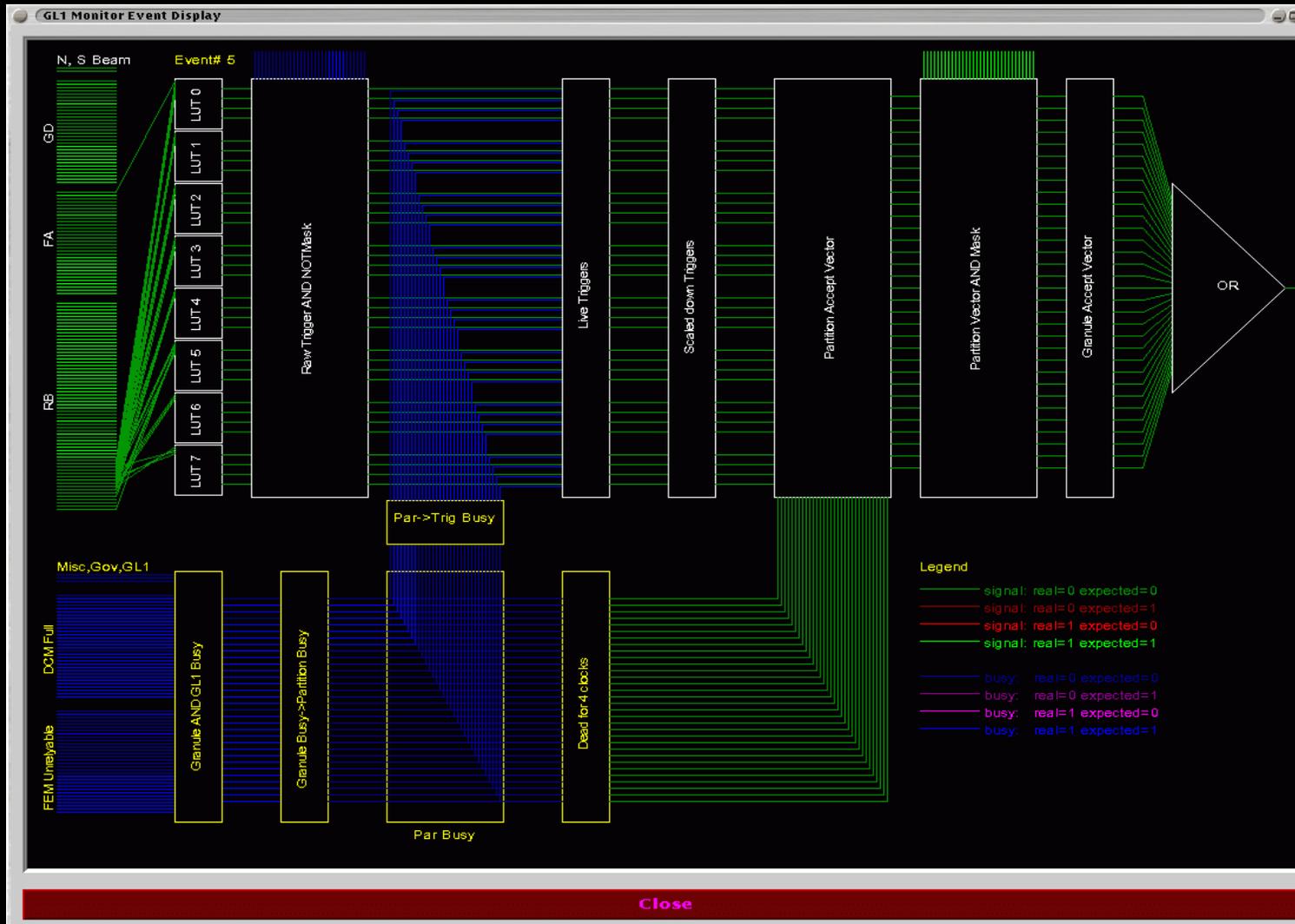


# Partitions

- **Partition** is the combination of the granules, and such group works as one unit.
- ✓ PHENIX may have up to 32 partitions that share 32 granules and up to 128 triggers.
- ✓ Partitions operate in parallel and independently of each other.
- ✓ All granules in partition have common triggers, busy signal, and their data are combined and are written into one file.
- ✓ All partitions configuration is fulfilled just by GUI program.



# Global Level 1 block diagram

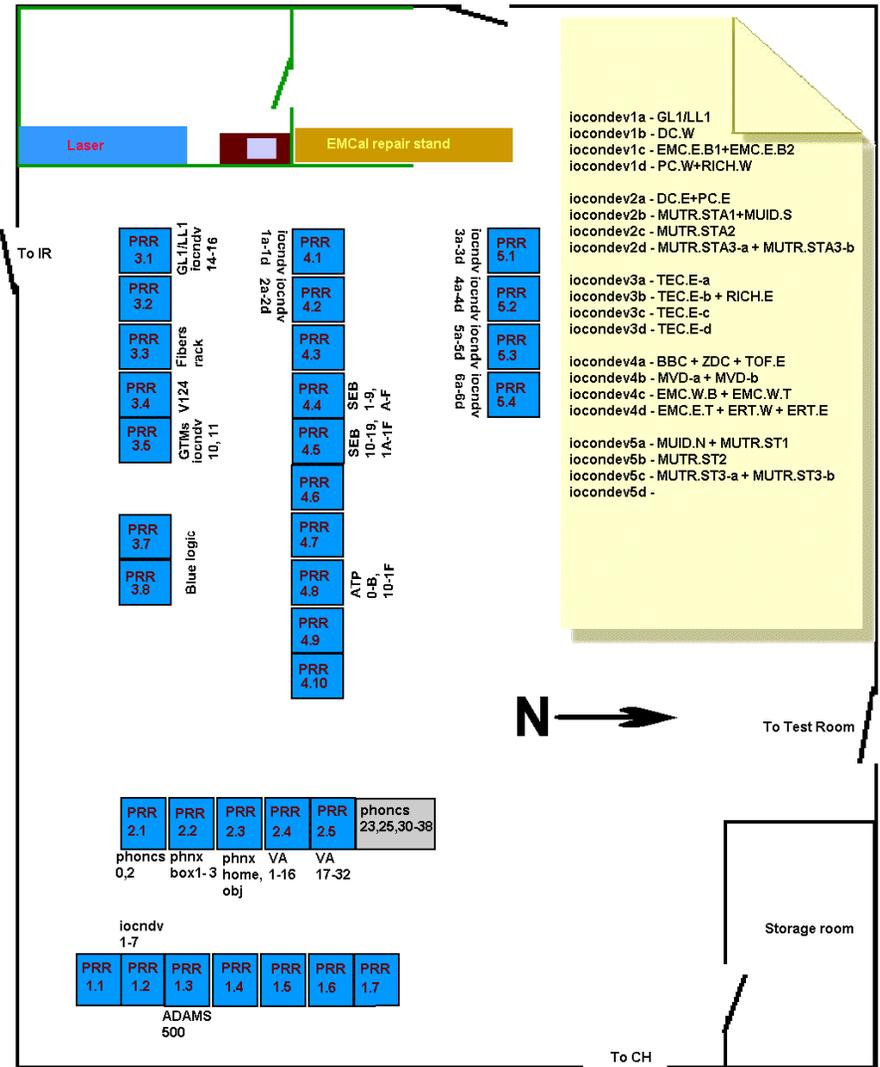


# DAQ electronics location

• Subsystem FEMs are located in Interaction Region (IR) at the vicinity of their detectors or directly on the detectors. All signals from and to the FEMs are transmitted through optical fibers.

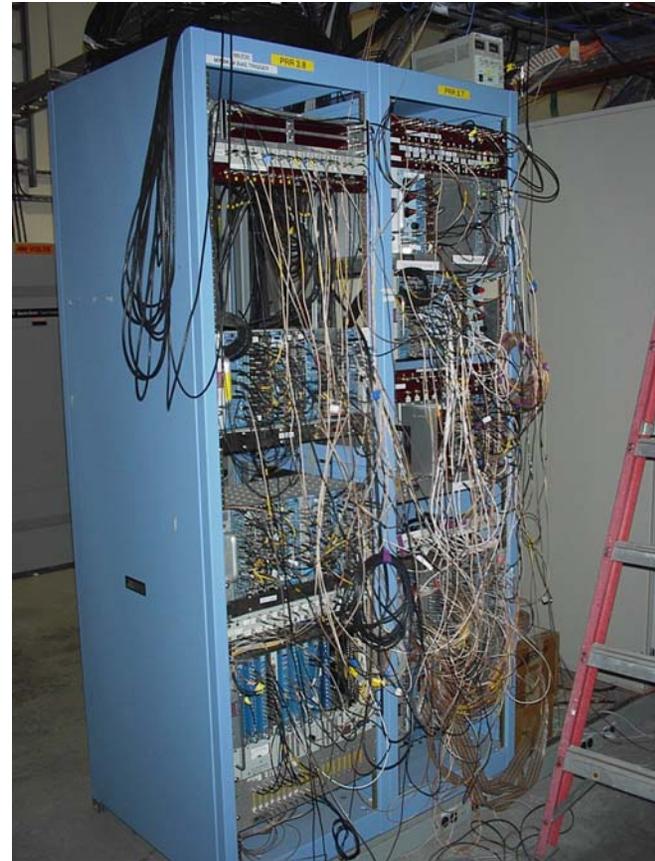
The rest of DAQ electronics is located in the Rack Room. We name VME crates by an IP name of the Power PC installed in it.

- The **GTM**s reside in two VME crates: iocondev10 and iocondev11, mounted in rack **PRR 3.5**
- Crates with **DCMs** are mounted in racks **4.1, 4.2, 5.1-5.4**
- **Global Level 1** and **Local Level 1** electronics are located in the rack **3.1**
- **Blue logic** NIM crates are in racks **3.7, 3.8**
- **SEB** computers are in racks **4.4, 4.5**
- **ATP** computers reside in rack **4.8**
- Data storage phnxbox 1-3 are located in rack **2.2**



# Blue Logic Rack

- *Better even do not approach it!*

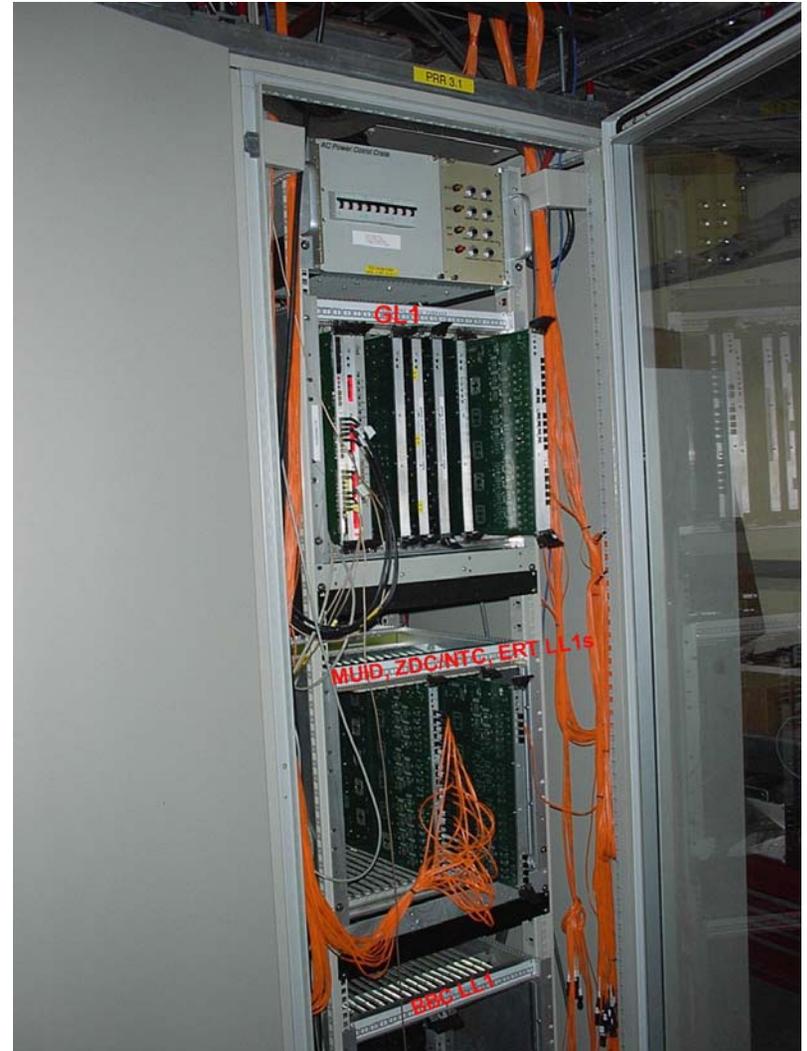


# Trigger System

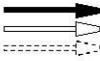
- Trigger electronics are located in rack PRR 3.1
- 1. GL1 is located in the top crate iocondev14. It consists of several boards (front):

| Board name | Slot (fixed/range) | Installed |
|------------|--------------------|-----------|
| PPG        | 3 (yes)            | yes       |
| GL1-2      | 4 (yes)            | yes       |
| GTM        | 5 (yes)            | yes       |
| GL1-1      | 9 (no/6-13)        | yes       |
| GL1-1      | (no/6-13)          | no, spare |
| GL1-1P     | 11 (no/6-13)       | yes       |
| GL1-1P     | (no/6-13)          | no, spare |
| GL1-3      | 16 (yes)           | yes       |

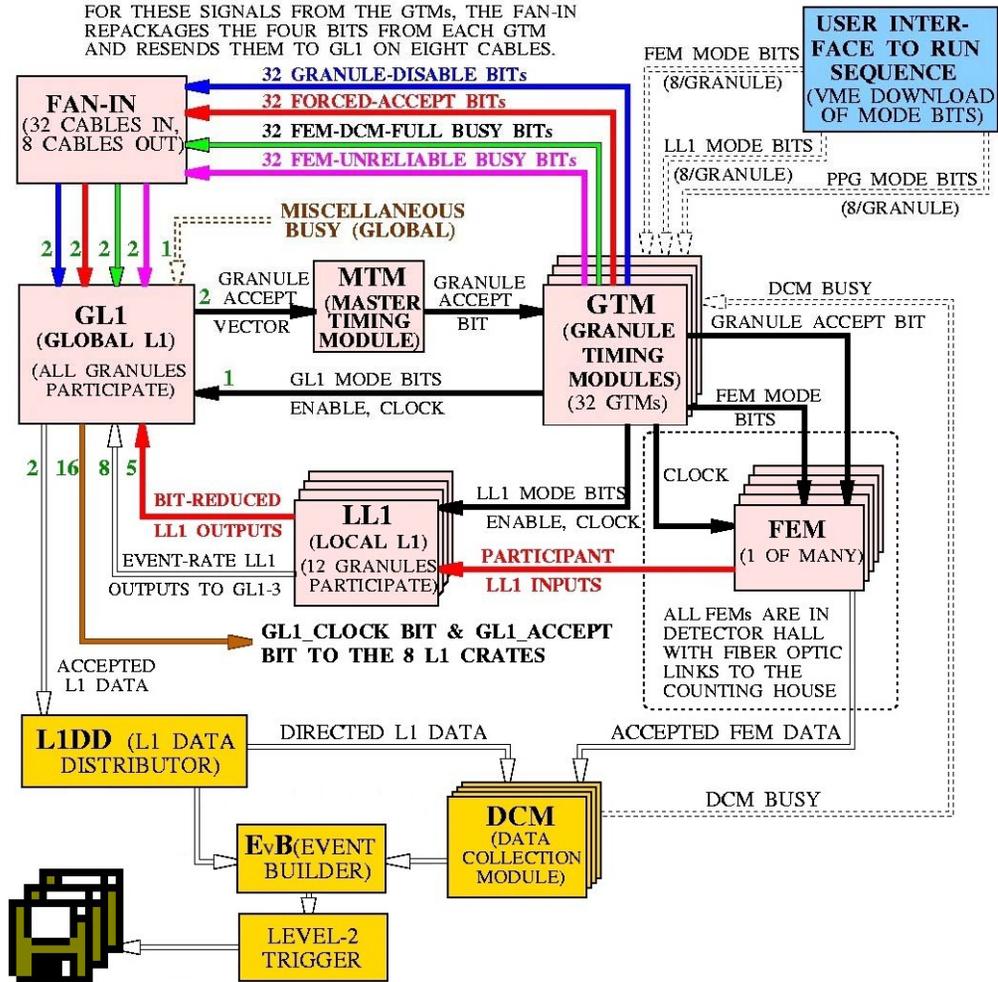
- Minimal working combination of GL1 boards: GTM, GL1-2, GL1-3, one GL1-1. GL1 may have 7 additional boards – any combination of GL1-1 and GL1-1P boards. Boards responsibility:
- **PPG** – Programmable Pulse Generator: issues signals to run Laser, EMC test pulses.
- **GL1-1** – defines 32 triggers: logic, Trig->Partition map, mask off, Scale down values.
- **GL1-2** – handles Granule’s busy signals, Dead-for-N busy.
- **GL1-3** – Trigger->Partition->Granule mapping, defines event buffering counter (1-5), governor delay.
- **GL1-1P** – configures 4 luminosity scalers. Mainly used in PP runs only.



# PHENIX DAQ

LEGEND:  FILLED ARROWS FOR DATA TRANSFER AT BEAM CROSSING RATE  
 EMPTY ARROWS FOR DATA TRANSFER AT ACCEPTED EVENT RATE  
 DASHED ARROWS FOR DATA TRANSFER AT ASYNCHRONOUS RATE

FOR THESE SIGNALS FROM THE GTMs, THE FAN-IN REPACKAGES THE FOUR BITS FROM EACH GTM AND RESENDS THEM TO GL1 ON EIGHT CABLES.



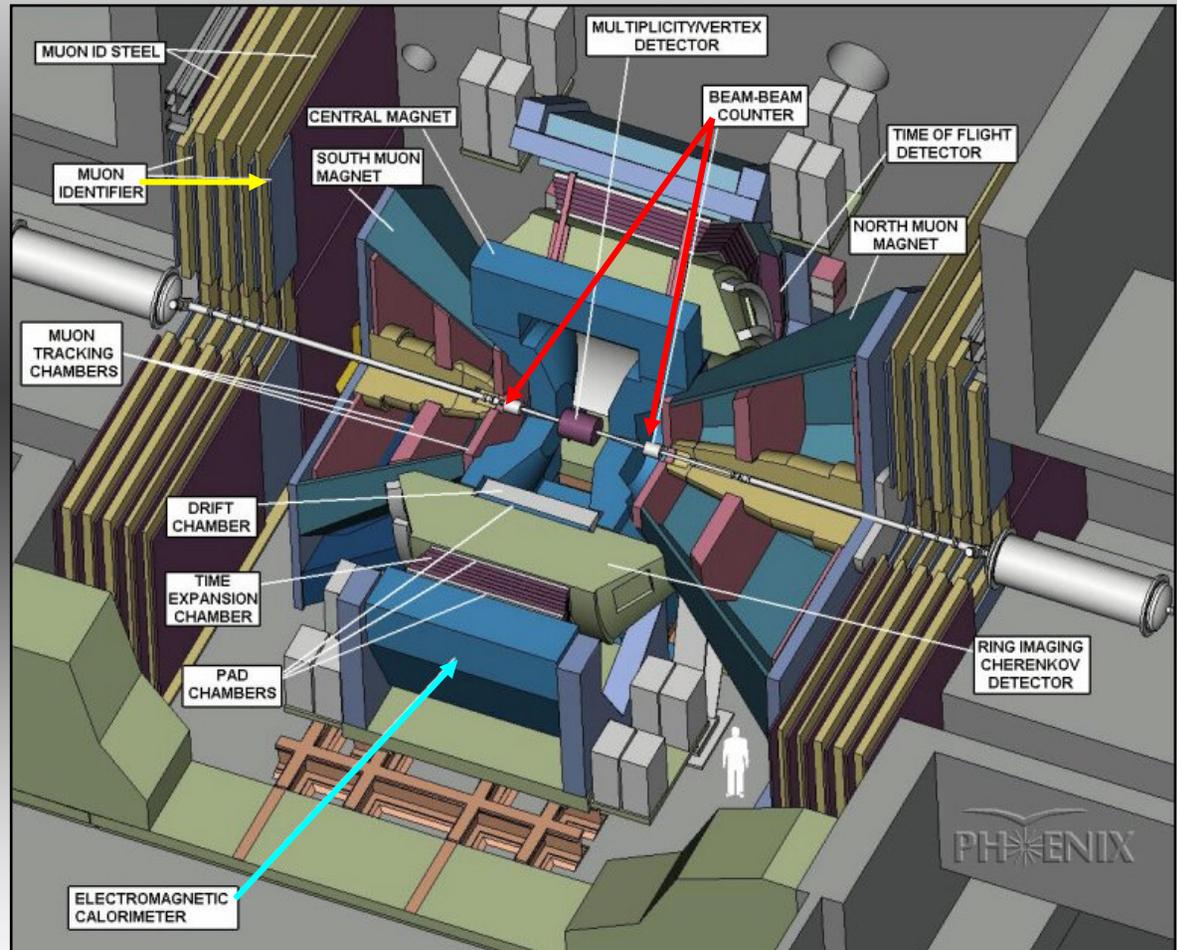
- Three levels of trigger decision:

  1. FEM->LL1 -> Reduced Bits
  2. RB->GL1->Accept->FEM
  3. FEM->DCM->EvB->LL2->HD

# Local Level 1

Subsystems used in LL1:

- ✓ **Beam – Beam Counters**
- ✓ **Muon Identifier**
- ✓ **NTC/ZDC**
- **EM Calorimeter (ERT)**



# BBC LL1 goal

Distance between BBC:  
288.7 cm

Selects events with

**Min** < **Vertex** < **Max**

**RUN1:**

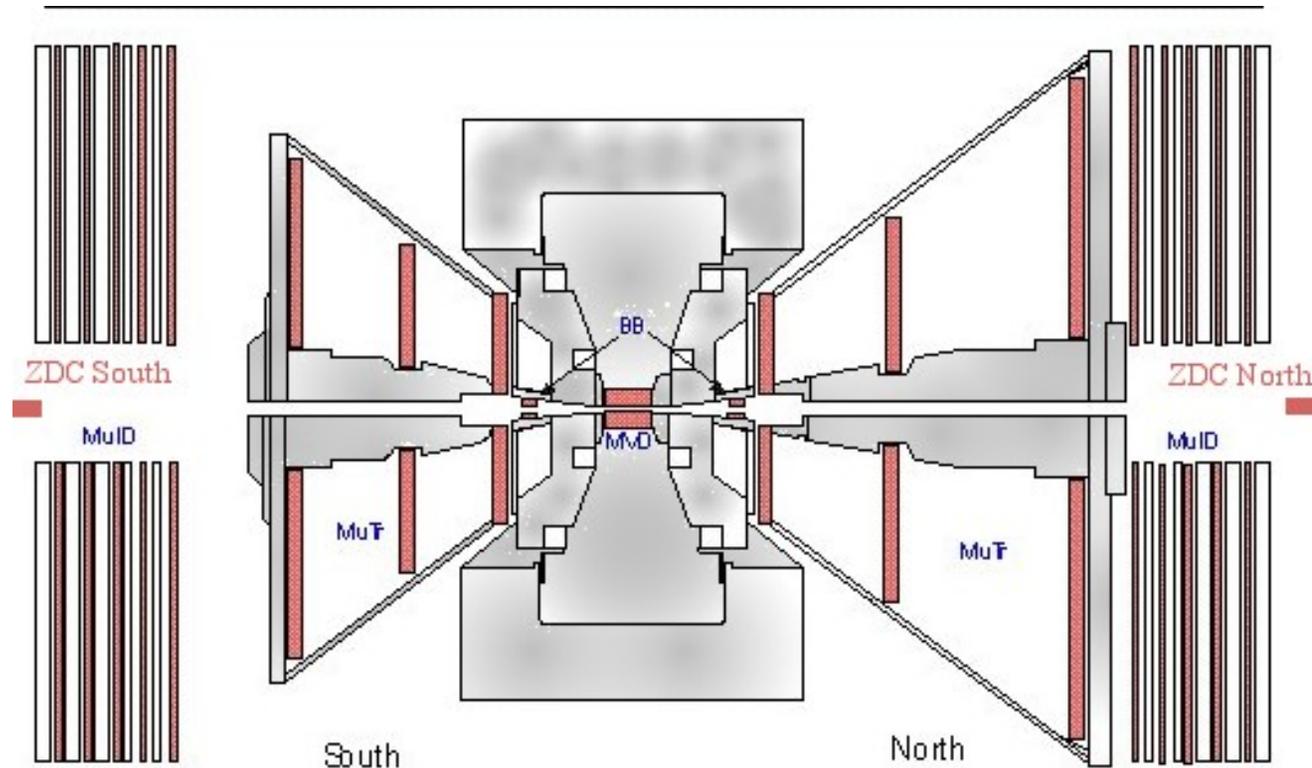
**Min** = - 20 cm

**Max** = +20 cm

**RUN2:**

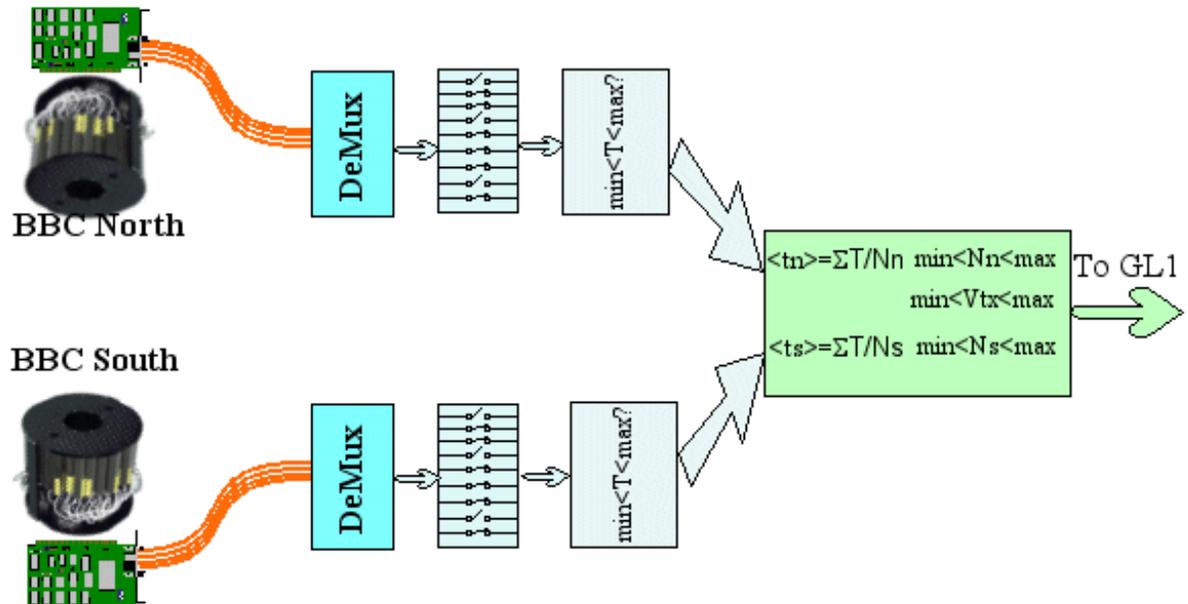
**Min** = - 30 cm

**Max** = +30 cm



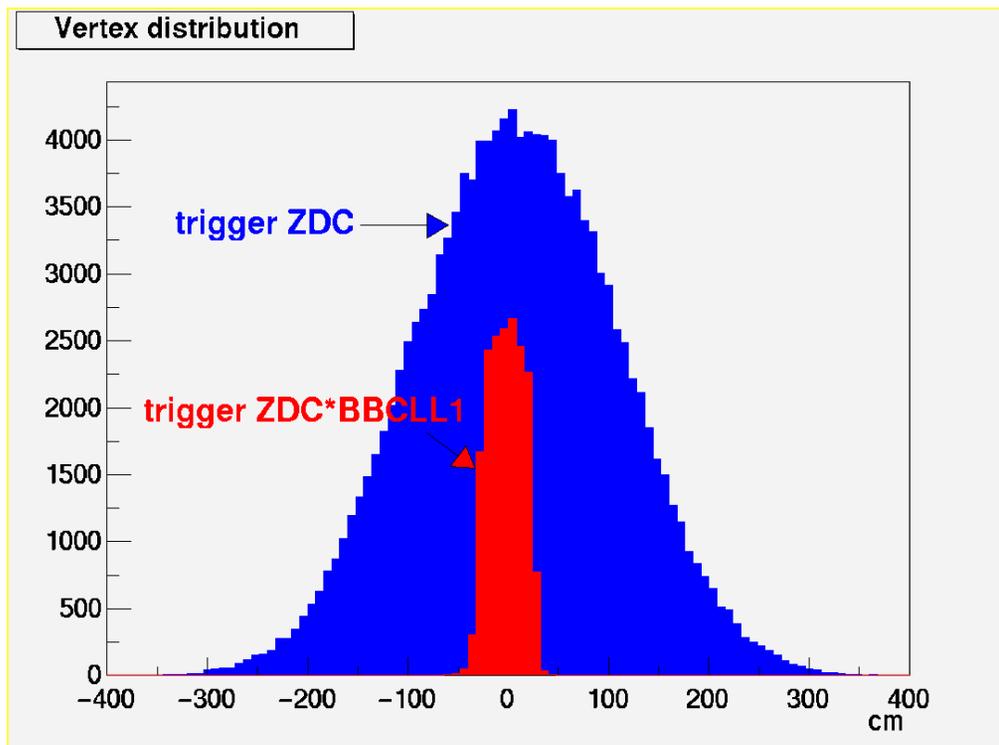
# BBC LL1 operation

1. Converts input bits into channel time values
2. Masks off bad channels
3. Checks time range for each channel
4. Determines number of hits in each arm
5. Calculates average arm time
6. For each arm checks if number of hits is in range
7. Checks if Vertex is in range
8. Result of the last two checks and FEM Unreliable signal are used as an input into 4->2 Look Up Table that creates 2 output bits for GL1

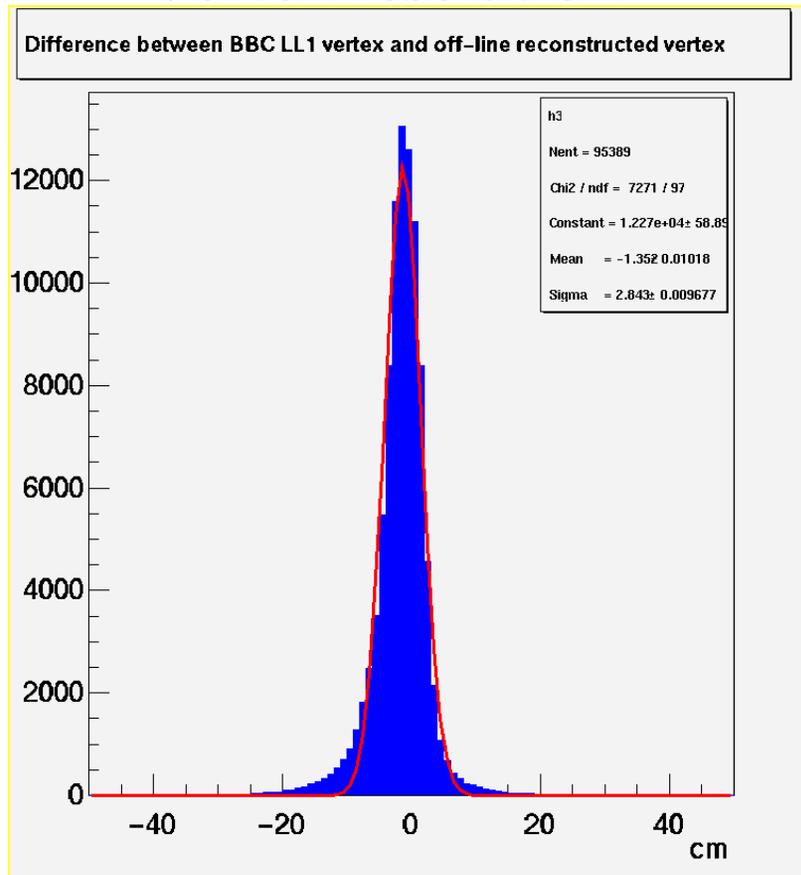


# Results: Vertex Cut

## Vertex cut



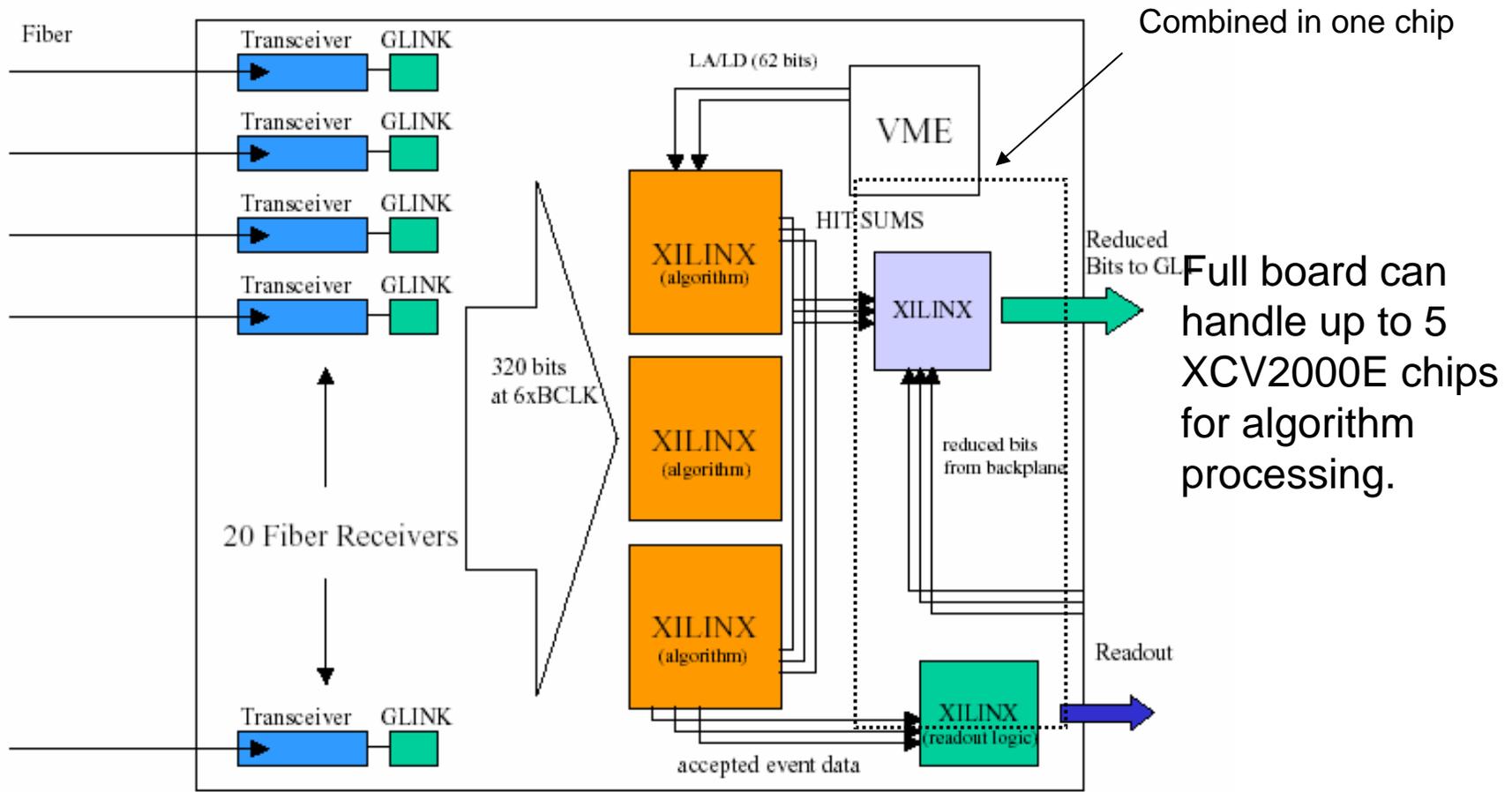
## Vertex resolution



# Common Level-1 Hardware Design

- First generation Level-1 systems (BBC) used detector specific electronics, non-programmable design – expensive to implement and modify.
- PHENIX needs a flexible set of Level-1 electronics that can adapt to a wide variety of detector systems, data rates, and physics requirements.
- Take advantage of technology advances, particularly in reprogrammable gate arrays (Xilinx XCV2000E ~2 million gates).
- Common hardware platform for a wide variety of trigger needs.
- Extended lifetime of hardware within PHENIX physics program.

# “Generic” LL1 Board

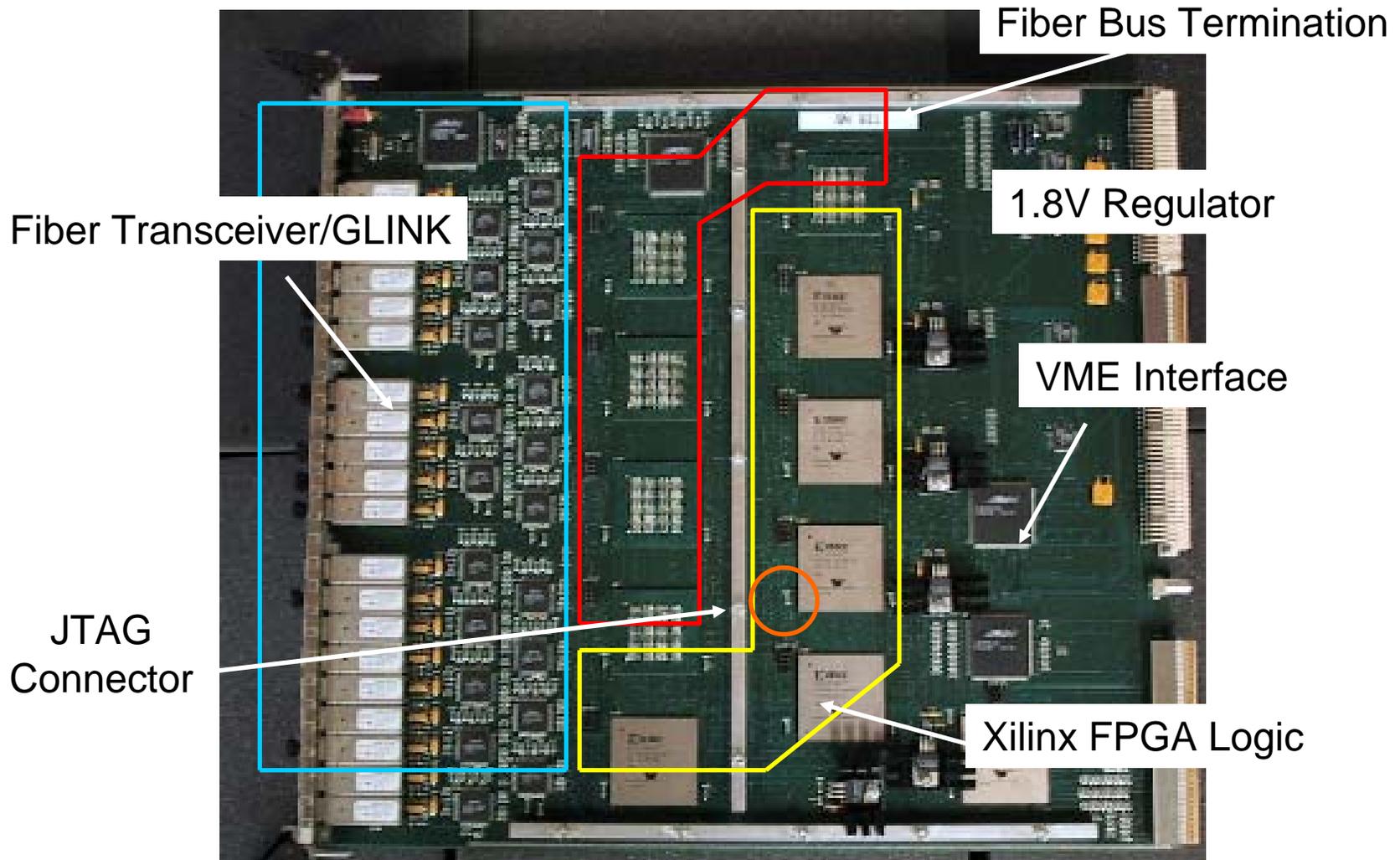


Full board can handle up to 5 XCV2000E chips for algorithm processing.

# Generic LL1 Board (cont.)

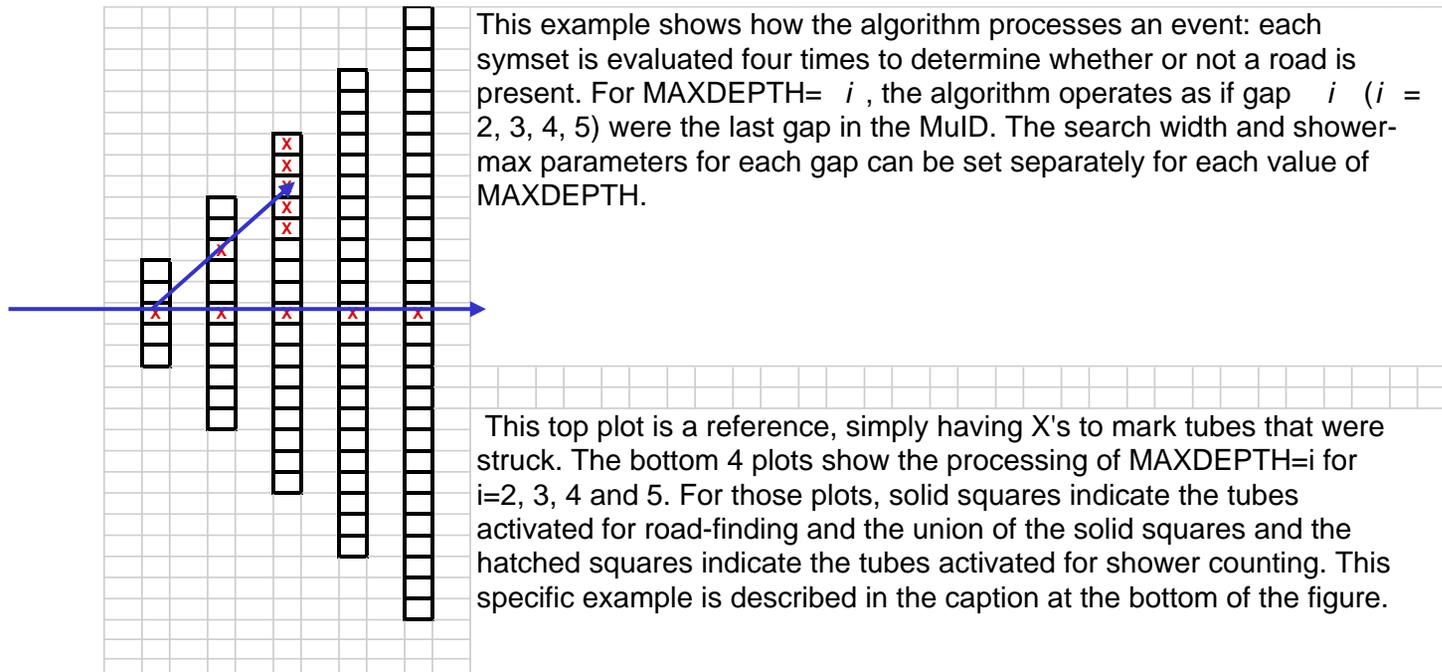
- Generic board with very flexible functionality.
- Fiber speeds individually selectable – can handle both 4xBCLK and 6xBCLK systems.
- Each algorithm chip can pass up to 18 bits of data to the transfer control chip.
- Backplane includes the ability to pass up to 32 bits between boards, as well as a 16-bit data bus (with clock and control)
- Multiple boards can be multiplexed into the same GL1 cable.
- All algorithm and fiber demux logic contained in Xilinx – there should be no need for hardware changes to accommodate new algorithms.
- A single board can (in principle) handle multiple LL1 systems.

# Generic Level-1 Board Design



# MuID LL1 Algorithm

- Dynamically steered algorithm, allows non-consecutive steered gaps.
- Uses groups of logical tubes (OR'ed physical tubes) organized as *symsets*.
- Tracks penetrating to each layer determined in parallel.
- Programmable search widths by layer.





# MuID LL1 Expected Performance

## [Event Rejection for pp Running:](#)

Studies by K. Read indicate that the MuID LL1 algorithm should be able to achieve sufficient rejection for pp (achieved a factor of 880):

<https://www.phenix.bnl.gov:8080/WWW/publish/kread/notes/minbias2.ps>

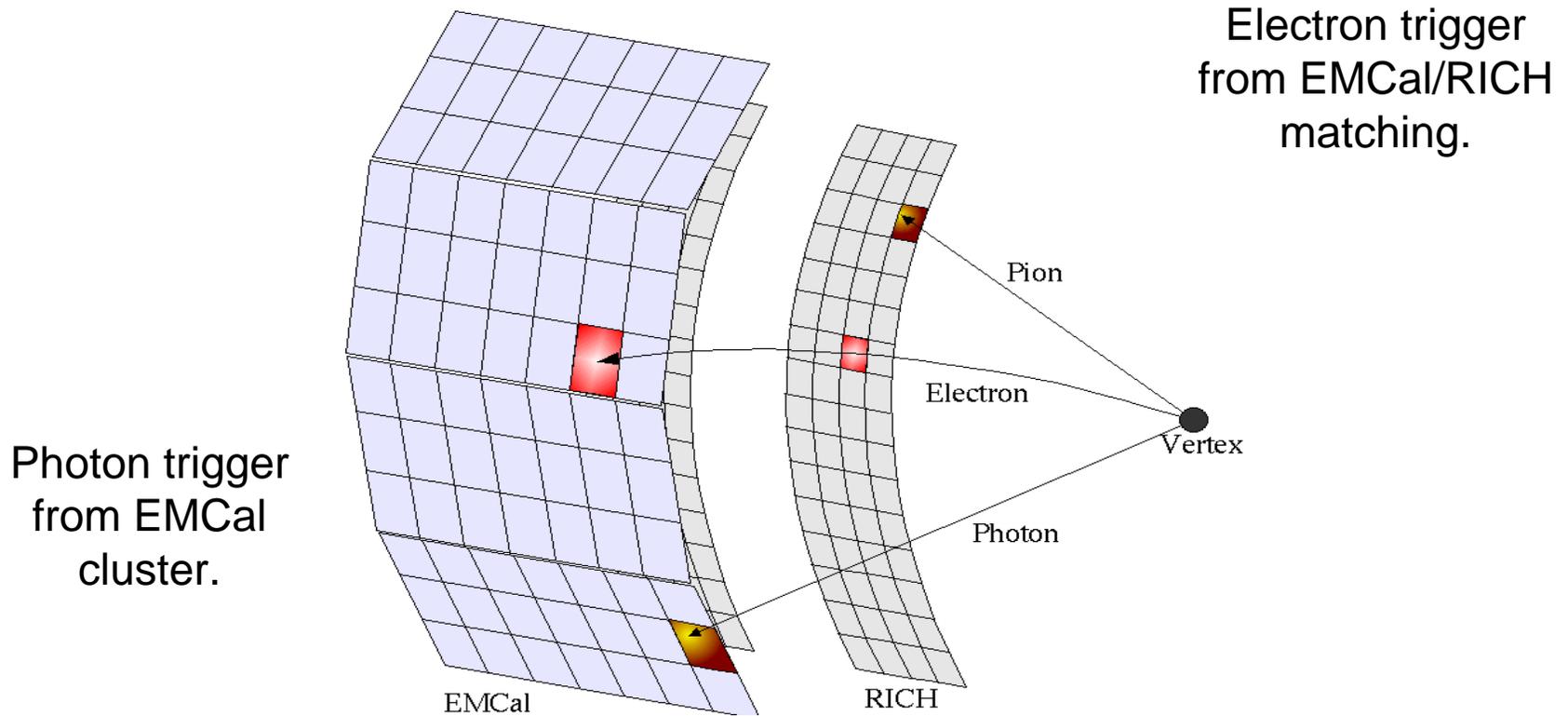
| sqrt(s) (GeV) | Lum. (cm <sup>-2</sup> s <sup>-1</sup> ) | s (mb) | Rate (Hz)          | Required Rejection (1/2 BW) |
|---------------|--|--------|--------------------|-----------------------------|
| 200           | 8x10 <sup>31</sup>                       | 50     | 4x10 <sup>6</sup>  | 320                         |
| 500           | 2x10 <sup>32</sup>                       | 60     | 12x10 <sup>6</sup> | 960                         |

## [Event Rejection for HI Running:](#)

*Note: For heavy-ion running event rejection is not required at Level-1 to stay within the DCM bandwidth.*

Envision at the present time that MuID LL1 data will be used to provide seeds for Level-2 algorithms (could change as our understanding of the trigger improves).

# EMCal/RICH Algorithm



# NTC/T0/ZDC Algorithm

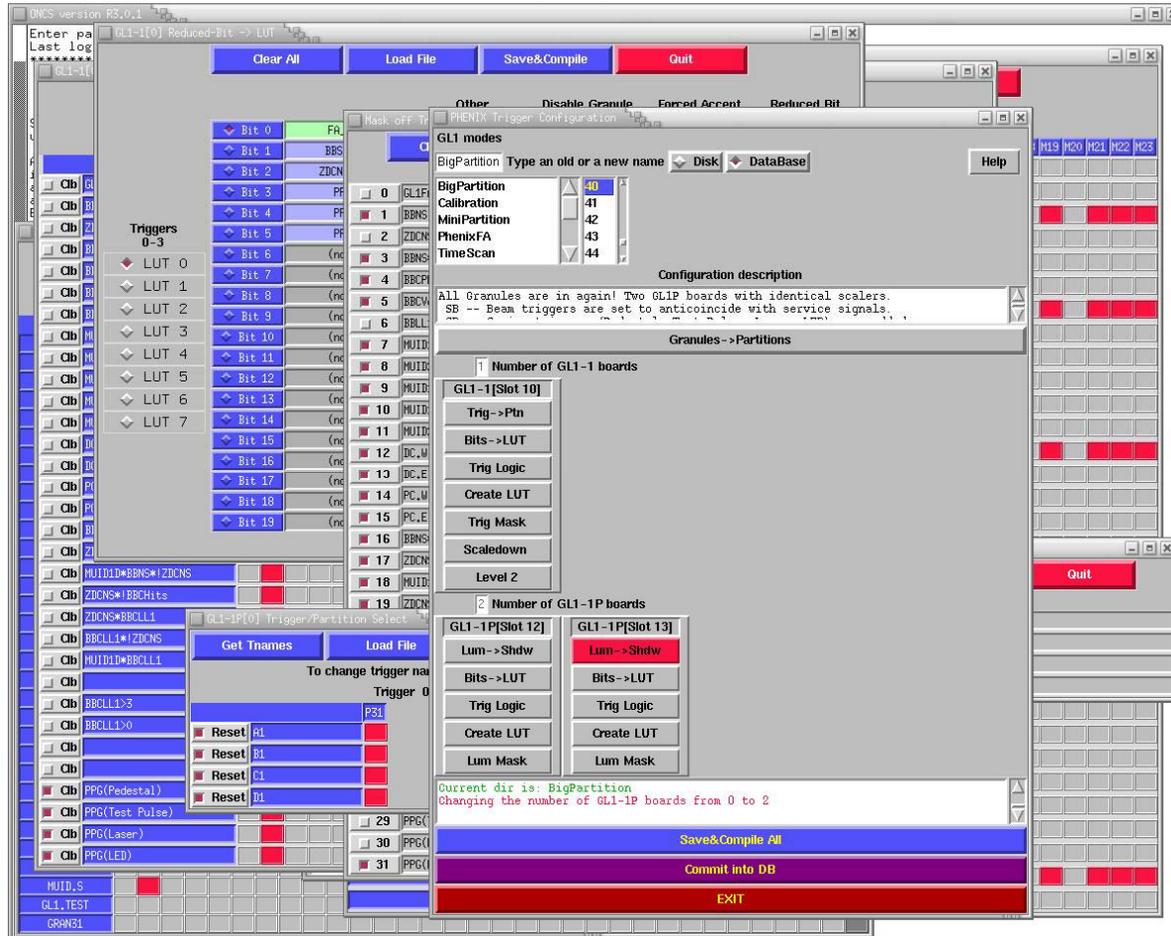
- ZDC:

One fiber, take TDC's from discriminated analog sum for each side. Subtract to get a vertex, compare to a range. Will be able to check two vertex ranges.

- NTC:

One fiber, four TDC values per side. Form mean time for each side, subtract to get a vertex and compare to a range. Will be able to check two vertex ranges..

# PHENIX Trigger System configuration GUI



# level1gui

### Level 1 Trigger

**File**

GL1 **BBC**

Global Level 1

GL1-1[0] **GL1-2** GL1-3 GL1-1P[0]

Commands

Show Raw Triggers      Show Live Triggers      Show Scaled Triggers

Clear All Counters

Status

|                       |                        |                          |
|-----------------------|------------------------|--------------------------|
| Latency Trim: 4       | Tag Trim: 3            | Trigger Mask: 0x00000000 |
| MonFIFO Empty=0xFFFFF | MonFIFO Full=0xFFFFF   | GL1 Xfer. Counter: 0     |
| VME slot: 9           | Board Serial No: 0x482 | Trans. Card: None        |
| Readout Flags=OK      |                        |                          |

GL1 Global Buses

VME: ■    GOV: ■    MISC: ■

Show Advanced Features    Run Config. Script    Gran./Trig. -> Part. Mapping

Start Monitor    GTM

Configuration Progress: 0% (PPRun4 14)

PHENIX Level 1 Trigger Interface

### GL1-1[0] Raw Triggers

| Trigger                 | Counter        | Rate     |
|-------------------------|----------------|----------|
| GL1FA                   | 105358         | 26       |
| Clock                   | -1.838714297E9 | 12240853 |
| BBCLL1                  | 1703665        | 0        |
| BBCLL1(moVertexCut)     | 3478731        | 2        |
| ZDCLL1wide              | 109836         | 0        |
| ZDCNS                   | 305994         | 0        |
| ZDCLL1narrow            | 49296          | 0        |
| ZDCN ZDCS               | 8426857        | 3        |
| ERT_2x2&BBCLL1          | 0              | 0        |
| ERT_Gamma1&BBCLL1       | 0              | 0        |
| ERT_Gamma2              | 3014           | 0        |
| ERT_Gamma2&BBCLL1       | 0              | 0        |
| ERT_Gamma3&BBCLL1       | 0              | 0        |
| ERT_Electron&BBCLL1     | 0              | 0        |
| MUIDLL1N_1D             | 0              | 0        |
| MUIDLL1S_1D             | 0              | 0        |
| MUIDLL1N_2D             | 0              | 0        |
| MUIDLL1S_2D             | 0              | 0        |
| MUIDN_1D1S&BBCLL1       | 0              | 0        |
| MUIDN_1D&BBCLL1         | 0              | 0        |
| MUIDS_1D1S&BBCLL1       | 0              | 0        |
| MUIDS_1D&BBCLL1         | 0              | 0        |
| SamePolarization        | -4.22803123E8  | 940083   |
| OppositePolarization    | 0              | 0        |
| Unpolarized             | 0              | 0        |
| Forward&MUIDS_1D        | 0              | 0        |
| (ZDCN ZDCS)&BBCLL1      | 183526         | 0        |
| (ZDCN ZDCS)&(BBCLL1S^N) | 592399         | 0        |
| MUIDLL1S_1D1S           | 0              | 0        |
| PPG(Test Pulse)         | 5268           | 1        |
| PPG(Laser)              | 5268           | 1        |
| MUIDLL1N_1D1S           | 0              | 0        |

Close

# Conclusions

- **Three level trigger system: Local Level1, Global Level1, Level2.**
- **No (or controlled) dead time.**
- **Supports multi partition DAQ configurations. Up to 32 partitions can be handled simultaneously.**
- **It is possible to configure up to 128 triggers as logical combinations of 130 input signals.**
- **Permits to enrich a portion of rare events in the data stream by scaling down other events.**
- **Pipelined and buffered trigger data stream.**