

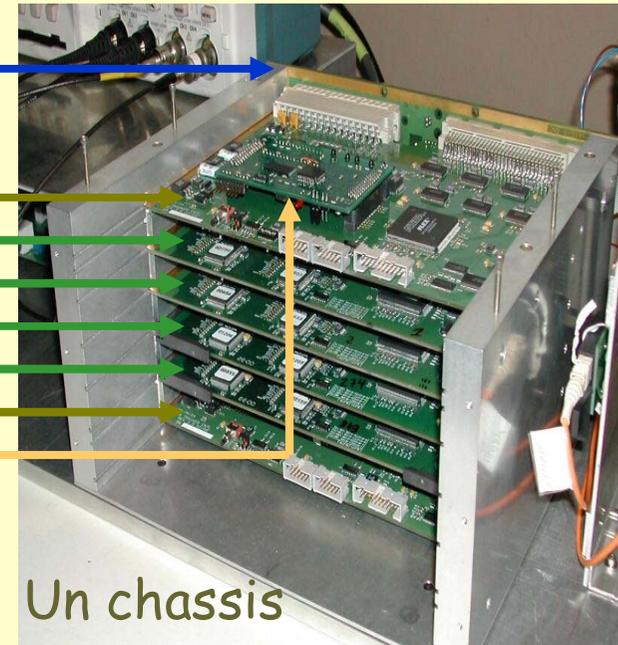
Muon Tracker Electronics Performances and Issues

Vi-Nham Tram & Olivier Drapier, LLR, Ecole Polytechnique, France

Muon Tracker Electronics

- 100+116 backplanes
- 168+192 CTLs
- 336+384 CROCs
- 168+192 ArcNets

During repairing/installation

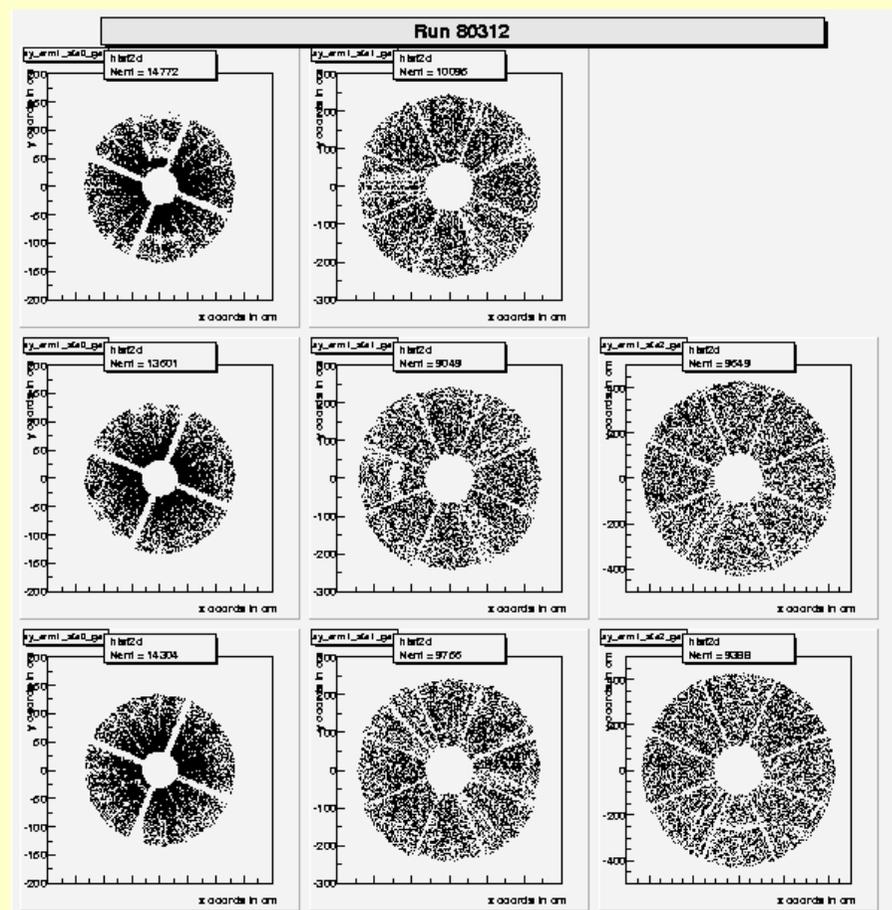
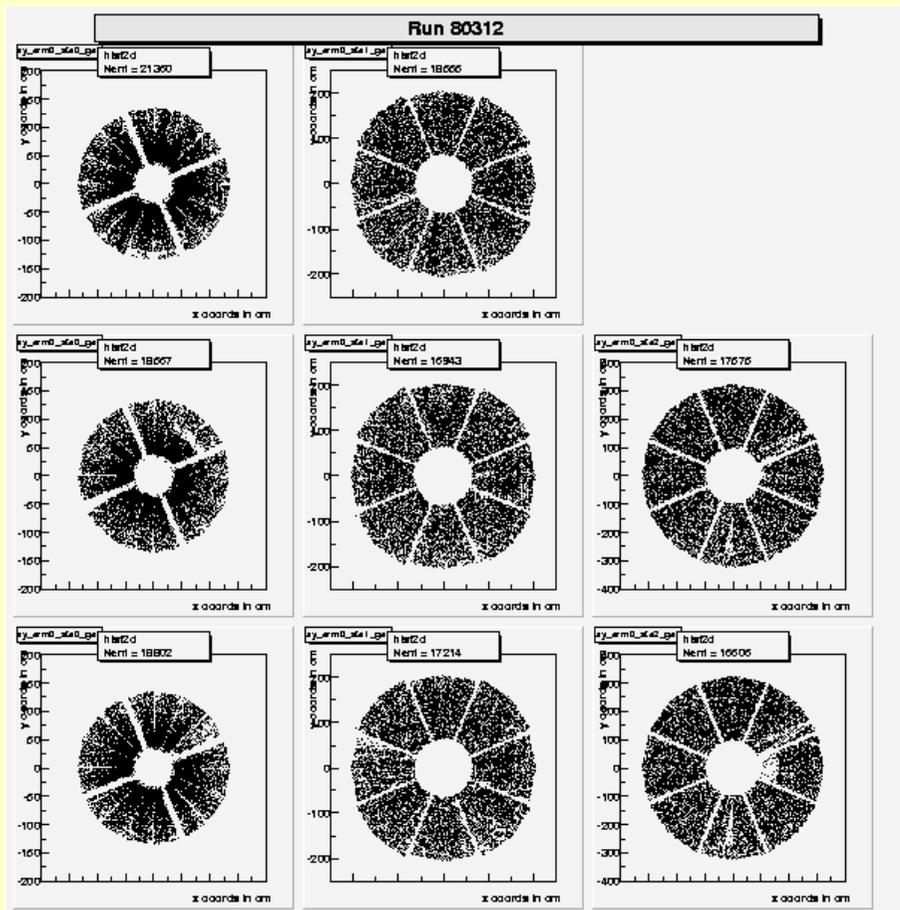


Replaced	Backplane	FEM	CROC	ArcNet
South	5	9	27	2
North	1	9	15	1

Run 3

South Arm

North Arm



Station 1

Station 2

Station 3

Station 1

Station 2

Station 3

Only few dead regions

Outline

- Troubles during Run 3
 - Duplicated channels
 - AMU Cell errors
 - Other problems
- Future
 - Spares
 - New Test Bench
 - RX/TX Boards

Duplicated Channels

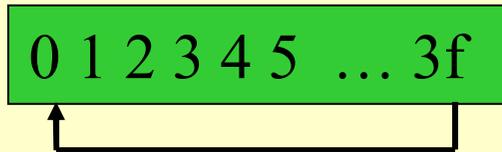
- Data lost by 16, 32 & 64 channels in some packets
- Occurred during the Run 2 & 3
- Only few FEMs :
 - * 4 Fems during Run 2 (South Arm)
 - * 7 Fems during Run 3 (South & North Arms)

~ 1 % channel loss

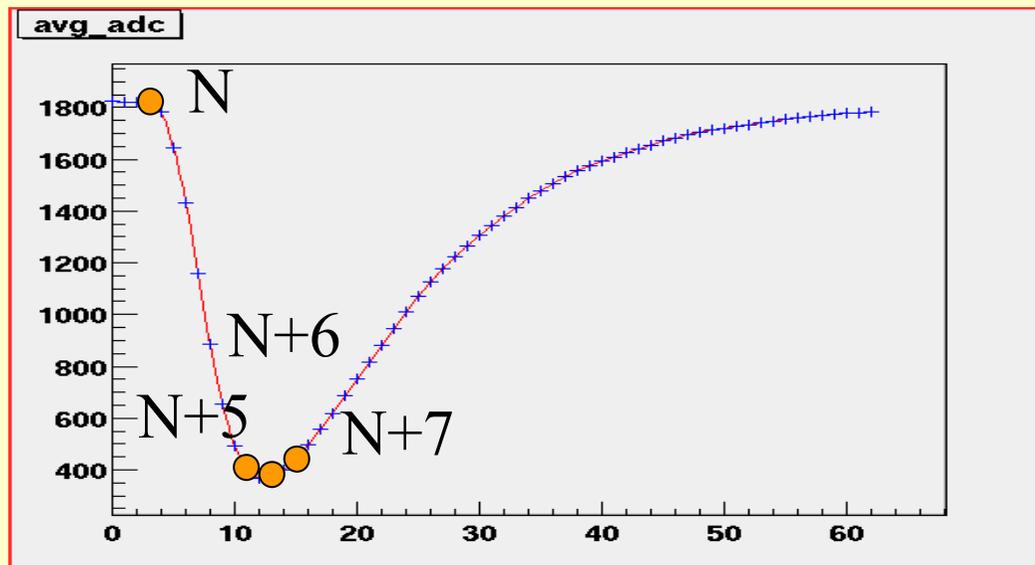
- Probably due to bad electrical contacts on CTLs, CROCs and/or Backplanes.
- not seen with old test procedure : will now be detected with a new Test Bench (to be installed next month)
- This will be addressed during next shut down :
 - * FEMs containing duplicated channels will be changed
 - * Spares will be tested

AMU Cell Errors

- Strip charges stored in the AMU (64 Cells)



- 4 time samples/event



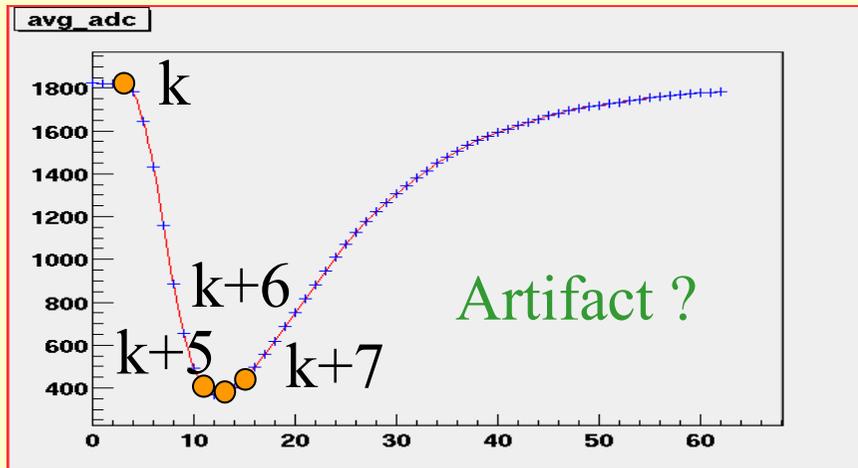
N

trigger

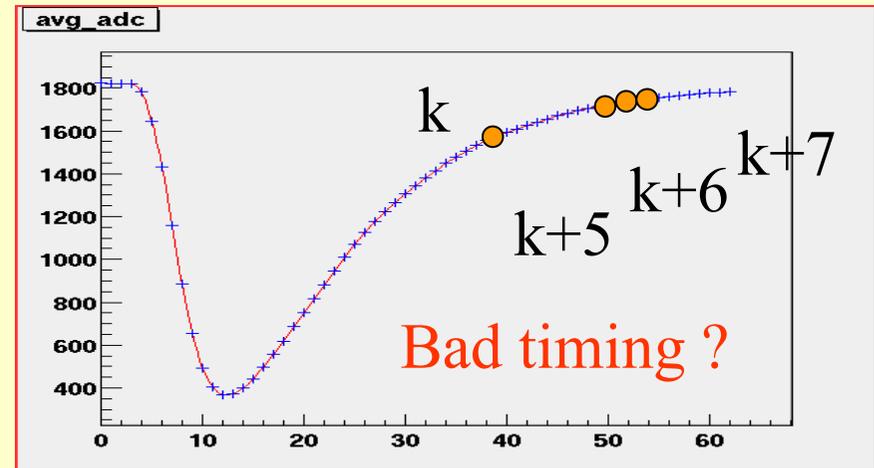
Cell addresses are written in the packet header

Some packets (~ 10 FEMs) have wrong cell addresses

- * either global shift : $k, k+5, k+6, k+7$ ($k \neq N$)
 - * or bad cell sequence : $N, N+5, N+7, N+8$
 - * total: $\sim 60\% - 100\%$ events in the worst FEMs
- \Rightarrow Artifact or real problem ?



= Good data



= Bad data

- Melynda & Olivier studied a dedicated calibration run
 - * Compare the ADC average value $(ADC(N+5) + ADC(N+6) + ADC(N+7))/3$ for good/bad events
 - * Compare individual samples for good/bad events

Mean values & RMS are identical for good & bad events

=> this AMU Cell problem does not affect data !

Interpretation :

The internal counter just skips one clock tick sometimes, but we still don't know why it appears in some FEMs only...

0 1 2 3 4 6 7 8 9 a b c d e ...

Others problems during Run 3

- South Arm :
 - Station 3 octant 5 : 64 dead channels
 - Only one CROC died !
 - Burn-in long enough
 - Good stability of AMU/ADC & Preamp chips (reliable cooling in IR helps)
 - Station 2 & 3 octant 5 & 6
 - Intermittent problem with G/Clink crate power supply (solved by raising the voltage : need further investigation)
- North Arm :
 - Station 3 octant 8 : 1 dead channel in one RX board (spare channel used : no data lost)

Spares

- 100 CROCs (need max : 8)
- 50 CTLs (max : 7)
- 20 ArcNets
- 15 Backplanes (max : 4)
- 8 LV distribution boards (max : 1)
- 6 RX & 4 TX boards

=> No need to build new boards

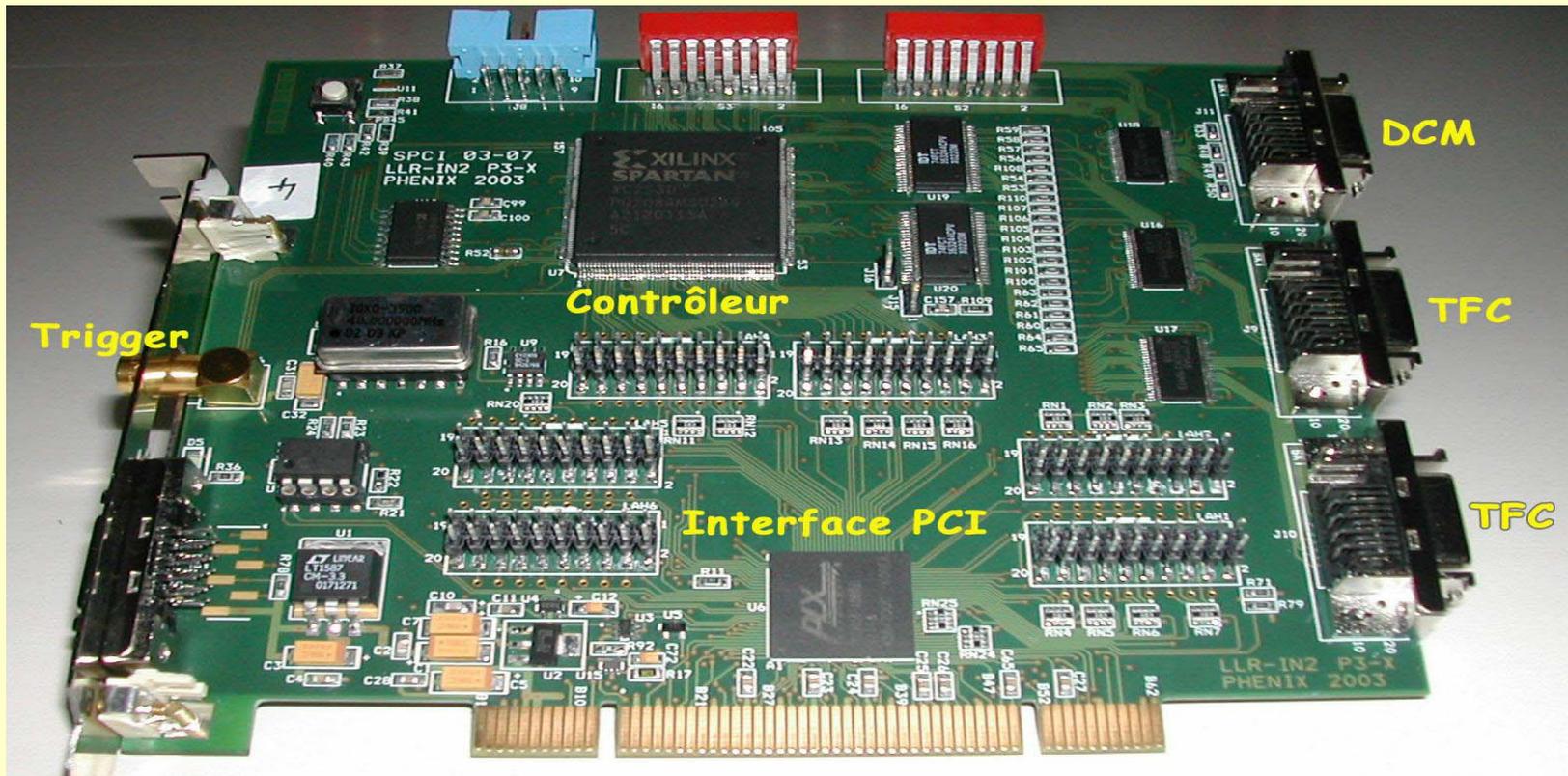
Test Bench improvement

Old Test Bench :

- Uses Mini DAQ & PC-ISA interface (obsolete)
- Arcnet interface & MiniDAQ cannot be driven from the same script
- Too many pieces (MiniDAQ, G/Clink, power 6/5/3.3 V, pulse generator...)
- Glink/Clink boards (old prototype) not reliable...
- Only 1 FEM (1 CTL+2 CROCs) can be tested
- 1 event at a time

New Test Bench

- New PCI board developed at LLR
- Directly connected to FEMs, TFC & DCM

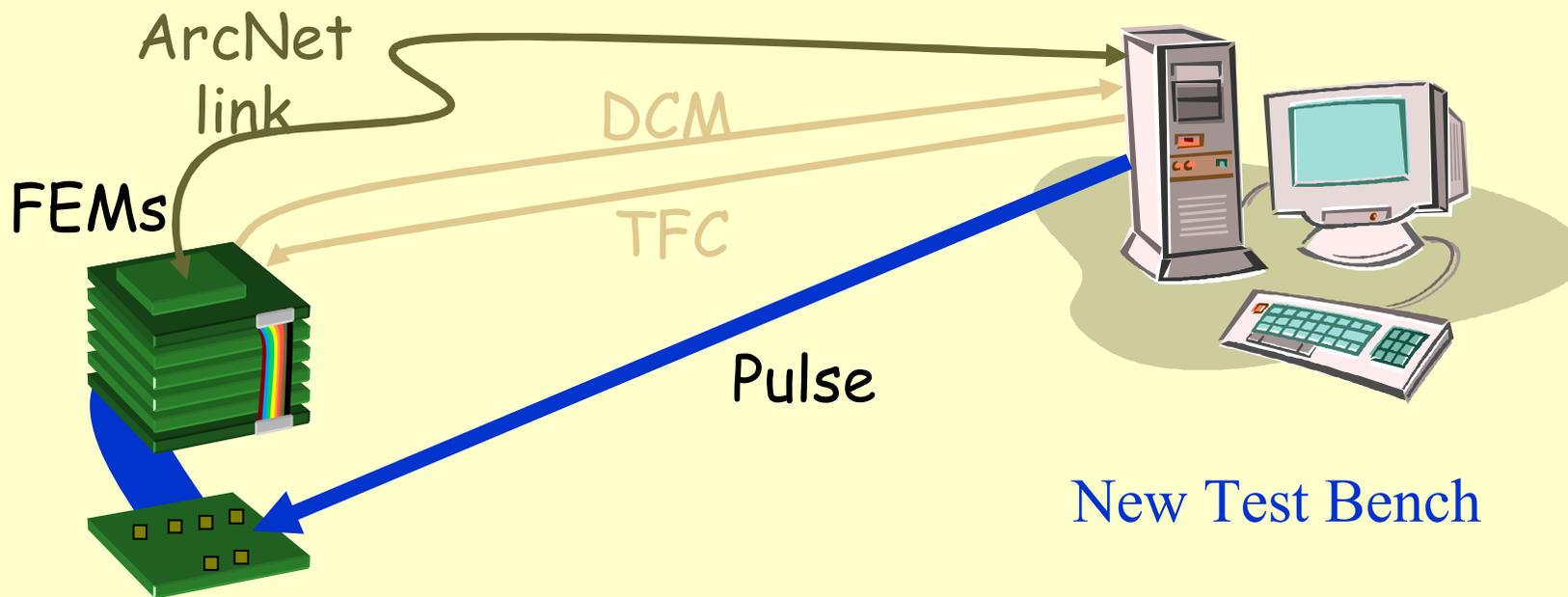
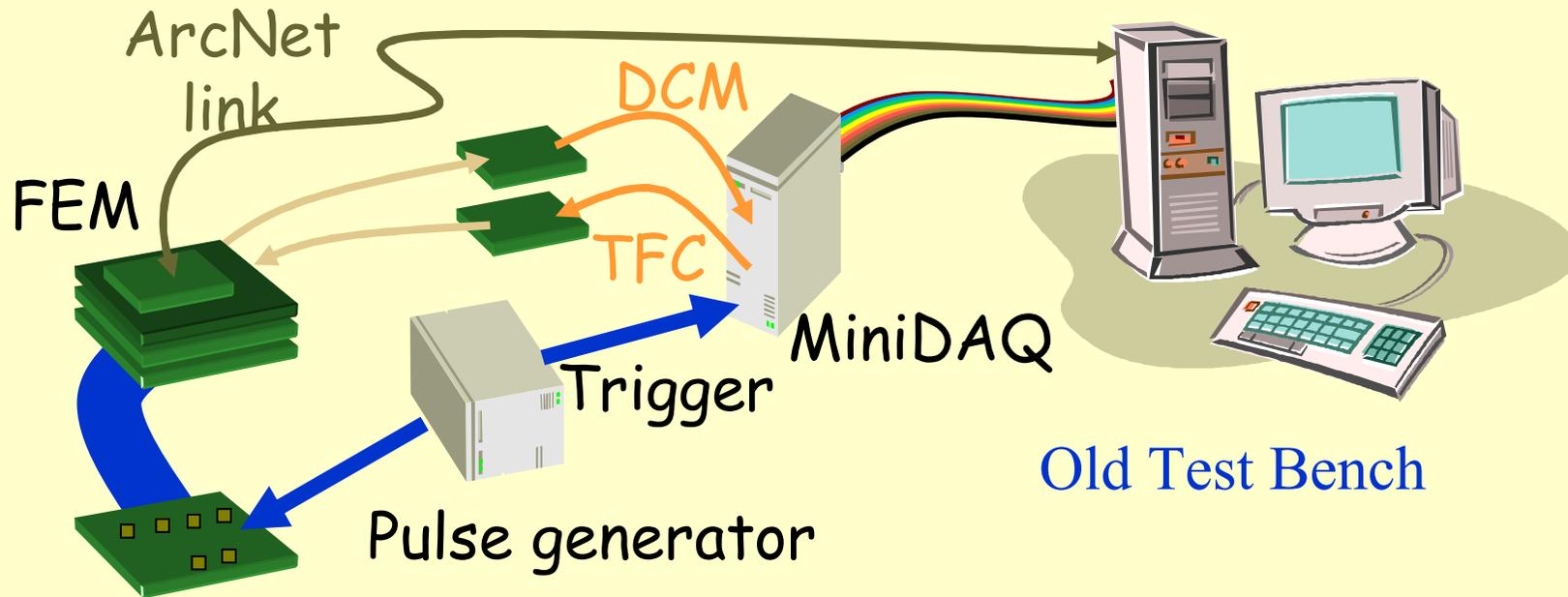


New Test Bench

Advantages :

- No MiniDAQ needed, only PCI interfaces
- Arcnet commands & acquisition from the same program
- everything fits in a PC (DAQ + pulse generator) only 6V for FEMs
- 2 FEMs (Master/Slave) tested at the same time
- multi-event acquisition => more tests (stuck bits, noise, duplicated channels)

2 benches will be installed next July (Alain Debraine, Franck Gastaldi & Simon Chollet) both at 1008 & LLR



RX/TX Boards

Study for new RX/TX boards :

- Use up-to-date parts (3.3 V)
 - Only use 3.3 V instead of 5 + 3.3 V
- => Improve reliability
- Prototype expected at the end of this year

Production expected in April 2004

Suggestion :

Build more RX boards to increase band width
in the future ?