

**Addendum  
to  
the PHENIX Vertex Upgrade Proposal**

This is an addendum to the PHENIX Vertex Upgrade Proposal we have submitted in July 2004. The proposed project is to construct a Silicon Vertex Tracker to provide precision vertex tracking near the collision point. The new detector will give PHENIX a new capability to detect particles with charm and beauty as well as large solid angle coverage. The project would be jointly funded by DOE and Japan (RIKEN).

The proposal was reviewed by “Project readiness review of the PHENIX Barrel Vertex Tracker” on January 19-20, 2005. The summary of the review report is given below.

Summary of findings and recommendations:

- *The Committee finds that the proposed project is well advanced in its development, and is technically feasible. Though some important technical challenges remain, we believe that the well-organized team put together by PHENIX for this project is capable of dealing with them. Some specific technical issues are listed in this report. We note that, in addressing these issues, the VTX group will very likely find it necessary to modify the work plan.*
- *The schedule proposed for this project, with a completion date in January 2008, is driven by a strong desire to utilize this detector for a high-statistics gold-beam run in 2008-2009. We find this schedule to be very aggressive. We recommend that the group re-examine the project schedule – taking account of the detailed recommendations given in the following sections of this report – without constraining the completion date to meet a specific goal of the RHIC operations plan.*
- *We find that the cost estimate for the project is well considered, and is based on sound practices for developing a project of this type. The materials budget appears to be credible. The labor cost should be re-evaluated after an updated schedule has been prepared. While we do not expect dramatic changes in the total cost estimate for the project, it is important to demonstrate that a realistic schedule, with appropriate schedule contingency, can be accommodated within the final cost estimate.*
- *Overall, we find that this project has been brought to a state that can meet the requirements for a DOE Major Item of Equipment project, to be funded in FY 2006. We recommend that PHENIX present to BNL management an updated schedule and cost estimate, addressing the detailed recommendations of this report, within the next few months. The timing of this update should be coordinated with BNL, and with DOE, to facilitate a successful cost/schedule “baseline” review to initiate the project.*

Following the review report and the recommendations given by the review panel, we have re-evaluated the project cost and the schedule. A full bottoms-up risk analysis was performed following the model presented to and approved by the review committee. Explicit schedule contingencies based on the risks has been added. We also reduced the budget in FY06 to \$1M based on the present budget circumstance. The project is now for three years to complete (FY06, FY07, and FY08) and the total project cost is \$4.4M including contingency, a slight (+\$100K) increase from the one presented in the proposal.

This addendum is organized as follows. In section 1, we briefly summarize the progress since the submission of the proposal to date. Most part of the progress was reported in the January review and considered by the review panel. After we received the review report, we updated the cost and schedule of the proposed project following the recommendations of the review report. The updated cost and schedule is presented in section 2. Main points of the changes from the proposal in the project are also summarized in the section. There are many recommendations and questions on specific technical issues in the report. The answers to these technical issues are presented in section 3. In the appendix, the review report is included.

# 1. Update since the submission of the proposal

Substantial progress has been made for preparation of the start of the project since we have submitted the proposal in July 2004. In this section, we briefly summarize our progress after the submission of the proposal to date. Most of the progress was reported in the January review and was considered by the review panel. We also include the progress after the review.

## 1.1 Pixel

### A. Q/A of ALICE pixel chip

The pixel detector uses pixel read-out (R/O) chip developed for ALICE experiment at LHC. At the time of proposal submission, RIKEN had purchased 16 wafers of the pixel R/O chip from CERN. After the submission of the proposal, RIKEN purchased and obtained 6 additional R/O chip wafers from NA60 experiment at CERN. Now total of 22 wafers are in hand.

No	Wafer Name	Class1	Class2	Class3	Remain	Yield
Lot 6						
1	<a href="#">ABA4J4T</a>	40	4	42	0	46.5%
2	<a href="#">AAA4J5T</a>	32	2	52	0	37.2%
3	<a href="#">A9A4J6T</a>	26	5	55	0	30.2%
4	<a href="#">AVA4LJT</a>	39	20	27	0	45.3%
5	<a href="#">ATA4LLT</a>	24	28	34	0	27.9%
6	<a href="#">A3A4JCT</a>	37	11	38	0	43.0%
7	<a href="#">AXA4LHT</a>	33	19	34	0	38.4%
8	<a href="#">AZA4IZT</a>	22	3	61	0	25.6%
9	<a href="#">ATA4I5T</a>	44	6	36	0	51.2%
10	<a href="#">AZA4E1T</a>	29	3	54	0	33.7%
11	<a href="#">ACA4J3T</a>	0	1	85	0	0.0%
12	<a href="#">AQA4DTT</a>	11	0	75	0	12.8%
13	<a href="#">A9A4ERT</a>	31	5	50	0	36.0%
14	<a href="#">AWA4E4T</a>	41	13	32	0	47.7%
15	<a href="#">ANA4M8T</a>	31	0	55	0	36.0%
16	<a href="#">ALA4MAT</a>	6	25	55	0	7.0%
Lot 5						
17	<a href="#">PJVM15T</a>	41	9	36	0	47.7%
Total		487	154	821		
Yield		33.31%	10.53%	56.16%		
Achievement		81.17%				

**Figure 1 Summary from the pixel R/O chip Q/A database. Name of the wafer and number of class-1 (good), class-2 (not good but functioning) and class-3 (not functioning) chips are shown for each of the 17 wafers probed so far.**

We have been probing these wafers using a semi- automatic probe station to identify good chips. In the proposal, we reported that 4 wafers had been probed and 134 class-I (i.e. good) chips had been found. This Q/A operation proceeded on schedule. All of the initial 16 wafers plus 1 newly purchased wafer had been probed so far. Figure 1 shows the summary of the Q/A results. We now identified 486 class-I chips in these 17 wafers. Since the newly purchased wafers comes from a lot with know

good chip yield of about 50-60%, we expect that we will have about 700 class-I chips when the probing of all 22 wafers is completed. We need 600 class-I chips including 150 spares to complete two layers of the pixel detectors.

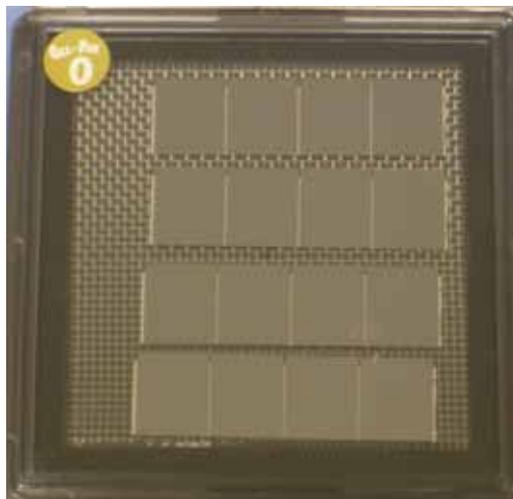
The probe station used for this Q/A operation at CERN is owned by RIKEN. It has been shipped back to RIKEN to be used in the VTX project.

#### B. Pixel Sensor

Six wafers (54 sensor chips) of PHENIX pixel sensor has been produced at CAMBERRA, Italy. They are to be bump-bonded with the R/O chips to form pixel sensor ladders. The 54 sensor chips in this first production are sufficient for the inner-most pixel layer, which requires 40 sensor ladders.

#### C. Bump bonding and the first pixel ladder

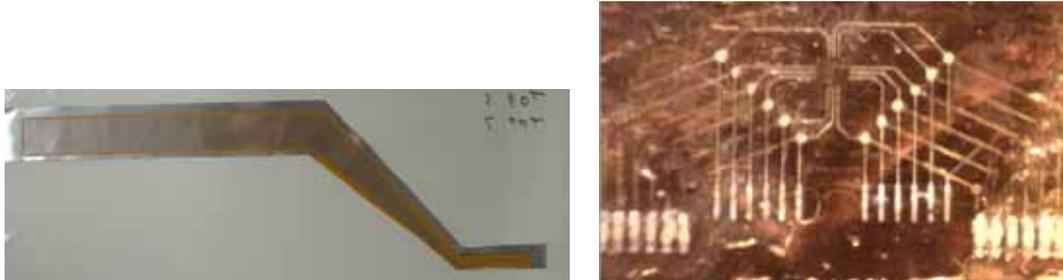
Four pixel R/O chips and one pixel sensor are bump-bonded to form one pixel sensor-ladder. One full ladder consists of 4 such pixel sensor ladders. The bump-bonding of the sensor chips and the R/O chips is one of the technical challenges in the construction of the pixel detector. Recently, the first articles of PHENIX pixel ladders have been produced by VTT, Finland, and they have been delivered to CERN. Figure 2 shows a picture of four bump bonded ladders delivered from VTT. Five additional ladders will be produced and delivered to CERN by the end of March 2005. They will be shipped to RIKEN, and then will be wire bonded with the pixel bus prototypes to produce the first functional PHENIX pixel ladders. See the next section about the pixel bus development.



**Figure 2 Four bump bonded ladders for PHENIX produced at VTT and delivered to CERN**

#### D. Pixel Bus

The data from the pixel R/O chips are read-out through a very thin, very high density digital bus, which we call pixel bus. This is one of the most technologically challenging components of the pixel detector.



**Figure 3 Left: Pictures of an Al/Kapton bus prototype made by Soliton. Right: Picture of three layer Al/Kapton test structure made by Soliton**

A very good progress has been made on the R&D of the pixel bus since the submission of the proposal. We are working together with a Japanese company (Soliton) to produce prototypes of the pixel bus. The R&D program is so far very successful. The company has produced a single layer prototype of Al-Kapton bus with  $30\ \mu$  wide Al traces and  $30\ \mu$  gaps. The trace width and the gap width are the same that required for the PHENIX pixel bus. The first trial of producing multi-layer structure (3 layers of Al-Kapton layers) was also successful, and the company has also successfully produced small through holes in the Kapton layers. We think all major issues in producing PHENIX bus are cleared.

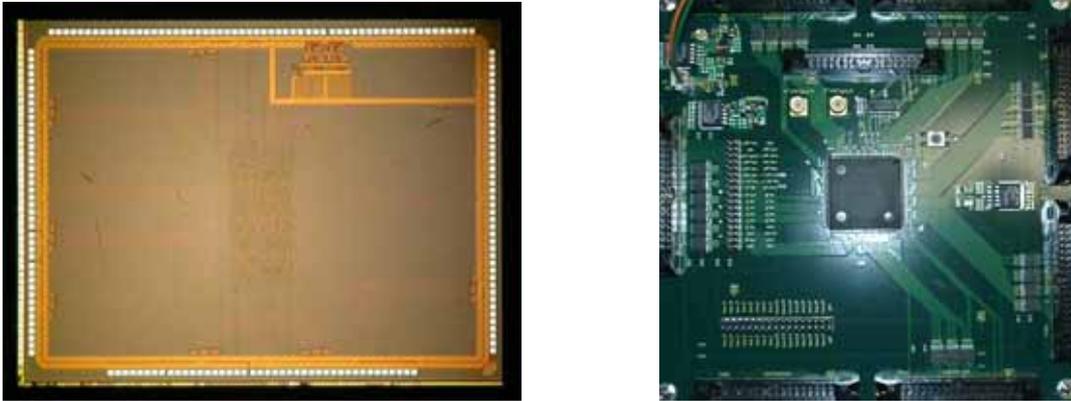
We are now preparing for producing the first functional prototype of PHENIX pixel bus. The prototype bus will be wire-bonded with the first articles of PHENIX sensor ladders to make the first prototype of fully functional PHENIX pixel ladder. To reduce the risk, we plan two steps in producing the prototype of the bus. In the first step, we will produce the pixel bus prototype with Cu/Kapton. This Cu/Kapton prototype is now scheduled to be delivered by the end of June 2005. The electrical test of the pixel bus itself and an integrated test with a real silicon pixel detector are now scheduled on July and August 2005. In the second step, production of pixel bus prototypes made of Al/Kapton will follow once we confirm that there is no major defect in the Cu/Kapton bus. The Al/Kapton bus will be made with the same mask and with very similar technology used for the Cu/Kapton bus.

#### E. Development of Digital Pilot ASIC

The data of the pixel R/O chips are read-out by an ASIC, called digital pilot chip, through the pixel bus. The digital pilot chip was originally developed for ALICE experiment using CERN/IBM multi-chip project. This ALICE version of digital pilot chip is, however, not suitable for PHENIX, and we need to make a small modification of the chip to meet read-out speed requirements of the PHENIX DAQ system. In the proposal, we reported that we had completed the modification of the design and had submitted the modified digital pilot chip to CERN/IBM multi-chip project in May 2004.

The submitted chip has been produced. We have received 170 chips in September 2004. The left panel of Figure 4 shows a picture of the PHENIX digital pilot ASIC. This number of chips is sufficient for the full pixel detector, which requires 120 new digital pilot chips to read-out. The produced chips have been tested in RIKEN by a

RIKEN post doctoral fellow who has designed the modified chip. The right panel of Figure 4 shows the test board for the digital pilot chip. The test result shows that the chip works as designed, and no problem or defect has been found so far.



**Figure 4** Left: picture of the modified digital pilot ASIC. Right: The test board for the digital pilot ASIC. The chip shown in the left panel is packaged in the SMT package at the center of the board.

Although the modified chip has worked very well, we have found that it is desirable to make one more small modification in the chip. The modification is to encode the event number information in the output data stream so that we do not lose the event alignment during the optical data transmission from the detector to the DAQ system even if something wrong happens during the transmission. This modification is relatively low risk. The design of the second modified pilot chip is in progress, and it will be submitted to CERN/IBM multi-chip project by the end of March 2005. The delivery of the chip will be in June-July 2005.

#### F. Development of Silicon Pixel Interface Read Out (SPIRO) module

SPIRO, which we previously called as pilot Multi-Chip Model (MCM), is a key component in the pixel readout chain. The main functions of SPIRO are (1) sending control commands to and receiving the data from pixel readout chips and (2) sending the data to Pixel Front End Electronics (FEE) via Gigabit Optical link. A SPIRO module consists of digital pilot chips described in the previous section, optical transceiver chips, optical link components and other support chips.

In January 2005, Ecole Polytechnique (France) group officially joined to the pixel detector subsystem. The new group takes the responsibility of the pilot MCM, which is now named as SPIRO. Design work for the 1<sup>st</sup> version of SPIRO will be starting in April 2005. The prototype SPIRO boards will be produced and available by middle of July. They will be connected with prototype pixel ladders (sensor ladders + pixel bus) in August 2005 for the first full system chain test.

#### G. Front End Electronics

Two electronics engineers at Stony Brook University have started the design work of the Pixel FEM. One of the engineers is the main person who developed the Front End

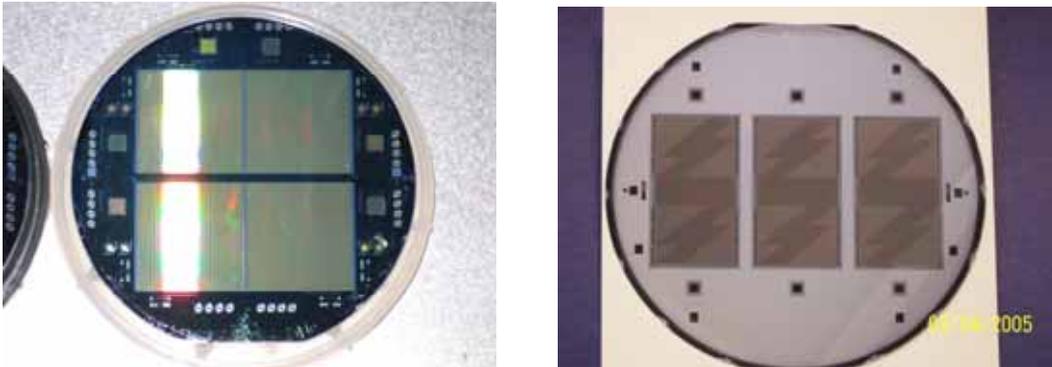
Module of the PHENIX Drift Chamber (DCH). The main function of the Pixel FEM is the interface between the pixel detector read-out system (SPIRO) and PHENIX Data Acquisition system (DAQ). To help the development of the FEM, a pixel detector readout system developed for the CERN/NA60 experiment has been set up at Stony Brook University. The read-out system includes one ALICE1LHCB pixel R/O chip, and the system will be used to investigate communication steps between the pixel R/O chip and the DAQ.

## 1.2 Strips

### A. Stripixel sensor development

At the time of proposal submission, we had ordered or were about to order test production of “pre-production” sensor to two companies, SINTEF in Norway and Hamamatsu (HPK) in Japan. This test production involves two types of design, “old” and “new”. The new design incorporates several features optimized for present design of the strip Read-Out Card (ROC). The old design sensors were ordered to both SINTEF and HPK, while the new design sensors were ordered to HPK only.

The test productions in SINTEF as well as in HPK have been completed, and the produced sensor wafers have been delivered. They have been subjected to various levels of tests and inspections. Figure 6 shows a sensor wafer each from SINTEF (left panel) and HPK (right panel). Initially these wafers were visually inspected and then those which pass the inspections, were also subjected to electrical QA checks at a new QA facility setup at BNL (see below.) The tested sensors will be then sent to ORNL and will be wire bonded with the first version prototype ROCs there and then subject to the full system chain test, which is now scheduled in March/April 2005. We will make the decision regarding the vendor and the design of the sensor based on the results of the test.



**Figure 5 Left: A picture of a SINTEFF sensor wafer . Right: A picture of Hamamatsu sensor wafer. A SINTEF wafer has two old design sensors and a HPK wafer has three new design sensors. Test structures and test diodes are seen in the peripheral part of the wafers.**

### B. sensor Q/A at BNL

Since the submission of the VTX proposal, a clean room with a semi-automatic probe stations has been setup in a RIKEN/BNL laboratory at BNL. Particle counting measurements has consistently shown that the contamination level of the clean room is better than 5 particles per cubic feet. The humidity in the room is at 30%. The semi-automatic probe station was borrowed from the BNL instrumentation division,

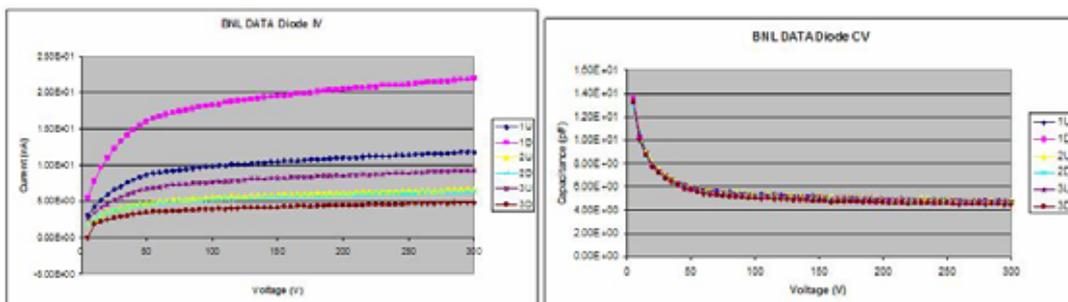
and it has been controlled using LabView program.



**Figure 6** Left: The clean room for the strip sensor Q/A at BNL. Right: Picture of Q/A station

A post doctoral fellow from RIKEN and a graduate student from Stony Brook have led the QA effort at BNL with significant involvement from a graduate student from Iowa State University. Around these three highly trained personnel (designated as shift leaders), we have further trained a group of 2 more post doctoral fellows and 5 graduate students from Stony Brook to work with the shift leaders to take shifts. The aim of this effort is to have a group of about 10-15 people who are able to run the QA stations at BNL and at Stony Brook in near future for three shifts a day if needed.

Figure 6 shows the BNL clean room and the probe station set up in the room. In Figure 7 we show the recent measurement results of the HPK sensors performed with this setup. As a first step, we have tried successfully to replicate all measurements of the QA nature that were provided to us by HPK for the set of wafers that were sent to us. The plan is to continue to study the HPK and the SINTEF wafers which we presently have as test production units, and develop the QA criteria for the production stage.



**Figure 7** Test results on a test diodes on a Hamamatsu sensor (625 m thick, new design) obtained at the BNL Q/A station. Left: I/V curves. Right: C/V curves.

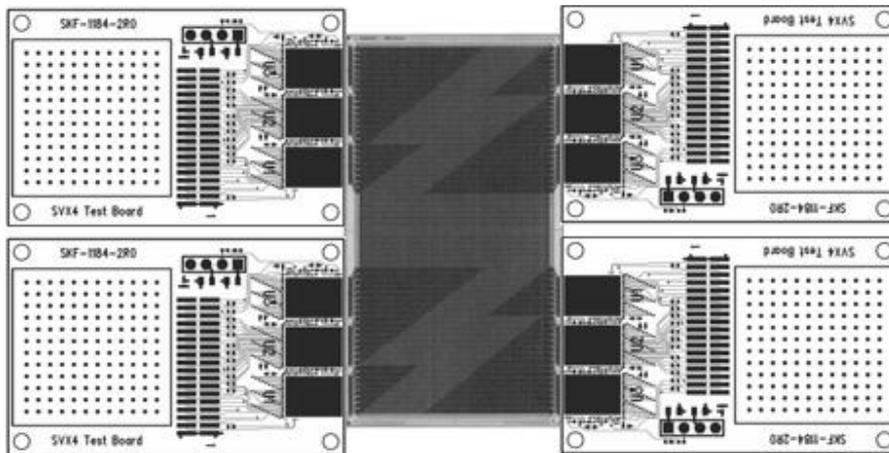
### C. SVX4 read-out chip

The strip detector uses SVX4 read-out chip developed at FNAL. RIKEN has purchased 18 wafers of SVX4 chip from FNAL through BNL. Based on the good

chip yield of a fully tested wafer in the same lot, each wafer should contain more than 300 good SVX4 chips. Thus the expected number of good chips in these 18 wafers is more than 5000, which is sufficient for the entire strip detector including healthy amount of spares. The first articles of the chips will be used in the 1<sup>st</sup> version ROC prototype now being developed at ORNL, and then will be used for the first system test now scheduled on March/April 2005.

#### D. Read-Out Card (ROC)

Design and manufacturing of the 1<sup>st</sup> version prototype of the strip ROC boards has been completed. In this version, a ROC is not a single board mounted on the sensor chip, but a set of four SVX4 hybrid boards and one RCC control board. One SVX4 hybrid board has 3 SVX4 chips and support circuit components, and a strip sensor is read-out by four hybrid boards as shown in Figure 8. These 4 hybrids are then controlled and read-out by a RCC control board. Significant progress was made in the testing/debugging of these ROC prototype boards and firmware, but the progress was limited since we so far have somewhat older version of SVX4 chips donated by FNAL. Tests will begin soon, after the production version SVX4 chips (version 2b) purchased by RIKEN have been tested by FNAL and shipped to ORNL. The prototype ROCs will be then connected with the pre-production sensors and will be subject to the full chain test. The test is now scheduled in March/April 2005.



**Figure 8** A schematic picture of four SVX4 hybrid boards of the first ROC prototype connected with a new design Hamamatsu sensor.

#### E. RC chip

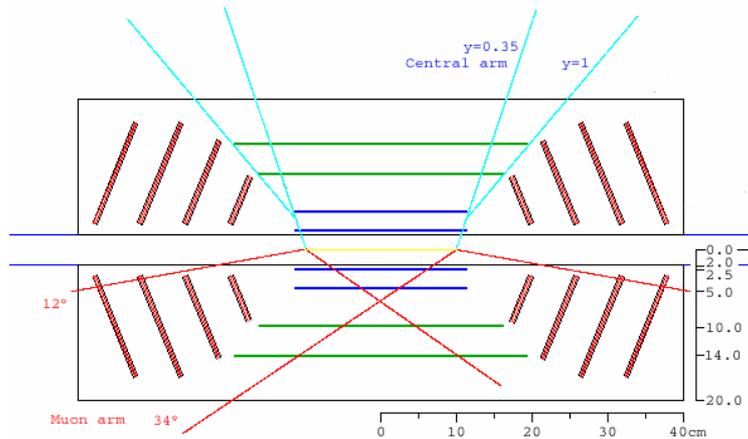
The strip sensor is a type of DC-coupling sensor, and it does not have bias resistors and coupling capacitors between p+ implant and Al metal layers. SVX4 is designed for AC-coupling sensors, and DC-coupling of the sensor to SVX4 chips might cause saturation of the preamplifier capacitors in SVX4 and noise fluctuation due to the leakage current from the sensor. The problems due to the leakage current can in principle overcome by resetting the capacitors in the SVX4 frequently, but its effect on the performance in particular to the S/N ratio has to be studied.

An alternative solution is to place an RC chip between the sensor and a SVX4, providing AC-coupling between the two. The RC contains 128 bias resistors and 128 coupling capacitors with the same pitch as the SVX4 chip. HPK has experience in making such an RC chip with their strip sensor fabrication technology. The design of the RC chip has been started with HPK. The 1<sup>st</sup> prototype of the chips will be delivered in the end of July 2005. Mean time, the noise performance of the SVX4 with AC coupling and with DC coupling to the sensor will be studied in the full system chain test of the 1<sup>st</sup> version ROC, now scheduled on March/April 2005. The decision regarding the use of the RC chip will be made based on the result of the system test.

### 1.3 Integration/Mechanical

#### A. Geometry update (Interface between the barrel and the End Cap)

As future extension of the VTX detector, we have a plan of end-cap silicon detectors that cover the forward rapidity regions and the acceptance of PHENIX muon arms. The end-caps will complement the VTX barrel by providing larger rapidity coverage, higher total rates and greater reach in transverse momentum. The interface between the barrel and the end-caps is intended to be as seamless as possible, but because of their close proximity, care must be taken to avoid interference of their services for readout, power and cooling. This is already being done to streamline engineering on the design. Although the end-cap detectors are not part of the present proposal, we include them in the mechanical design of the VTX for future upgrade.



**Figure 9 Schematic cross-sectional view of the VTX detector (the barrel+the end-cap)**

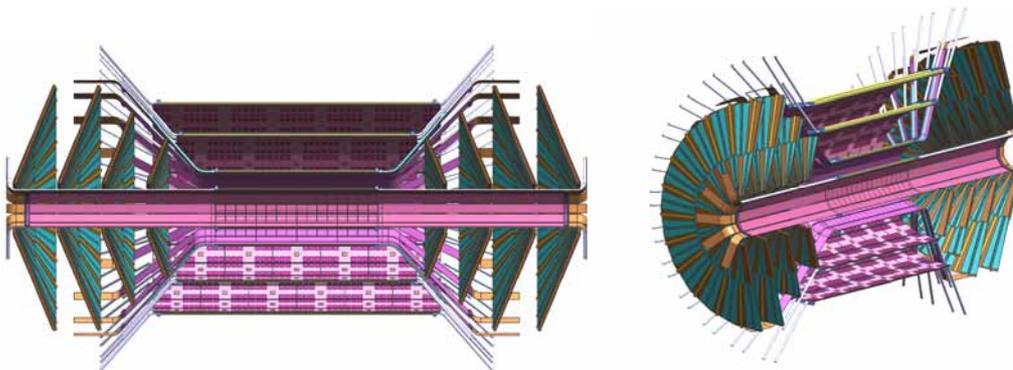
Figure 9 is a schematic for the current cross-sectional view of the VTX detector including both of the barrel and the end-caps. The blue lines are the pixel layers at radii of 2.5 cm and 5 cm, while the green lines are the strip layers at radii of 10 cm and 14 cm from the beam axis (yellow line). The cyan lines at an angle corresponding to a rapidity of  $y=1$  define the edge of the strip layers. Also in cyan are lines indicating the PHENIX central arm acceptance. The set of four thick red lines on either side of the of the VTX barrel denote the position of the end-cap layers. The thin red lines on the bottom half indicate the PHENIX muon arm acceptance for an

“interaction diamond” of  $z = \pm 10$  cm. The black rectangles represent the envelope for the VTX, where clearance for the 3 cm diameter Be beam pipe defines the inner surface of this envelope, while space for future detector upgrades constrains the outer surface.

### B. Mechanical Integration

The core mechanical design team for the VTX detector has been assembled. Don Lynch (BNL), the new chief mechanical engineer for PHENIX, will coordinate VTX integration effort with LANL engineers Walt Sondheim and Jan Boissevain. Robert Pak (BNL) and Dave Lee (LANL) will provide oversight. CAD tools at LANL were used to produce the 3D views of the VTX detector shown in Figure 10.

The right-hand diagram of Figure 10 is a refinement of the cross-sectional view in Figure 9, showing possible routings for cabling and cooling of the barrel layers. Two possibilities are shown: the inner layer services are routed along the beam pipe, while services for layers 2, 3 and 4 are routed out along a direction roughly corresponding to  $y=1$ . No support structures, or services for the endcap, are shown. The left-hand diagram is a perspective view demonstrating how services are brought in radially at both ends, using the entire perimeter.

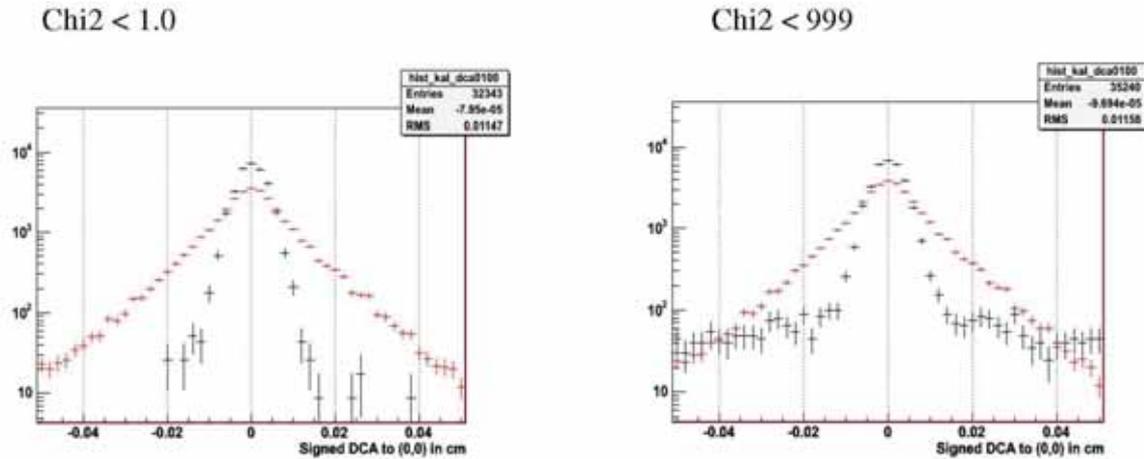


**Figure 10 3D models of the VTX detector.**

## **1.4 Software**

### A. Simulation study --- Kalman fitting

A track fitting code using a Kalman filter technique has been developed for the VTX detector by Iowa State University group. In this code, a track reconstructed from the PHENIX central arms is projected on the VTX detector and is associated with the hits on the silicon detector layers. Then the distance of the closest approach (DCA) of the track to the primary collision vertex is calculated. The new code performed a global fit of the hits in VTX tracker and the track reconstructed in the PHENIX central arms. The effect of the multiple scattering is taken into account in the global fit.



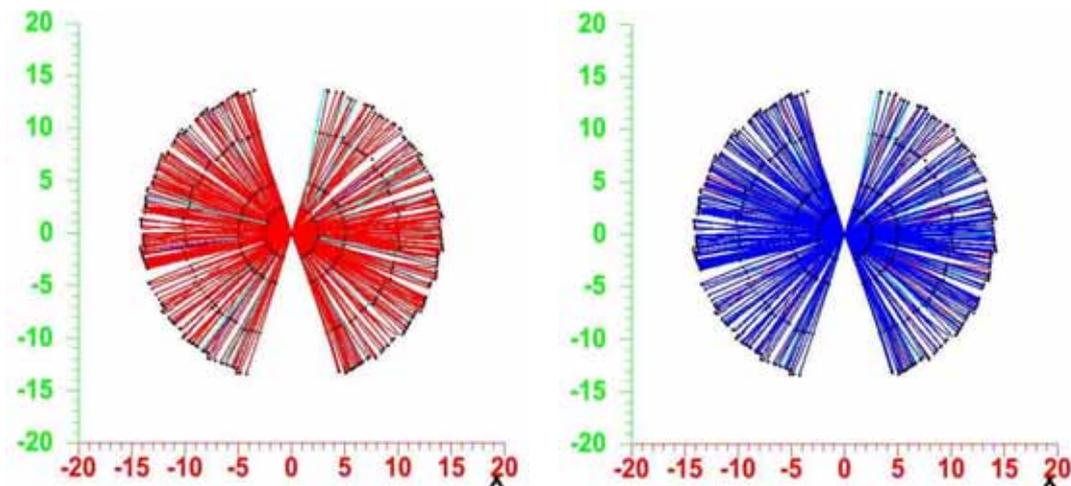
**Figure 11** DCA distribuion of tracks from  $D^0$  decays (red) and that from primary vertex (black) from simulation. In the right panel, a very loose chi-squares cut is applied, while a tight chi-squared cut is applied in the left.

The code is evaluated using the simulated events from a GEANT simulation of VTX detector in PHENIX. The simulated tracks are reconstructed by the standard PHENIX reconstruction program, and then they are connected with the VTX detector using the Kalman fit program. Results from the simulation are shown in Figure 11. In both panels of the figure, the black histograms show the DCA distribution of the tracks from the primary vertex in simulated central Au+Au collision events, and the red histograms show that of charged tracks from simulated  $D^0 \rightarrow K\pi$  decays. In the right panel, very loose chi-squares cut ( $\chi^2 < 999$ ) is applied, and the DCA distribution of the primary tracks has a very long tail caused by high multiplicity of the event. This long tail would prevent clear separation of charm decay tracks from background tracks. In the left panel, the tail is cleaned up by a tight chi-squares cut, and the primary vertex has a Gaussian DCA distribution. The simulation demonstrates that VTX detector can clearly separate charm decay tracks and background tracks.

### B. Self tracking program of the VTX

In the Kalman fit program described above, a track is first reconstructed by the PHENIX central arms and then associated with the hits in the VTX detector. Thus the VTX detector can be used only those tracks that are reconstructed by the PHENIX central arms. The code also requires that the position of the primary vertex is known, and the vertex position have to be determined by a separate program.

In parallel to the Kalman fit program, a new tracking code for the VTX is being developed by Stony Brook University group. The code reconstructs the tracks from the hits in the VTX detectors only, and it finds the position of the primary vertex. Some initial results from the self-tracking program are shown in Figure 12. The program could reconstruct tracks with high efficiency (about 90%) in central Au+Au collision events.



**Figure 12** An event display of a simulated central Au+Au collision event. Left. Real (simulated) tracks are shown in red. Right: The reconstructed tracks in the same event are shown in blue.

## 1.5 Project

### New collaboration Institute

In January 2005, Ecole Polytechnique (France) group officially joined to the pixel detector subsystem. The group has 2 electronics engineers, 5 physicists, and 1 graduate students working on the project. The group also has their own budget of about 100K euros contributing to the pixel project. They now take responsibility of SPIRO module of the pixel read-out chain.

### New collaboration member

Robert Pak is now officially a member of PHENIX. The rest of BNL Chemistry Group will officially join PHENIX soon.

## 2. Updated cost and schedule

We have a review on January 19/20 2005. There are two major recommendations from the review panel.

- *The schedule proposed for this project, with a completion date in January 2008, is driven by a strong desire to utilize this detector for a high-statistics gold-beam run in 2008-2009. We find this schedule to be very aggressive. We recommend that the group re-examine the project schedule – taking account of the detailed recommendations given in the following sections of this report – without constraining the completion date to meet a specific goal of the RHIC operations plan.*
- *We find that the cost estimate for the project is well considered, and is based on sound practices for developing a project of this type. The materials budget appears to be credible. The labor cost should be re-evaluated after an updated schedule has been prepared. While we do not expect dramatic changes in the total cost estimate for the project, it is important to demonstrate that a realistic schedule, with appropriate schedule contingency, can be accommodated within the final cost estimate.*

The review panel also recommended as follow:

- *Define the scope of the project to be complete when the tested detector is ready to be brought into PHENIX and installed. Do not include installation or in-beam commissioning tasks that depend on the operations schedule of PHENIX and RHIC.*
- *The WBS schedule should be updated as soon as possible to include the following...*
  - *Full resource loading*
  - *Physicist and student effort, even though these do not contribute to the cost. In many places we were told that these would augment the efforts of engineers and technicians. These hours should be counted.*
  - *Identify schedule float and contingency explicitly. There should be ~30% schedule contingency identified, and a plan for managing and updating this throughout the duration of the project. Make sure there is enough contingency in the labor cost to cover the schedule contingency.*
  - *Check to ensure realism in the details of the schedule. Start tasks after some parts are in hand, rather than after all are in hand, consistently through the project. Make all contingency explicit. Include time for training personnel (e.g. wire bonding, ROC assembly).*
  - *Develop (and study) labor profiles.*

Following these recommendations, we have updated the cost and schedule. The main points of the updates are:

1. A reduced budget of \$1M for FY06 is assumed. This is the most optimistic scenario and requires a favorable DOE Nuclear budget from Congress. Other

- tasks were delayed to the start of FY07.
2. With these assumptions and with the addition of schedule contingencies (see below) the project now takes three years to complete (FY06, FY07, FY08).
  3. The extension of time has had a small impact on the cost. The two items that increased were the only two “standing” salaries of the two electrical and mechanical system engineers which were extended from approximately 28 months to 36 months. The earlier proposal already contained a 12 month contingency on these two salary lines.
  4. A full bottoms-up risk analysis was performed following the model presented to and approved by the Review committee. Three categories of risk were assigned for each task (cost risk, technical risk, and schedule risk) and used to calculate both a cost and schedule contingency for each item. This has led to some items being assigned more cost contingency, others lower contingency, depending on the total risk.
  5. Following the recommendation of the committee, explicit schedule contingencies (based on the above risks) were added to the project.
  6. The 2<sup>nd</sup> round strip-ROC development is now made with regular PCB and a later round with Kapton PCB is now scheduled and budgeted.
  7. The installation tasks and costs are now separated out as pre-ops costs and the construction deliverable is a completed VTX ready for installation.
  8. The manpower for the installation of Low Voltage power supplies, racks, services etc. to be covered by the PHENIX operations budget. The equipment for these to be covered by the VTX budget.
  9. Various small bugs in the schedule that were identified during the review were fixed

With all the above changes, the total change in the budget is +\$100K with the new budget (including contingency) now being \$4.4M.

Some of the recommendations (resource loading, progress tracking) by the review panel have not been incorporated due to lack of time at this moment. We will incorporate them in the project in coming few months.

### **Impact of FY07 Start**

There is a possibility that funding can only start in FY07. Assuming a 2 year funding profile, we should still be able to complete the project by the end of FY08. Some adjustments must be made, specifically to keep research and development work for the critical path items on track. The necessary funding during FY06 needs to be made available through either R&D funds or operation capital at BNL. The work included in our current planning for FY06 goes beyond the development of components and includes for a number of critical path items the start of production. This would need to be delayed if funding starts in FY07 rather than in FY06. We foresee that the completion of the project can be delayed by a few months but probably by much less than a year. We do note however that there is less scheduling contingency if the project is funded in FY07/08 and thus a start in FY06 is much more desirable.

## Updated Budget

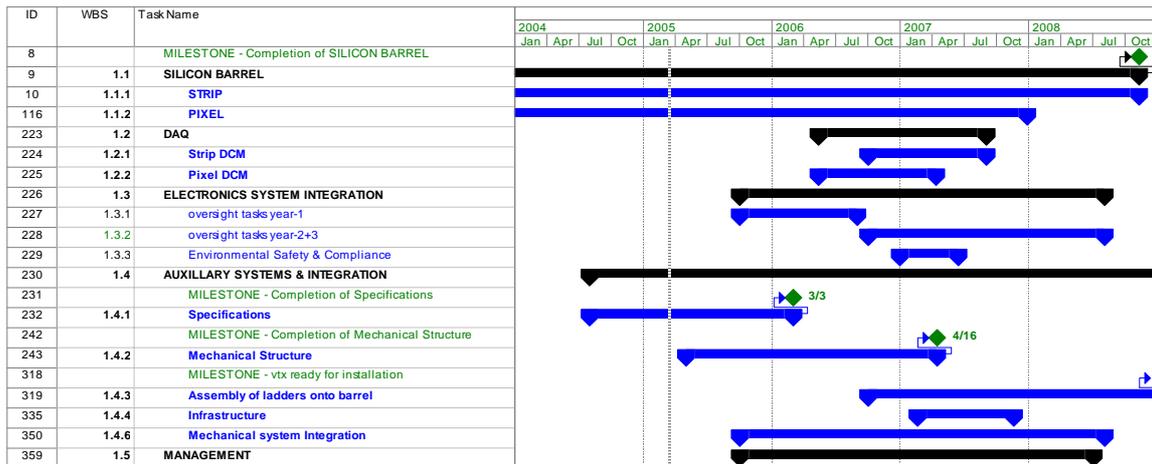
Table 1 summarizes the estimated costs for the VTX project and shows the split between the two funding agencies. For those items for which we seek funding through the DOE, a detailed cost-breakdown is given in Table 2. The cost of the DOE is after the start of the construction in FY06. The cost of the R&D performed using the generic detector R&D fund in FY04 and FY05 is not included.

## Updated Schedule

The overall schedule to complete the VTX detector upgrade for PHENIX is summarized in Figure 13. It assumes start of the DOE construction project in FY06. The subsequent plots, Figure 14 to Figure 16, show the detailed schedule for each major WBS element. The schedule after year 2004 is shown. Figure 17 gives the funding profile for the DOE project.

**Table 1 Overview of the total estimated cost for the VTX project. The DOE cost does not include the R&D in FY04 and FY05.**

WBS	Name	DOE	RIKEN	TOTAL
1.1.1	Strip	1,673,458	1,210,000	2,883,458
1.1.2	Pixel	0	1,650,039	1,650,039
1.2	DAQ	115,813	85,625	201,438
1.3	Electronics System Integration	600,000		600,000
1.4	Auxiliary System & Integration	1,953,864	70,800	2,024,664
1.5	Management	83,952	0	83,952
	<b>Total</b>	<b>4,427,087</b>	<b>3,016,464</b>	<b>7,443,551</b>



**Figure 13 The overall schedule for the VTX project.**

**Table 2 Cost breakdown for tasks to be funded through the DOE. Tasks which do not show a cost correspond to deliverables for which the RIKEN Institute will take fiscal responsibility. The table also does not contain the R&D cost before the start of construction.**

WBS	Name	Fixed	Labor	DOE	Transfer overhead	Contingency percentage	DOE contingency	Total DOE
1.1.1	STRIP							
1.1.1.1	Strip FEE	555,363	373,853	929,216	70,302	32%	315,224	1,314,742
1.1.1.2	Strip Sensor	27,171	0	27,171	1,652	32%	8,647	37,470
1.1.1.3	Strip System test	27,295	43,750	71,045	3,038	34%	25,521	99,603
1.1.1.4	Assembly and Testing of Strip	41,125	35,000	86,125	0	43%	36,818	122,943
1.1.1.5	Services, LV, racks etc	65,800	0	66,000	0	50%	32,900	98,700
	Totals	716,754	462,603	1,179,357	74,992	33%	419,110	1,673,458
1.1.2	PIXEL							
	Totals	0	0	0	0	0%	0	0
1.2	DAQ							
1.2.1	Strip DCM	55,000	30,000	85,000	7,650	25%	23,163	115,813
1.2.2	Pixel DCM	0	0	0	0	0%	0	0
	Totals	55,000	30,000	85,000	7,650	25%	23,163	115,813
1.3	ELECTRONICS SYSTEM INTEGRATION							
	Totals	0	425,000	425,000	0	41%	175,000	600,000
1.4	AUXCILARY SYSTEMS & INTEGRATION							
1.4.1	Specifications	0	0	0	0	0%	0	0
1.4.2	Mechanical Structure	372,500	230,500	603,000	60,300	31%	208,065	871,365
1.4.3	Assembly Of Ladders onto Barrel	43,076	32,500	75,576	3,263	29%	23,023	101,862
1.4.4	Infrastructure	118,375	110,000	228,375	0	30%	68,513	296,888
1.4.5	Mechanical System Integration	0	515,000	515,000	0	33%	168,750	683,750
	Totals	533,951	888,000	1,421,951	63,563	32%	468,351	1,953,864
1.5	MANAGEMENT							
	Totals	0	60,000	60,000	3,600	32%	20,352	83,952
	Totals	1,305,705	1,865,603	3,171,308	149,804	33%	1,105,975	4,427,087

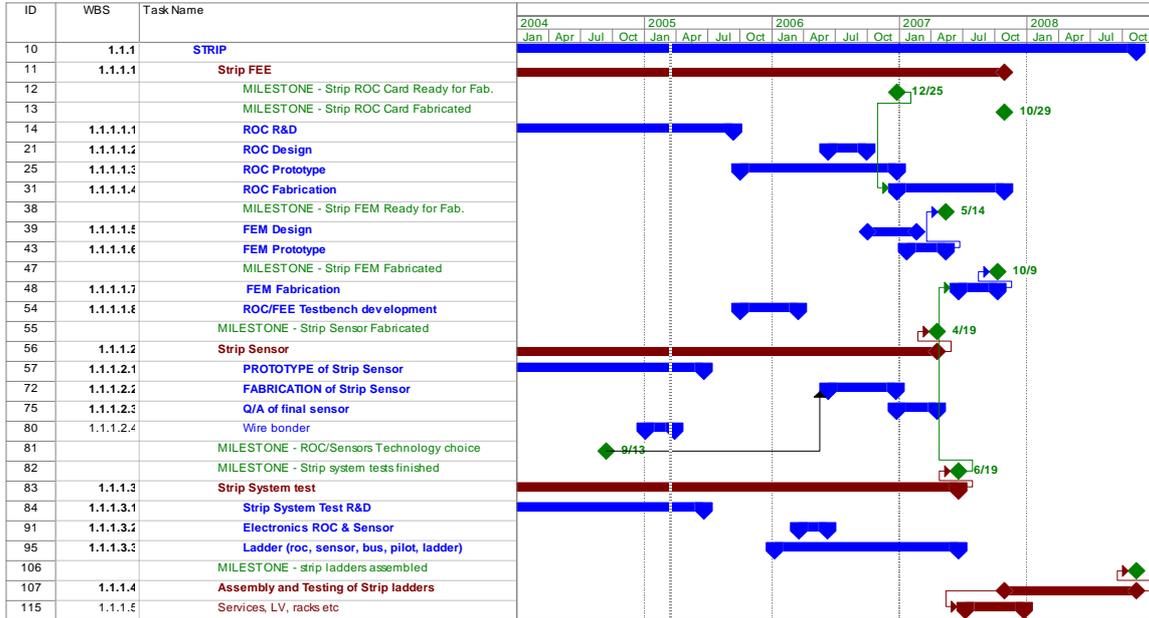


Figure 14 The schedule for the strip layers

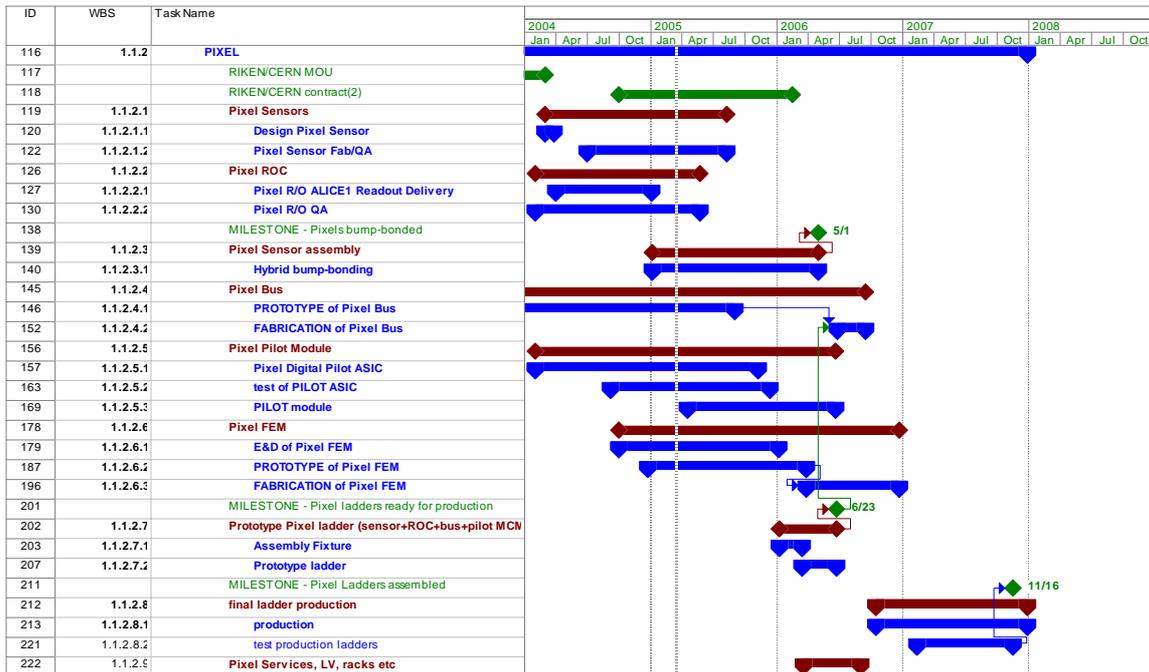


Figure 15 The schedule for the pixel layers

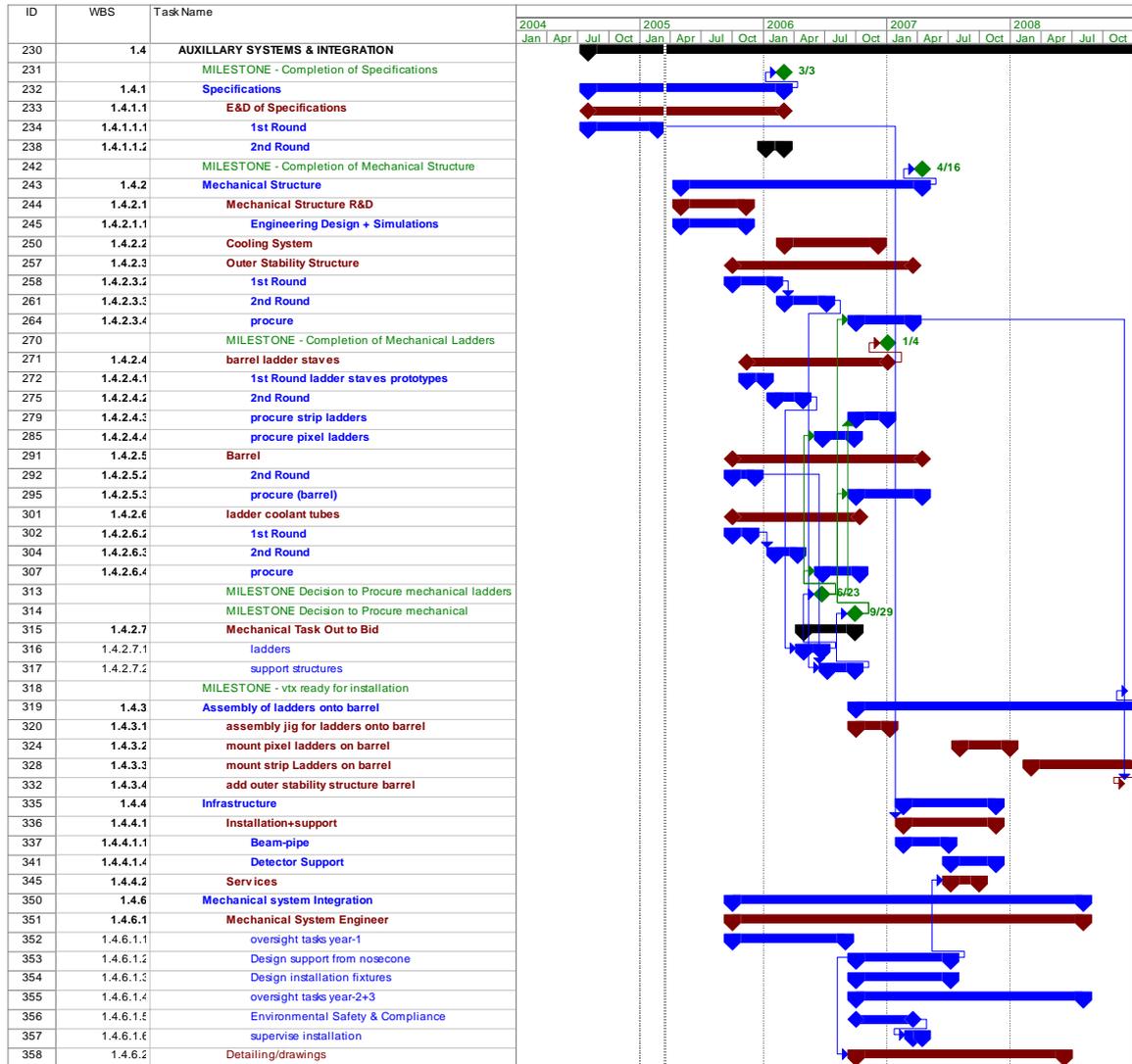
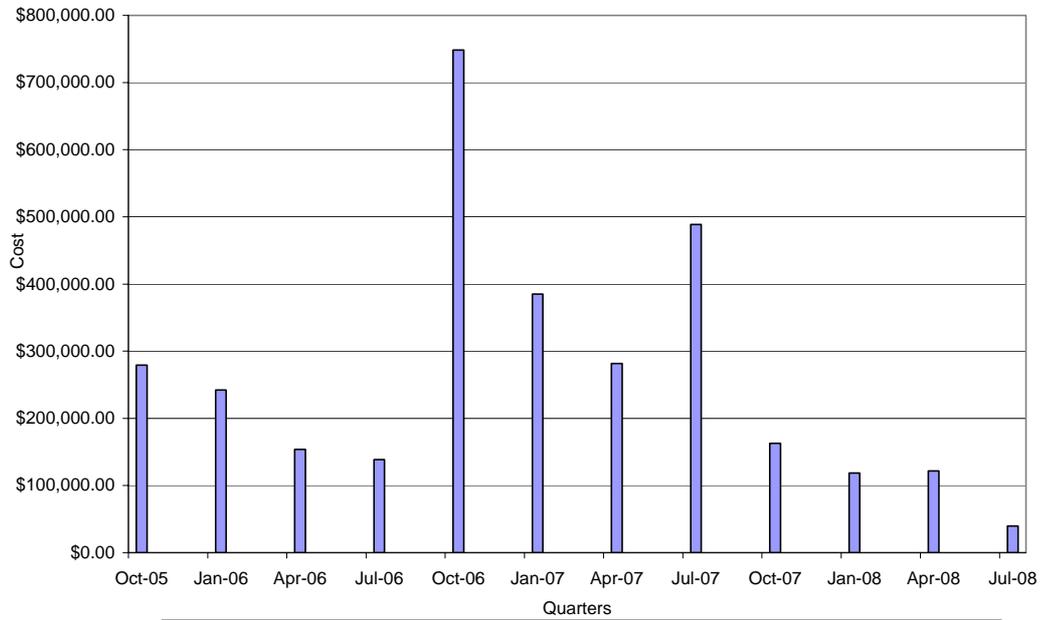


Figure 16 The schedule for the auxiliary and integration



DOE Construction Costs (without contingency) per Quarter

Figure 17 The cost profile of the project

### 3. Answers to the technical issues in the Review Report

#### **Silicon Strip Layers**

1. *The Al/Kapton circuit may not fabricate*
2. *A Cu/Kapton backup design circuit may not fabricate or require excessive iterations to succeed. (Note recent experience of ATLAS and CMS in this regard).*

#### **Strip ROC**

*The Al-polyimide circuit is not as aggressive the Pixel Bus. If Soliton can fabricate the Pixel Bus then they should be able to fabricate the Strip-ROC circuit as well. However, to meet the schedule there should be a plan to have a parallel non-polyimide solution. This would be valuable for testing even if the polyimide solution works well eventually. Design details will probably require a good deal of physicist input, and that needs to be included in the plan.*

#### **Answer:**

We understand the review committee's concern about the Kapton circuit board. However, we should point out that we are not pushing the technology envelope for the strip ROC. The Kapton circuit board used in the strip ROC is significantly less challenging than the thin Aluminum bus that we are developing for the pixel layers. For instance, 100 micron trace width and 100 micron space is much less demanding than the fine pitch required for the pixel bus and is perfectly acceptable for the ROC. We can also use Cu traces instead of Al, at the cost of a somewhat worse radiation length budget. In PHENIX, we are using a Kapton PCB for our Pad Chamber subsystem for 10 years and we are confident that we can fabricate the Kapton board. Nevertheless, we also understand the concern by the review panel and the need for a conservative back-up plan that is guaranteed to work.

Following the recommendation, we have added an additional round of prototype effort in the ROC development. The review committee strongly endorsed development of a scale-size prototype as soon as possible. In order to avoid complications and delays in going to a Kapton implementation at the next round of prototype effort we will instead go first to a scale-size prototype implemented as a conventional PCB material, but as thin as possible. Commercially available boards can be fabricated with copper layers as thin as desired (although not aluminum) and the insulating layers are somewhat thicker than for a Kapton board, but they are not a dominant component of the material budget. The design of the circuit and the RCC ASIC will be the same in the two versions, with the only difference being the technology for the board. In this way, we can develop a very conservative back-up solution without delaying a full system test. We will perform a full system chain test in both versions, and we will make the decision on which technology we use in the production based on the outcome of the system test. Note that we plan one more round of development (pre-production) after this technology choice is made. We believe that we can safely accommodate any adjustment needed in this

pre-production stage regardless which technology we chose. We have updated the project file and included this conservative back-up solution.

If we chose a conventional PCB solution for the ROC, the largest concern is that it will certainly increase the radiation length of the ROC, which has negative impact on the detector performance. Since the strip detectors are used in the outer two layers of the VTX, its impact on the DCA resolution is minor. Monte Carlo simulation study we have done shows that the DCA resolution is determined by the inner two pixel layers. Additional thickness in the strip layers will increase the conversion background to PHENIX central arms and will worsen the momentum resolution of central arm tracks and VTX only tracks. These are undesirable consequence of thicker ROC, but we think they are acceptable. We will evaluate the impact of thicker ROC by a detailed Monte Carlo simulation.

*3. The ROC as power bus may have excessive voltage drops*

**Answer:**

We have evaluated the voltage drops in the power bus in the ROC. Our conservative estimate of the voltage drop in the bus is 60 mV, which is acceptable.

*4. ROC as power/signal bus incorporating 12 chips may be vulnerable to single point failures.*

**Answer:**

We will mitigate this in the design in a couple of ways. We decouple the serial string through the RCCs. We will also make the bus pads (which connect two ROCs) large enough for several wire-bonds. In the current design this still leaves us vulnerable to two different failure modes.

A) A chip fails in such a way that power and ground are short circuited.

B) An RCC fails in such a way that its data readout token signal is not passed.

We will investigate the likelihood of A. If this sort of failure is a serious concern, as evidenced by operational experience in CDF and D0, we could bring power down the ladder independently for the different ROCs. We will investigate designs which allow bypassing of a particular RCC, thus eliminating B as a concern.

*5. Low noise/low pickup requirements for analog measurements may be undermined by behavior of ROC and bus on top of silicon strips*

**Answer:**

CDF had their digital bus running directly on top of their sensors. It is true that we will have a more significant noise source both because the digitization process from all the chips occurs in parallel and because the digitization clock is at a higher speed than the readout clock. However, all of these clock lines are implemented in differential logic

(LVDS). CDF found that the most significant noise sources were the handful of SVX4 signals implemented in single-ended logic. These are present both on the bus and in the chip and they found that a shield layer eliminated problems from this noise source. Following the recommendation by the review, we will implement a similar shield. The noise problem will also be investigated by the system test using the second prototype on the top of the sensor.

*6. Lack of substrate and proximity of conducting layers to strips adds significant source capacitance to each input channel.*

**Answer:**

Again, this problem will be investigated by the system test using the second prototype on the top of the sensor. Investigation of the RC decoupling chip subsequent to the review showed that this chip will be too large to mount on the board. One mounting solution is to place this chip between the sensor and the SVX4 so that it would serve as a pseudo substrate.

*7. Impact of test and rework could be excessive.*

**Answer:**

When CDF fabricated 4-chip hybrids using tested boards and tested chips they found ~89% initially successful yield. Approximately ~4% were repairable, but ~4% were damaged in the subsequent encapsulation process. Assuming that yield scales with the power of the number of chips on the hybrid we expect our 12-chip hybrid to have an initially successful hybrid yield of ~70%. Our hybrids also include the RCC chip, so this is probably a slight overestimate. We further expect ~10% will have repairable problems and that we will lose roughly 10% in encapsulation.

Fortunately this project requires a relatively small number of hybrids (244 total) and we believe that our production testing schedule allows time to test and fix the required number of extra boards. We will continue to explore options for reducing the number of SVX4s on a single hybrid, but all options conceived of to date require a significant increase in the material budget.

*8. Impact of detector bias and local bypass at ROC on ladder design*

**Answer:**

This part of the design has not been completed. We are investigating the best solution of how to bring the bias voltage of the sensor on the ladder.

**AC Coupling (of the strip sensor)**

*A decision needs to be made soon to use either AC or DC coupling of the strip sensors*

*to the SVX4 chip. If AC coupling is the choice, this may have an effect on cost and schedule. Note that the number of wire bonds increases by almost a factor of two for the AC case, lowering the ROC yield, but operational stability gains may make that a good trade-off.*

**Answer:**

We are aware of that this critical decision should be made as soon as possible. One of the main purposes of the system test of the first prototype ROC is to measure the S/N performance with AC and DC coupling. The AC/DC decision will be made based on the results of the test, which is scheduled in March/April 2005. We have also started the design of the RC chip with HPK.

**RCC (of the strip ROC)**

*The conversion from working VHDL code to ASIC should be relatively straightforward and the VHDL can be tested on the prototype that is now being assembled. Note that some of the schedule and cost risk for this process can be mitigated by extensive careful simulation prior to ASIC submission.*

**Answer:**

The ORNL engineers that will work on the development of the RCC ASIC have previous experience for a similar conversion of VHDL code to ASIC. We plan to have careful and extensive simulations prior to ASIC submission.

**Pixel Bus**

*This is technically very aggressive. Good progress has been made on a preliminary proof of principle. We strongly encourage continued work with Soliton (a manufacture of flexible PC boards). Previous experience in the community with polyimide has been mixed, and back-up solution should be pursued in parallel (which may have an adverse impact on the material budget).*

**Answer:**

We are well aware of the technical challenge of the pixel bus. In fact, we consider this to be the most critical item in the pixel project. To reduce risk for the project, we now plan two steps in the development of the pixel bus. In the First step, we make pixel bus with Cu-Polyimide. Multilayer Cu-Polyimide flexible cables with fine pitch and high density traces that meet our requirement are commercially available in these days in the market. Moreover, it should be noted that the ALICE pixel group has produced Cu-Polyimide bus with 40 micrometer wide signal traces and with pitch that is somewhat larger than our requirement. The bus has been build and tested with a real silicon pixel detector in a test beam last year, and it worked fine without any problem. The Multilayer Cu-Polyimide bus for PHENIX pixel detector is now scheduled to be delivered by the end of June, and the first electrical test of pixel bus itself and an integrated test with a real silicon pixel detector is now scheduled on July and August 2005. In the second step, Al-Polyimide multilayer pixel bus production will follow once

we confirm that there is no major defect in the Cu-Polyimide bus from the electrical test. The Multilayer Al-Polyimide pixel bus will be produced using the same masks and almost identical techniques that will be used for the Cu-Polyimide bus. Furthermore, a parallel R&D project to produce Al-Polyimide flexible cables is on going at KEK with another company by our collaborator. The progress is almost at the same level as that of the Soliton R&D project that was presented in the review.

### **Digital Pilot Chip**

*This is technically not very risky, and ongoing tests may show good results within weeks. Radiation hardness specification was not addressed in the presentation to the Committee. Is there a Single-Event Upset problem? What is the testing plan?*

#### **Answer:**

A test on the Single-Event Upset(SEU) of the pilot chip ASIC for the ALICE experiment has been carried out by ALICE silicon pixel group. The tested ASIC is made with the same radiation tolerant technology in IBM processes that used for the PHENIX pilot ASIC. They bombarded 58 MeV proton beam on the ASIC with integrated dose of about  $3.5 \times 10^{12}$  protons/cm<sup>2</sup>. This amount of exposure corresponds to 500 krad of the radiation dose. 4 SEU has been observed during this test, and SEU/Integrated-Flux found to be  $(11.5 \pm 5.8) \times 10^{-9}$  cm<sup>2</sup>. A similar test of the PHENIX pilot ASIC is now under consideration. We are planning to carry out a radiation hardness test of our ASIC in July-August 2005.

### **Front End Module (of the pixel layers)**

*Still at the conceptual stage; unlikely to be high risk item.*

#### **Answer:**

Two engineers at Stony Brook University have started the design work of the Pixel FEM. One of the engineers is the main person who developed the Front End Module of the PHENIX Drift Chamber.

### **Other electronics issues**

*It may be prudent to include a radiation testing step on completed ladders.*

#### **Answer:**

We will consider a radiation hardness test of completed ladders.

*Power supplies need to be addressed for a complete system. There may be some surprises here.*

#### **Answer:**

Steve Boose (BNL), an electronics engineer who worked on all of the PHENIX power supplies, has started working on LV and HV power supply and rack space issues.

### **Cabling**

*The design is largely conceptual, and needs work, but is unlikely to be a large risk factor. Mechanical interferences close to the ladder may be an issue.*

### **Cabling and cooling**

*The design is largely conceptual and needs work. The concern is mostly in the region of highest density just off the ends of the ladder adjacent to the planned endcaps. Care needs to be taken not only to avoid interferences in the assembled detector, but also to avoid interferences during the actual assembly and to facilitate ease of assembly.*

#### **Answer:**

Two LANL engineers have started working on the routing of cables and cooling tubes using a very detailed 3D CAD model. The 3D model, when it is completed, is to include all cables, cooling tubes, and all other services that are needed for the VTX. This pre-design engineering step is included in the project.

### **Grounding and Shielding**

*A plan for system wide grounding and shielding was not presented in the review nor in the proposal. Grounding and shielding couples directly to the mechanical design in terms of materials chosen for the support structures and how the support structure will, if at all, be grounded. It also couples directly into the ladder power and signal schemes.*

#### **Answer:**

The grounding and shielding issue is very important. The electronics system engineer will work on this issue.

### **Alignment**

*An understanding of the sensor-sensor intra-ladder alignment requirement and ladder-to-ladder requirements must be quickly established based upon physics requirements. The precision of the required alignment greatly influences the mechanical design and assembly procedures. Realistic Monte Carlo simulations that include non-perfectly placed components and include software alignment procedures will greatly aid in this understanding.*

#### **Answer:**

The 25 micron internal alignment comes from the required precision of the DCA measurement. It should be noted that the NA60 experiment, which uses the same pixel device as ALICE and PHENIX, achieved inter-layer alignment of better than 10 microns in the offline analysis stage. Therefore, we think that a similar level of the pixel-to-pixel and pixel-to-strips alignment can be achieved for the PHENIX VTX. We have implemented a detailed GEANT model of VTX in the standard PHENIX Monte Carlo simulation program, PISA. The offline alignment program will be developed using the GEANT program.

*The Committee also suggests that the mechanical support group consider building a*

*model of the VTX detector as soon as practical. This will be useful in developing plans for support of the detector, for cable and cooling tube routing, and discovering the interferences.*

**Answer:**

We are making 3D CAD model to study the support, cabling, cooling etc. We will make a mechanical mock-up when this design work was completed.

- The project should produce a “requirements document”, or parameter book, that provides the basis for setting the key specifications, especially those that are cost drivers. For example: Have the alignment specs for sensors and ladders been incorporated into tracking studies? Did they come from tracking studies? How was the allowable heat generation arrived at? What is the justification for the chosen operating temperature? What are the criteria for making decisions that involve increasing the material budget?

Answer: We are preparing the requirement document and parameter book as requested by the review. This has not been completed due to lack of time, but we will produce it in coming few months.

# Appendix      Review Report

## Project Readiness Review of the PHENIX Barrel Vertex Tracker

January 19-20, 2005

Reviewers: Brenna Flaughner (Fermilab), Carl Haber (LBNL), David Lynn (BNL), Venetios Polychronakos (BNL), Rick Van Berg (Univ. Pennsylvania)

BNL Convenor: Thomas Ludlam

### Overview and summary

The Silicon Vertex Tracker (VTX) is proposed by PHENIX to provide precision tracking of charged particles at radii close to the collision axis with accuracy sufficient to resolve the displaced vertices of charmed particle decays in high energy collisions at RHIC. This capability adds an important new element to the physics reach of PHENIX, both for the study of phenomena related to the formation of quark gluon plasma in heavy ion collisions and for the study of the spin dependence of the interaction in polarized proton collisions.

The proposed detector is comprised of four cylindrical layers of silicon sensors, with inner radius of 2.5 cm and outer radius of 14 cm. The inner two layers use silicon pixel technology adapted from the hybrid-pixel design being implemented at CERN for the ALICE experiment. The outer two layers utilize a novel strip detector configuration, with stereoscopic strips, 80  $\mu\text{m}$  by 3 cm, giving effective 2-dimensional readout with high resolution. This technique, developed by the BNL Instrumentation Division, is being implemented for the first time in this detector. The strips are read out using the LBNL-Fermilab SVX4 chip.

An early conceptual design for this detector was reviewed by BNL's Detector Advisory Committee (DAC) in November 2003, resulting in a number of detailed questions relating to the technical implementation and to the planned management of the construction of the device within the PHENIX collaboration. The present proposal, submitted to BNL in July 2004, has been modified to address the recommendations of the DAC review. The proposed project would be jointly funded by DOE and Japan (RIKEN). The total cost estimate is \$7.3M, with proposed DOE funding of \$4.3M. The Japanese responsibility is primarily for the fabrication of the pixel layers, while the U.S. responsibility is primarily for the fabrication of the strip layers, the mechanical structure, and the overall mechanical and electrical integration. The stated goal of PHENIX is to begin this project in FY 2006, and complete the detector in FY 2008.

The purpose of this review was to evaluate the technical feasibility of the design, and its readiness to begin construction on the proposed time scale, and to provide an assessment of the cost and schedule for the project as proposed by PHENIX. The agenda for the review is given as Appendix A.

#### Summary of findings and recommendations:

- The Committee finds that the proposed project is well advanced in its development, and is technically feasible. Though some important technical challenges remain, we believe that the well-organized team put together by PHENIX for this project is capable of dealing with them. Some specific technical issues are listed in this report. We note that, in addressing these issues, the VTX group will very likely find it necessary to modify the work plan.
- The schedule proposed for this project, with a completion date in January 2008, is driven by a strong desire to utilize this detector for a high-statistics gold-beam run in 2008-2009. We find this schedule to be very aggressive. We recommend that the group re-examine the project schedule – taking account of the detailed recommendations given in the following sections of this report – without constraining the completion date to meet a specific goal of the RHIC operations plan.
- We find that the cost estimate for the project is well considered, and is based on sound practices for developing a project of this type. The materials budget appears to be credible. The labor cost should be re-evaluated after an updated schedule has been prepared. While we do not expect dramatic changes in the total cost estimate for the project, it is important to demonstrate that a realistic schedule, with appropriate schedule contingency, can be accommodated within the final cost estimate.
- Overall, we find that this project has been brought to a state that can meet the requirements for a DOE Major Item of Equipment project, to be funded in FY 2006. We recommend that PHENIX present to BNL management an updated schedule and cost estimate, addressing the detailed recommendations of this report, within the next few months. The timing of this update should be coordinated with BNL, and with DOE, to facilitate a successful cost/schedule “baseline” review to initiate the project.

#### **Technical Assessment**

This project has benefited from a great deal of R&D and simulation effort within the PHENIX collaboration. The basic design is sound, and well matched to the PHENIX detector and its research goals. Several key components are borrowed from other efforts, providing some aspects of the project with a jump-start that avoids significant design costs and reduces risk. (For example, the Pixel Readout chip and SVX4 satisfy a great deal of the readout chain.) In our specific comments we focus on those areas where the Committee feels the project is breaking new ground, and has a greater exposure to technical risk.

The silicon strip and pixel ladder designs include many advanced concepts. A successful implementation of these will no-doubt be viewed as a significant achievement and will influence future designs in other experiments. Because of these advanced concepts, certain technical risks are assumed. Wherever possible, these should be mitigated by conservative back-up solutions pursued in parallel. The impact of these backups and other delays incurred in making the baseline advanced concepts work must be included in the work plan, the schedule, and the cost. We list here some of these advanced concepts, for the strip layers. (A similar list could be made for the pixels. We focus on the strips, which are the responsibility of the DOE funded portion of the project.):

1. Use of 2D detectors
2. Al/Kapton circuitry utilizing fine pitch, multi-layer constructions
3. Integration of hybrid (ROC) and power/signal bus across a ladder
4. Deadtimeless operation (simultaneous charge acquisition, and digitization/readout) with thin kapton circuits and bussed structures on top of the silicon strips.
5. 12 SVX4 chips on a ROC
6. Assembly of such structures over the full surface of a ladder
7. Repair and rework of such structures.

The resulting technical issues and risks will therefore include,

1. The Al/Kapton circuit may not fabricate
2. A Cu/Kapton backup design circuit may not fabricate or require excessive iterations to succeed. (Note recent experience of ATLAS and CMS in this regard).
3. The ROC as power bus may have excessive voltage drops
4. ROC as power/signal bus incorporating 12 chips may be vulnerable to single point failures.
5. Low noise/low pickup requirements for analog measurements may be undermined by behavior of ROC and bus on top of silicon strips
6. Lack of substrate and proximity of conducting layers to strips adds significant source capacitance to each input channel.
7. Impact of test and rework could be excessive.
8. Impact of detector bias and local bypass at ROC on ladder design

We suggest a comprehensive internal, and then external, review occur of the ROC/ladder concept to account for these and other issues which arise. Such a risk-assessment procedure may be appropriate for other systems as well, as discussed in the following section on Management, Cost, and Schedule. The reviews should result in a revised work plan and a conservative backup plan to account for these potential difficulties.

We recommend an accelerated effort to reach a full ladder system test as soon as possible, with components that as closely as possible approximate the final design, in order to

validate a significant set of the design choices. For example, a copper based ROC utilizing the FPGA version of the RCC, but otherwise dimensionally equivalent, could be more quickly fabricated for such a ladder system test. This is in keeping with our recommendation that more conservative solutions to technically challenging tasks be pursued on a shorter time scale.

Some additional recommendations specific to the ROC/ladder structure include,

1. Implement a shield layer in or below the ROC. Ground to AG at one signal point to avoid current flow.
2. Find a way to distance the ROC bottom plane or shield from the strips to avoid increased capacitance.
3. Explicitly treat detector bias and bypass in ROC design
4. Analyze ROC, ROC + detector, and half-ladder, ladder for testability, rework, and repair scenarios.

The main technical issues for the electronic chain focus on the intermediate pieces between the readout chips and the new Data Collection Module, which handles the back end of the chain and is progressing well:

Pixel Bus - This is technically very aggressive. Good progress has been made on a preliminary proof of principle. We strongly encourage continued work with Soliton (a manufacturer of flexible PC boards). Previous experience in the community with polyimide has been mixed, and a back-up solution should be pursued in parallel (which may have an adverse impact on the materials budget).

Digital Pilot Chip – This is technically not very risky, and ongoing tests may show good results within weeks. Radiation hardness specification was not addressed in the presentation to the Committee. Is there a Single-Event Upset problem? What is the testing plan?

Cabling – The design is largely conceptual, and needs work, but is unlikely to be a large risk factor. Mechanical interferences close to the ladder may be an issue.

Front End Module – Still at the conceptual stage; unlikely to be high risk item.

Strip ROC – The Al-polyimide circuit is not as aggressive the Pixel Bus. If Soliton can fabricate the Pixel Bus then they should be able to fabricate the Strip-ROC circuit as well. However, to meet the schedule there should be a plan to have a parallel non-polyimide solution. This would be valuable for testing even if the polyimide solution works well eventually. Design details will probably require a good deal of physicist input, and that needs to be included in the plan.

AC Coupling – A decision needs to be made soon to use either AC or DC coupling of the strip sensors to the SVX4 chip. If AC coupling is the choice, this may have an effect on cost and schedule. Note that the number of wire bonds increases by almost a factor of two for the AC case, lowering the ROC yield, but operational stability gains may make that a good trade-off.

RCC – The conversion from working VHDL code to ASIC should be relatively straightforward and the VHDL can be tested on the prototype that is now being assembled. Note that some of the schedule and cost risk for this process can be mitigated by extensive careful simulation prior to ASIC submission.

Other electronics issues –

It may be prudent to include a radiation testing step on completed ladders.

Power supplies need to be addressed for a complete system. There may be some surprises here.

The mechanical design is in its preliminary stage and will need to evolve and integrate with the requirements of the overall detector design. Examples of some items that seem currently neglected but are quite important are:

Cabling and cooling - The design is largely conceptual and needs work. The concern is mostly in the region of highest density just off the ends of the ladder adjacent to the planned endcaps. Care needs to be taken not only to avoid interferences in the assembled detector, but also to avoid interferences during the actual assembly and to facilitate ease of assembly.

Grounding and Shielding - A plan for system wide grounding and shielding was not presented in the review nor in the proposal. Grounding and shielding couples directly to the mechanical design in terms of materials chosen for the support structures and how the support structure will, if at all, be grounded. It also couples directly into the ladder power and signal schemes.

Alignment - An understanding of the sensor-sensor intra-ladder alignment requirement and ladder-to-ladder requirements must be quickly established based upon physics requirements. The precision of the required alignment greatly influences the mechanical design and assembly procedures. Realistic Monte Carlo simulations that include non-perfectly placed components and include software alignment procedures will greatly aid in this understanding.

The Committee also suggests that the mechanical support group consider building a model of the VTX detector as soon as practical. This will be useful in developing plans for support of the detector, for cable and cooling tube routing, and discovering the

interferences.

## **Management, Schedule, and Cost**

### Management –

The Committee finds that the management structure presented for the project is a convincing one, with an experienced Project Manager assisted by a capable Deputy. The subsystem structure is good. The responsible people have been identified, and, from the presentations, appear to be in charge. In the pre-construction phase of the project there is good communication among the subsystems and managers – it is detailed and frequent, and well integrated into the management structure of the PHENIX experiment.

### Recommendations:

- A task-by-task risk assessment should be carried out in a way that is consistent across the project. This may be done in a way that is external to the VTX project, but internal to PHENIX or BNL.
- The project should produce a “requirements document”, or parameter book, that provides the basis for setting the key specifications, especially those that are cost drivers. For example: Have the alignment specs for sensors and ladders been incorporated into tracking studies? Did they come from tracking studies? How was the allowable heat generation arrived at? What is the justification for the chosen operating temperature? What are the criteria for making decisions that involve increasing the material budget?

### Schedule –

The schedule as presented, with a completion date of January 2008, is regarded by the Committee as extremely aggressive. In the detailed schedules shown, most (if not all) tasks appear to have no schedule contingency.

### Recommendations:

- Define the scope of the project to be complete when the tested detector is ready to be brought into PHENIX and installed. Do not include installation or in-beam commissioning tasks that depend on the operations schedule of PHENIX and RHIC.
- The WBS schedule should be updated as soon as possible to include the following...
  - Full resource loading
  - Physicist and student effort, even though these do not contribute to the cost. In many places we were told that these would augment the efforts of engineers and technicians. These hours should be counted.
  - Identify schedule float and contingency explicitly. There should be ~30% schedule contingency identified, and a plan for managing and updating this throughout the duration of the project. Make sure there is

enough contingency in the labor cost to cover the schedule contingency.

- o Check to ensure realism in the details of the schedule. Start tasks after some parts are in hand, rather than after all are in hand, consistently through the project. Make all contingency explicit. Include time for training personnel (e.g. wire bonding, ROC assembly).
- o Develop (and study) labor profiles.

#### Cost –

The project cost is split between DOE and RIKEN, with well-defined responsibilities for deliverables. The cost of the pixel layers, funded through RIKEN, is largely based on fixed contracts for which a low contingency is reasonable. The Committee was presented a schedule of DOE labor and material costs that totaled \$4.3M. This includes 40% contingency.

For the DOE costs, the Committee found that the estimates for M&S is generally credible. The cost estimates for labor are less clear: if the schedule is stretched, these may expand. While we do not expect dramatic changes in the total cost estimate for the project, it is important to demonstrate that a realistic schedule, with appropriate schedule contingency, can be accommodated within the final cost estimate.

The project is urged to develop a more complete “cost book”. The level of detail presented for the ROC should be followed for the entire project. Detailed examination by the Committee found that a few items might be missing; e.g. the cost of purchasing the jigs for HYTEC assembly work.

Recommendation: The labor cost should be re-evaluated after an updated schedule has been developed, as discussed above.