

SVX4 Front End

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The SVX4 front end was designed at Fermilab and mates with the SVX4 back end, designed at LBL, to produce a complete SVX4 128 channel silicon detector readout chip. The front end contains 128 identical channels of integrating charge preamp and a 46 cell analog pipeline which is cycled by the beam crossing clock. Hit cells are temporarily removed from the pipeline for readout to the back end, where the data is digitized, sparsified, and read out. SVX4 is “deadtimeless,” so that front end signal acquisition can continue uninterrupted while back end digitization and readout is occurring. Operation of the front end requires only a 2.5V supply, a front end clock, and a few digital control lines.

Description of Front End Operation

The front end has two modes of operation: **Initialize** and **Acquire**.

In **Initialize** mode, the front end clock signal (FEClk) is routed to control a 148 bit shift register, which is downloaded with program bits. 20 of these bits set programmable parameters such as trigger delay, bandwidth, bias current, etc. The remaining 128 bits form a mask register which is used to selectively enable or disable reception of a calibration test charge to each of the 128 preamp inputs. The serial program bit stream line, Srin, actually comes from the back end chip which also has a programmable register. The serial data is clocked into the registers on the rising edge of FEClk. After downloading of the shift register is complete, application of a strobe pulse (via the CalStrobe control line) transfers the 20 programmable parameter bits to a SEU tolerant shadow register. The strobe also resets the pipeline cell position to cell0. Initialization must be performed after power up and before acquisition begins. Although theoretically not necessary, it may be desirable to periodically repeat initialization to insure that the chip remains in a known operating condition.

In **Acquire** mode, the front end clock (FEClk) is routed to the analog pipeline and is used to advance the 46 cells in round robin fashion at the beam crossing rate. At each of the 128 channel inputs, an integrating charge preamp accepts a positive input charge from the detector, and the preamp output feeds the pipeline. The system charge transfer gain is 15 mV/fC. As the pipeline cells are advanced with the front end clock, they perform correlated double samples on the preamp output. A given cell is reset while the front end clock is high, takes a first sample of the preamp output when the clock goes low, and

takes the second sample when the clock goes back high, which also advances the pipeline to the next cell. The voltage difference between the two samples, representing the preamp charge integrated during that time, is thus stored in the cell. The duty cycle of the clock obviously controls the amount of time spent resetting and acquiring on a cell. Typically, the front end clock should have a low duty cycle so that only a small portion of the clock cycle time (minimum 20 ns) is spent resetting, and most is used for acquiring the preamp output. This is desirable since the slower the preamp risetime, the lower is its series noise.

The dynamic range of the preamp (200 fC) is larger than the dynamic range of the pipeline (40 fC), so that many signal charges can be integrated and sampled without saturating the preamp. However, the preamp must periodically be reset via an external control line (PreampReset) in order to prevent eventual saturation. PreampReset is active high, with a minimum required width of 80 ns to achieve complete reset. It is typically performed during beam gaps in order to avoid incurring any deadtime. The timing of PreampReset is not critical, but after reset, one beam crossing time should be allowed for the preamps to settle before inputs can be accurately acquired.

The Level 1 Accept (L1A) control input is used to remove a “hit” cell from the pipeline, with a delay of from 1 to 42 beam crossings, and temporarily store it in a FIFO so that it is queued for readout to the back end. The delay is determined by the value programmed in the shift register during Initialize mode. L1A is normally high during acquisition, and pulsed low to store a cell. L1A must go low and return high between front end clocks, i.e., while FEClk is low. Up to four cells can be stored in the FIFO and queued for readout. If four cells are stored, additional L1As are simply ignored.

A special pipeline cell, the “pedestal cell,” is reserved for acquiring pedestal only. It is used during readout along with a stored cell. The back end essentially digitizes the difference between the hit cell and the pedestal cell. The pedestal cell is not part of the normal round robin of acquisition cells, and so must be explicitly refreshed periodically. This is one of the functions of the PR2 control line. If PR2 is high when FEClk transitions from low to high, then normal acquisition is inhibited for that clock cycle. The normally intended pipeline acquisition cell is skipped over and the pedestal cell instead is placed in the pipeline for acquisition of the pedestal. Thus one cycle of deadtime is incurred by refreshing the pedestal cell. If this is done during a beam gap, deadtime can be avoided.

Operation of SVX4 is “deadtimeless,” so that the readout and digitization process can occur in parallel with normal acquisition. Front end cell readout is accomplished by asserting the PR1 control line in conjunction with FEClk (which continues to control normal acquisition). If PR1 is high at the low to high transition of FEClk (PR1 should then subsequently be lowered), the pedestal cell readout is then initiated. The read amp is reset during the first clock cycle, then the pedestal cell is held in the read amp at the start of the second clock cycle. The read amp output feeds the back end, which uses the pedestal voltage to autozero the ADC. When PR1 is raised a second time, the next FEClk low to high transition removes the pedestal cap from the read amp and initiates readout of

the stored hit cell, which is read out in a manner similar to the pedestal cell. The hit cell voltage can then be digitized by the back end. If desired, the effective signal polarity which is digitized can be reversed by setting the PB parameter bit in Initialize mode. This reverses the readout order to (signal – pedestal) instead of (pedestal – signal). After digitization is complete, the readout cell needs to be removed from the FIFO and placed back into the pipeline. This is accomplished by doing a PR2, which has the dual function of digitally restoring the cell to the pipeline and of retaking the analog pedestal on the pedestal cell capacitor.

In order to facilitate testing, a small charge injection capacitor (25 fF) can be switched in from each preamp input to a common bus line. A 128 bit programmable channel register (downloaded in Initialize mode) can function as a mask register, and determines whether or not an injection capacitor is switched in for each channel. When in Acquire mode, the common bus voltage is determined by the state of the CalStrobe control line. When CalStrobe is low, the common bus is grounded. When CalStrobe goes high, the common bus is connected to the VCAL pad. Thus, raising CalStrobe injects a charge of magnitude $(VCAL)(25fF)$ to each channel which has a mask setting of 0.

Usually it is desirable for all channels on a chip to be functional. However, sometimes “black hole” effects are present in detectors, which result in a DC current being applied to a preamp input. This can effect neighboring channels by turning on input diode protection circuits, which can activate parasitic current paths. Therefore, a provision has been included which allows a selected channel’s preamp reset to be held high, which harmlessly sinks any positive input current to ground without affecting any other channels. This feature is enabled by setting the programmable Mask/Disable bit during Initialize. If Mask/Enable is high, then the 128 bit channel register is used not as a charge injection mask register, but as a channel disable register. Any channel which has its mask bit set high will have its preamp reset held always high.

Powering the SVX4 Front End is very straightforward. An analog power supply, **AVDD**, of 2.5V must be provided for the preamp and the analog sections of the pipeline. This supply is bypassed on chip with an integrated 0.012 uF capacitor. Best deadtimeless performance is obtained if an external 0.1 uF bypass capacitor is added close to the chip (within an inch or so). The front end analog ground is NOT supplied through a pad, but through the low resistance back side of the die. Thus, the die must be connectively attached to a ground plane. A digital supply (DVDD and DGND) is required to drive the pipeline digital logic. This supply is not derived from front end pads, but is routed in from the back end chip digital supply. For deadtimeless operation, AVDD and DVDD should come from two physically separate power supplies. If, however, front end acquisition will not be occurring simultaneously with back end digitization and readout, it may be possible to derive AVDD and DVDD from the same external power supply.

There is an internal master bias circuit on the front end chip which supplies the bias reference for both preamp and pipeline. Preamp and pipeline bias currents can be adjusted via programmable shift register bits. The on-chip bias reference voltage is connected to the **Bias** pad. Under normal conditions, no external bias current reference

needs to be provided. Since the bias circuit is referenced to AVDD, an on-chip Bias to AVDD bypass capacitor is included. An external bypass capacitor from Bias to ground can be provided in order to improve the integrator PSRR. The optimal value of this bypass will depend on the value of the integrator input capacitance to ground (not to neighbor channels).

Two preamp diagnostic bias pads are included on the prototype so that they can be forced if necessary. (Ncas) supplies an internal preamp cascode voltage, and Vrset controls the placement of the DC reset point of the preamp. Under normal conditions, no connection to these pads is necessary.

Several other diagnostic pads are available for chip testing, including (P127), (R127), and (W127). These are buffered versions of the Ch. 127 preamp output, pipeline read amp output, and pipeline write amp output. The buffers are simple PMOS followers which require external bias (a pullup resistor). Without an external pullup, a buffer will be inactive.

Following is a complete list of I/O and bias lines for the SVX4 front end:

INPUTS

Inputs which come directly from front end pads:

In<0:127> -- The 128 preamp inputs. DC input voltage is approx. 0.45V.

Inputs which come from back end pads (through the back end I/O connections):

PreampReset – Front End preamp reset. Active high.

L1A (Level 1 Accept) – removes a pipeline cell from acquisition and stores it in the readout FIFO. Normally high, pulses low between front end clocks to store a hit cell.

PR1 (Pipeline Read bit 1) – used to read out pedestal and hit pipeline cells.

PR2 (Pipeline Read bit 2) – used to refresh the dedicated pipeline pedestal cell.

CalStrobe – transfers programmable shift register data from shift register to shadow register in Initialize mode, applies test input charge to unmasked channels in Acquire mode.

FEClk, FEClkb – Front End Clock. Loads programmable shift register in Initialize mode, advances pipeline and controls acquisition in Acquire mode.

Inputs which are derived in the back end and supplied to the front end:

Srin – Programmable shift register serial bit stream input.

FEMode – Front End mode bit. Low = Initialize, High = Acquire

Useseub – Pulling this high bypasses the SEU shadow register so that the 20 program bits come directly from the shift register output. Defaults low internally.

OUTPUTS

Outputs to the back end:

PipeOut<0:127> -- The pipeline read amp outputs.

CellID<0:5> -- The digital cell number of the pipeline cell being read out.

Srout – Programmable shift register output bit.

Front End diagnostic pads:

(P127) – Preamp channel 127 buffered output.

(W127) – Pipeline channel 127 write amp buffered output.

(R127) – Pipeline channel 127 read amp buffered output.

SUPPLY/BIAS

AVDD – Preamp and pipeline analog supply voltage (2.5V).

Bias – Master bias reference for preamp and pipeline amps. No external current required, external bypass cap to ground can improve integrator PSRR. DC voltage approx. 0.8V.

VCAL – Calibration voltage for test charge injection. Charge injected is $(VCAL) \cdot (25 \text{ fF})$.

Diagnostic supply/bias pads:

(AGND) – Analog ground (supplied through the backside of the die).

(Dvdd) – Pipeline digital supply voltage (from back end).

(Dgnd) – Pipeline digital ground voltage (from back end).

(Ncas) – Internal preamp cascode bias voltage. DC voltage approx. 0.6V.

(Vrset) – Internal preamp reset level bias voltage. DC voltage approx. 1.0V.

Programmable Shift Register bit assignments

0: PB (pipeline readout polarity bit). 0 = pedestal – signal, 1 = signal – pedestal.

1-6: Pipeline level 1 trigger delay. Bit 1 is MSB, bit 6 is LSB. Valid range is 1-42.

7-8: IRSel1-0 (pipeline read amp bias current select). Read amp bias current = 13 uA + (IRSel0)*(13 uA) + (IRSel1)*(26 uA). Increasing the read amp bias current simply speeds up the risetime. The lowest current is probably acceptable.

9-10: IWSel1-0 (pipeline write amp bias current select). Write amp bias current = 26 uA + (IRSel0)*(26 uA) + (IRSel1)*(26 uA). Increasing the write amp bias current speeds up the pipeline reset speed and the pipeline risetime. Nominal bias current = 52 uA.

11-14: ISEL3-0 (preamp input transistor bias current select). Bias current = 164 uA + (ISEL3)*(256 uA) + (ISEL2)*(128 uA) + (ISEL1)*(64 uA) + (ISEL0)*(32 uA).

15-18: BW3-0 (preamp bandwidth). Used to adjust preamp risetime. Risetime will depend on input capacitance, bias current, and bandwidth setting. The bits are binary weighted: BW0 = LSB, BW3 = MSB.

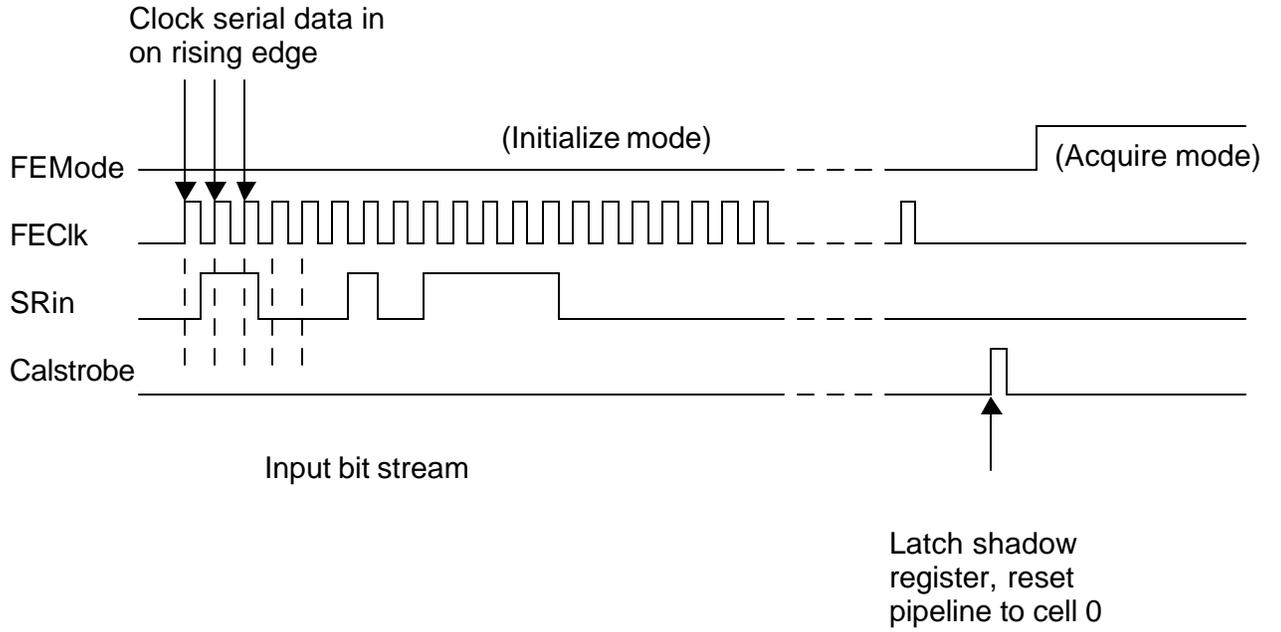
19: Mask/Disable. If Mask/Disable = low, then the 128 bit channel register functions as a mask register for test charge injection (register bit = high to enable charge injection). If Mask/Disable = high, then the 128 bit channel register functions as a channel disable register (register bit = high to disable channel).

20-147: Channel register <0:127>

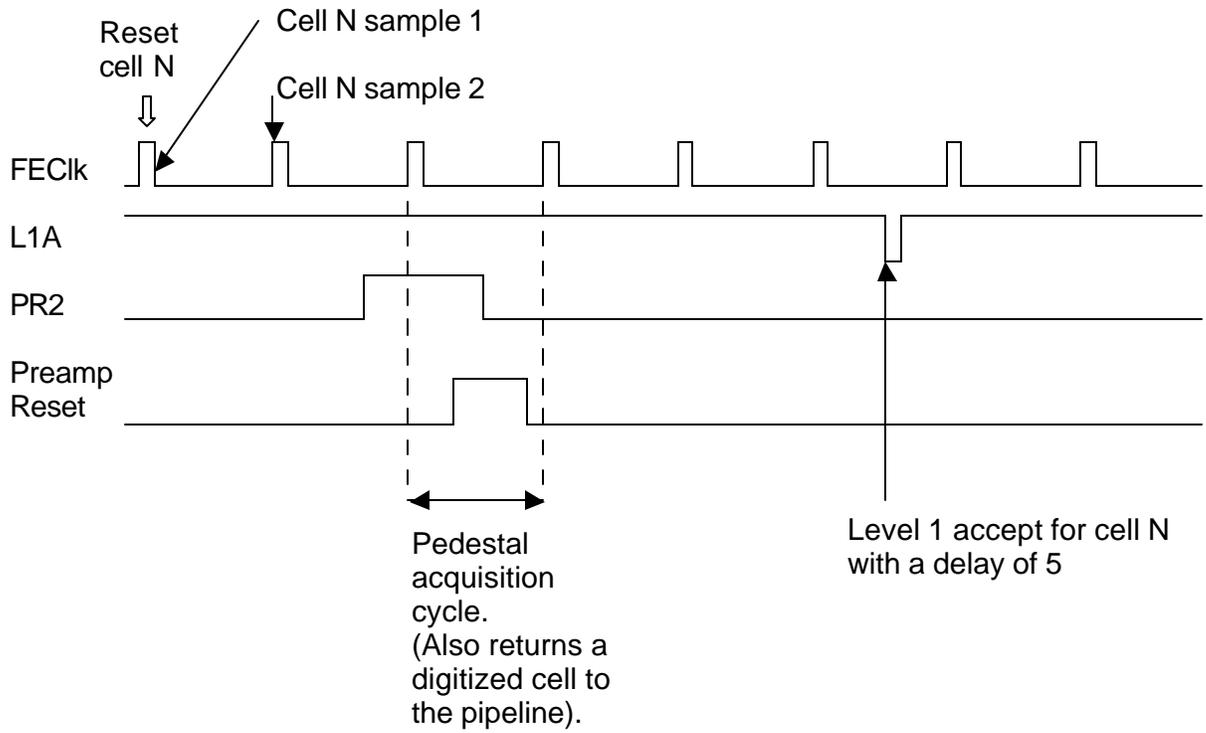
Note that during programming, the serial program bit stream should be supplied to the SVX in reverse order so that the last bit (bit 147) appears first.

Timing Diagrams

Initialize



Acquire



PreampReset shown during pedestal acquisition cycle, but this can occur any time.

Pipeline Readout

