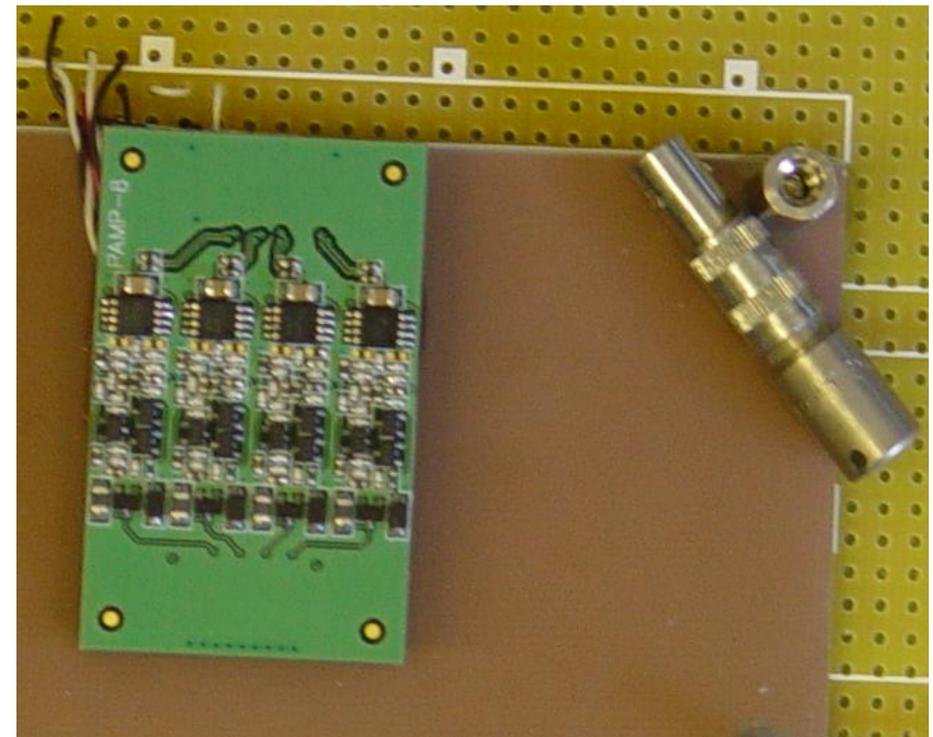
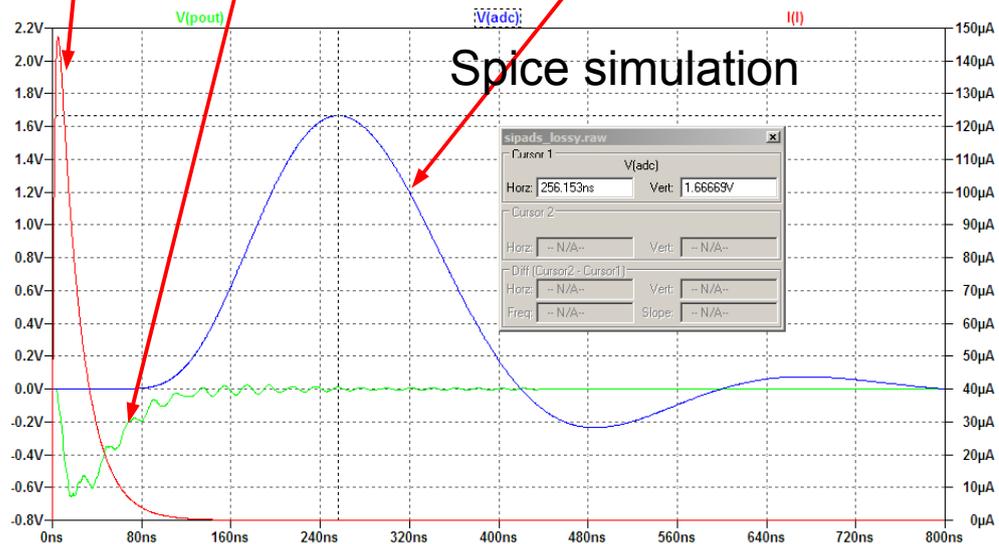
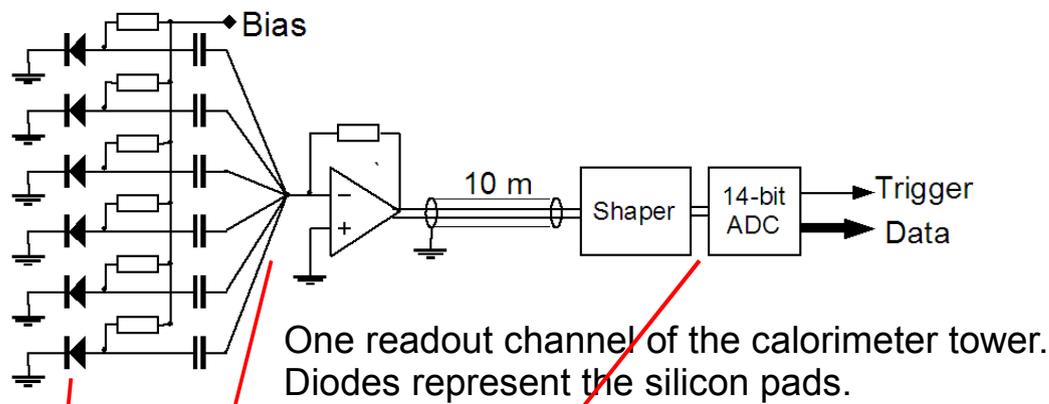


# FOCAL Electronics

Andrey Sukhanov, BNL

- Readout of Pad Sensors
- Measurement of Amplitude and Time in FPGA
- Generation of Trigger Primitives
- Readout of Strip Sensors
- Summary, Readiness for the System Prototype

# Readout of Pad Sensors

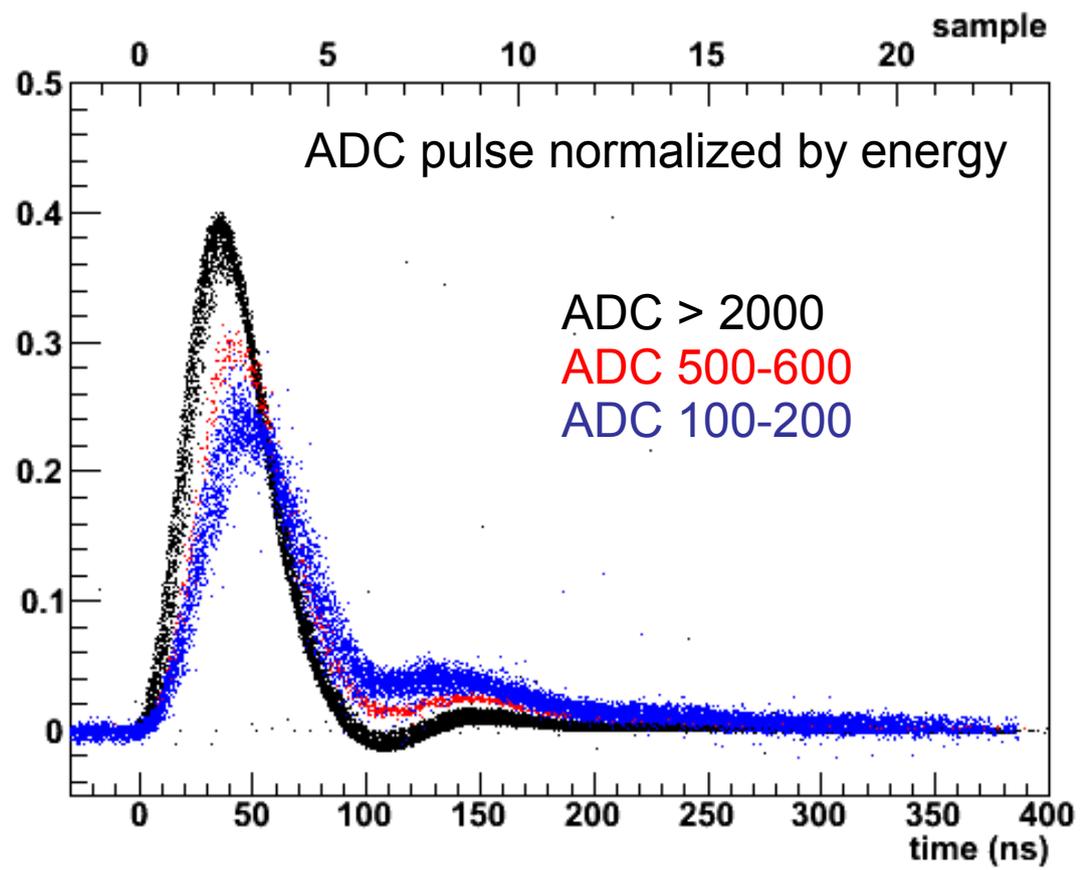


8-channel preamplifier

ADC clock 50 MHz,  
Digitization time = Shaping time + ADC latency  
= 400ns + 8\*20ns = 560 ns

# Pulse Shape Energy Dependence

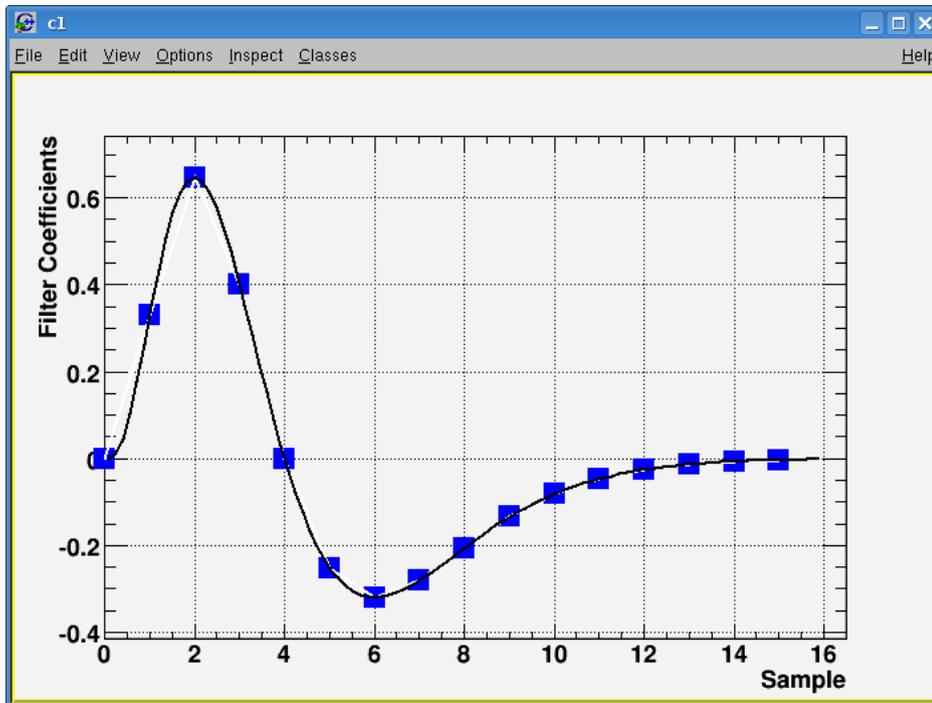
Measured during CERN test beam run in 2007



# Determination of the Pulse Parameters using FPGA for Pulses of Known Shape

Algorithm:

- 1) Apply matched filter to the signal using FIR
- 2) Determine the zero-crossing time
- 3) Correct amplitude, based on the time



Simulation of the signal superposed with the uncorrelated gaussian noise.

Amplitude to RMS noise improvement 1.5

Time resolution:

$$\sigma(t) = G \cdot \frac{RMS_{Noise}}{A} \cdot \frac{T}{\sqrt{N}}$$

G = 0.34 for unipolar shape  
= 0.2 for bipolar shape

RMS<sub>Noise</sub> – RMS of input noise

A – pulse amplitude

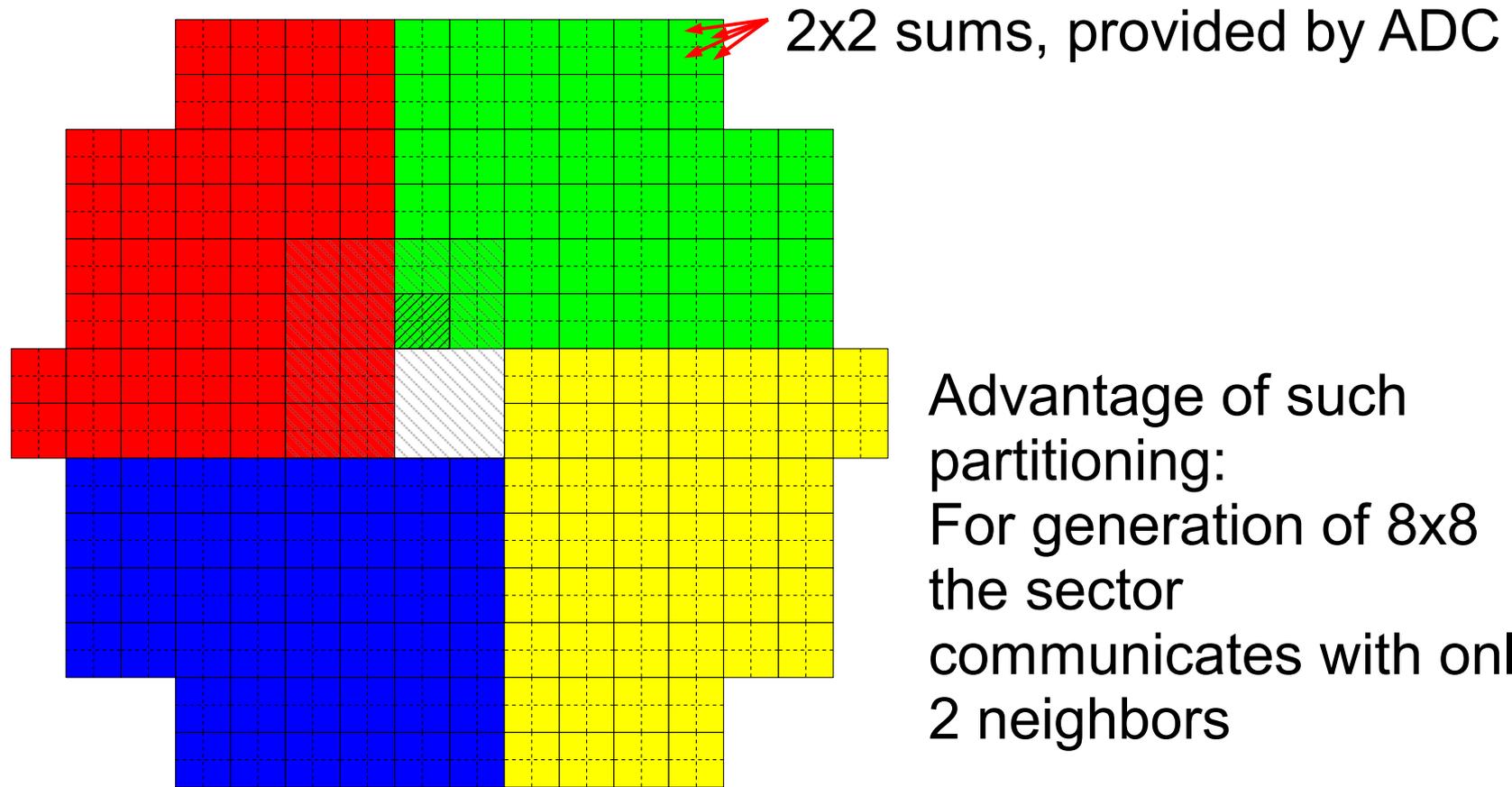
T - sampling period

N - number of samples

**The algorithm delivers the same precision as the offline fitting, using Minuit.**

For 50 MHz sampling rate, 16 samples and signal/noise of 40 we can achieve 0.5 ns timing resolution and increase amplitude resolution by the factor of 1.6 in real time.

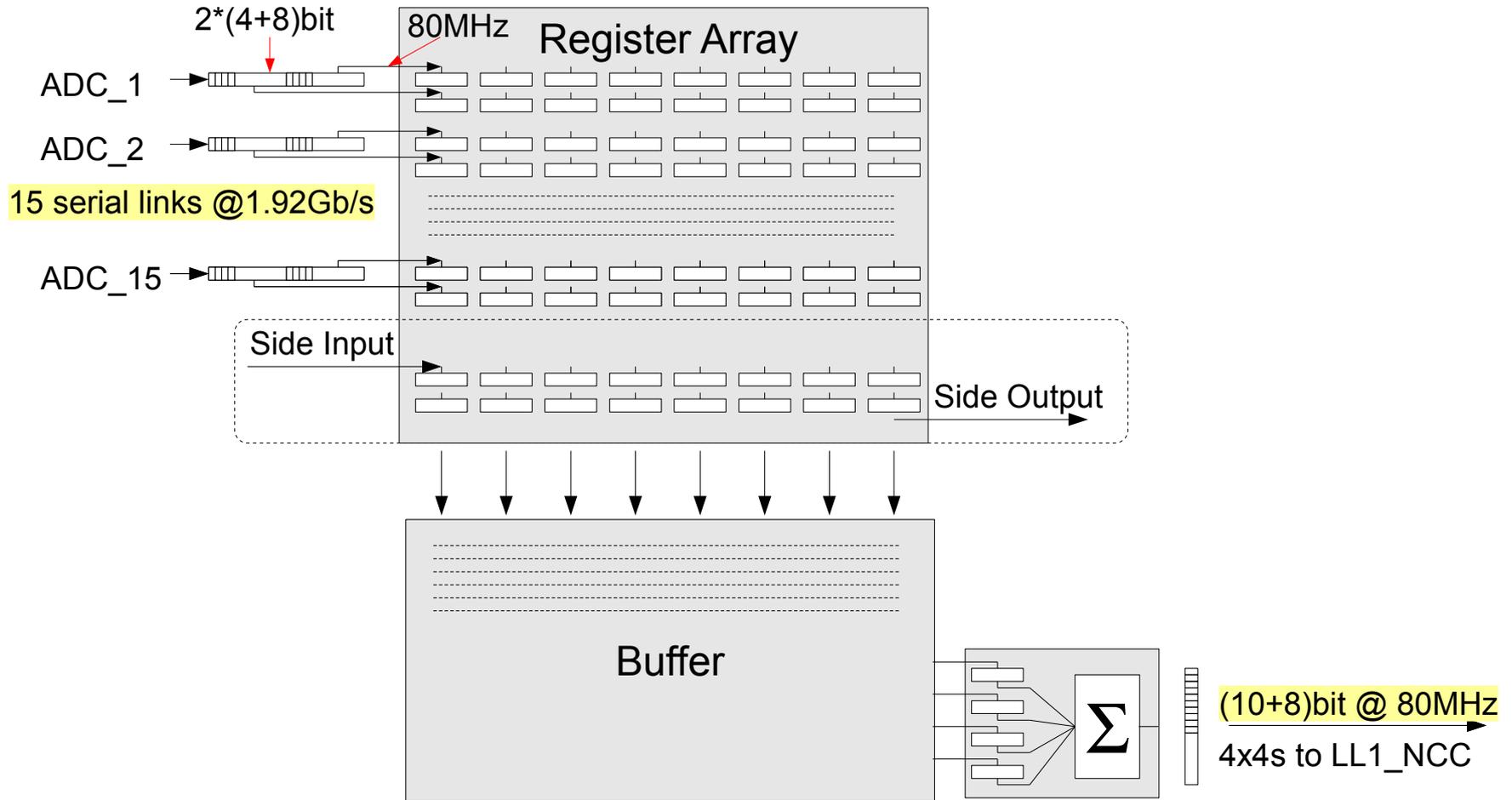
# Generation of L1 Trigger



Transversal segmentation of calorimeter for calculation of 4x4 and 8x8 sums

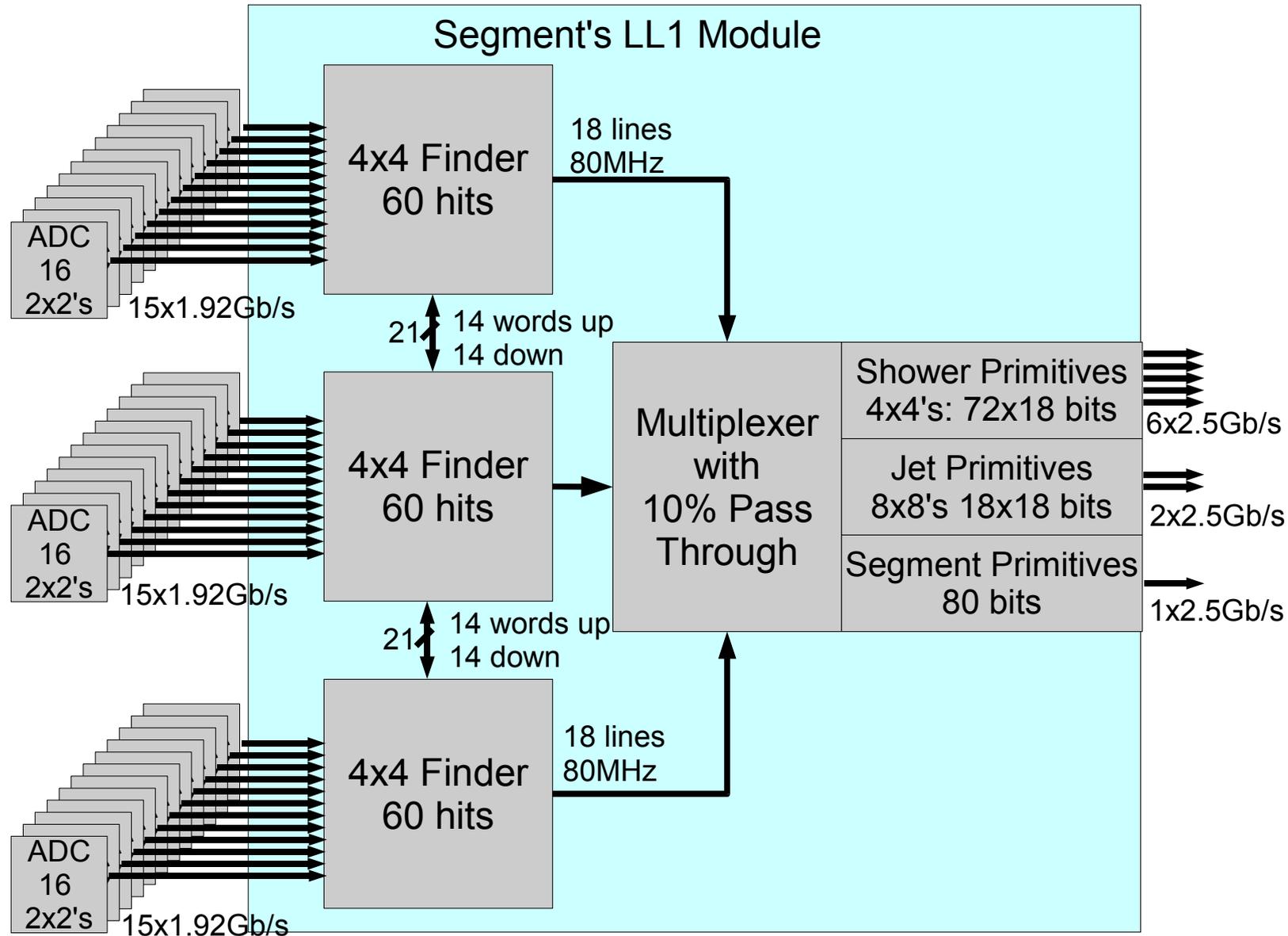
# Generation of Overlapped 4x4s Sums

ADC provides zero-suppressed data: 4bit address and 8bit data  
2x2s from ADCs

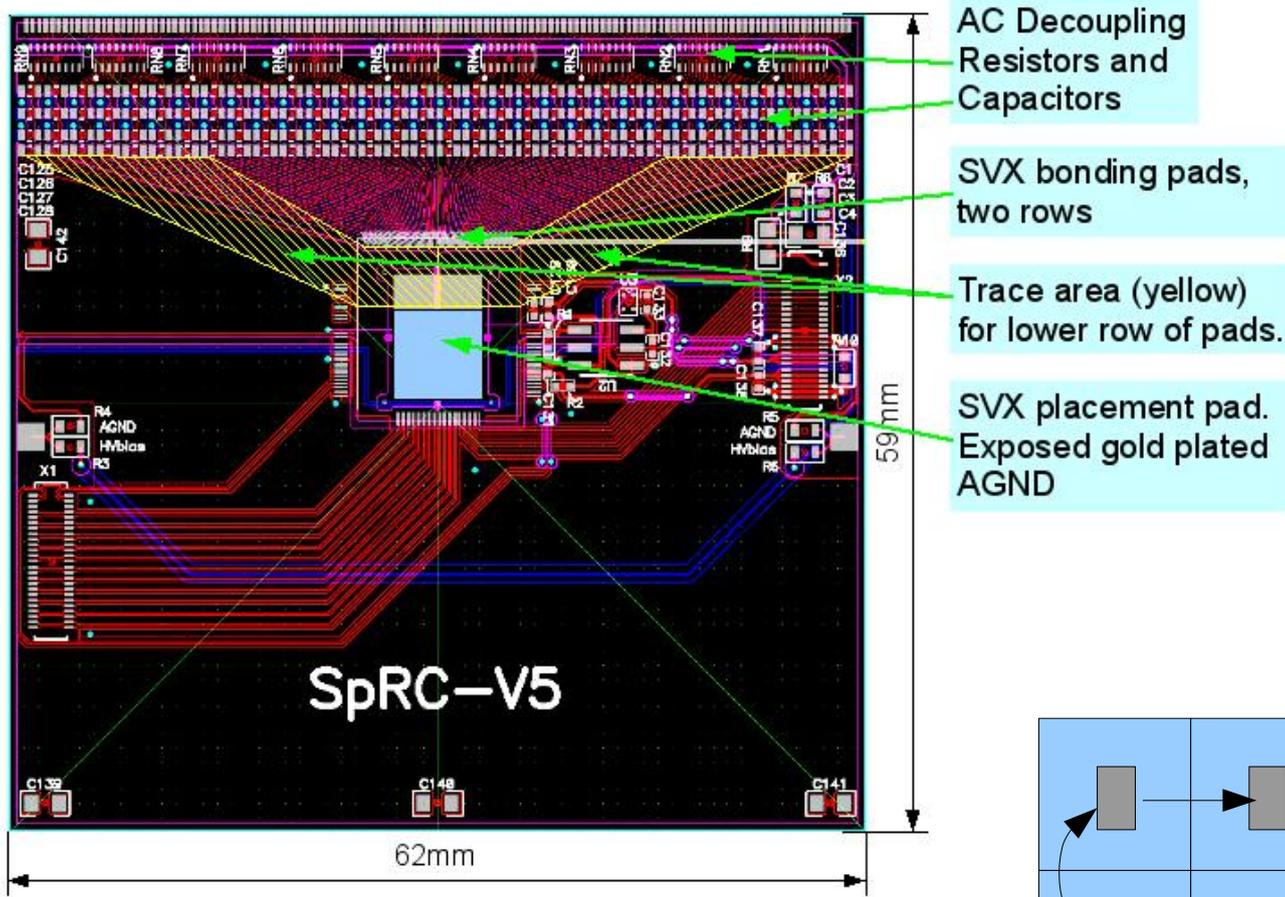


Processing time = 1+1/8 beam clocks.

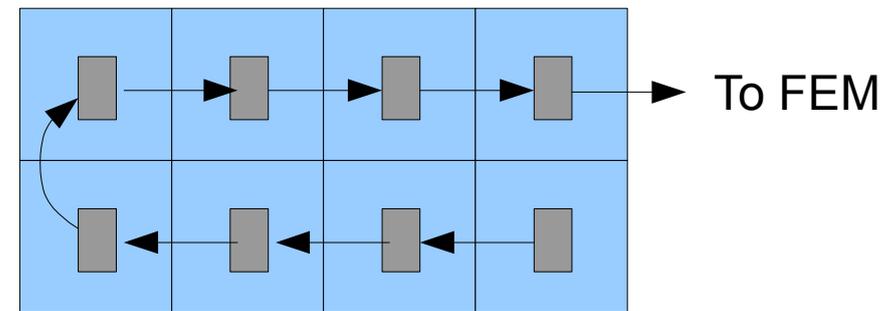
# Segment's LL1 Module, Proposal



# Readout of Strip Sensors using SVX4 chip

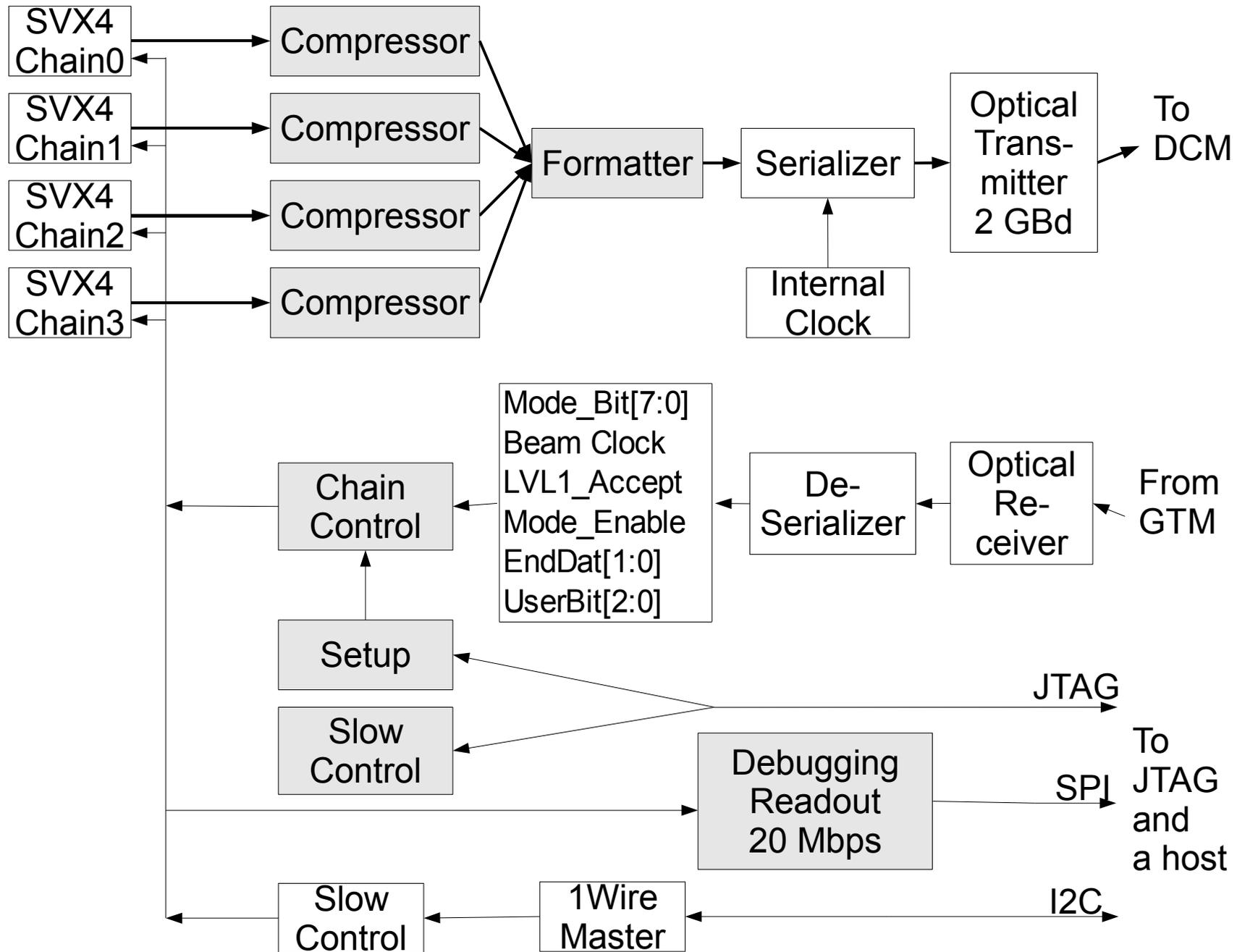


Readout card, mounted on top of the strip sensor

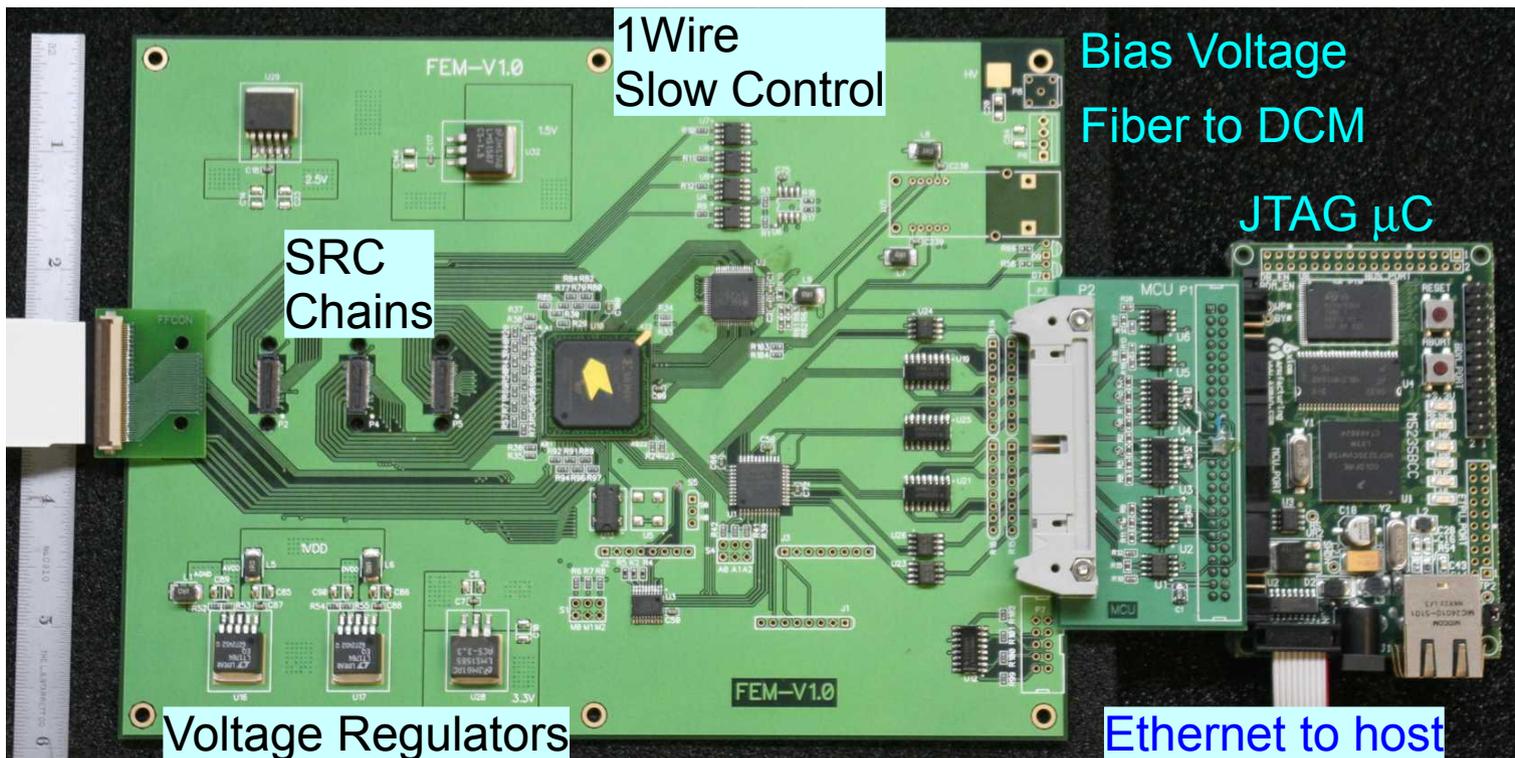


Readout chain of strip sensors.  
Any individual sensor could be bypassed.

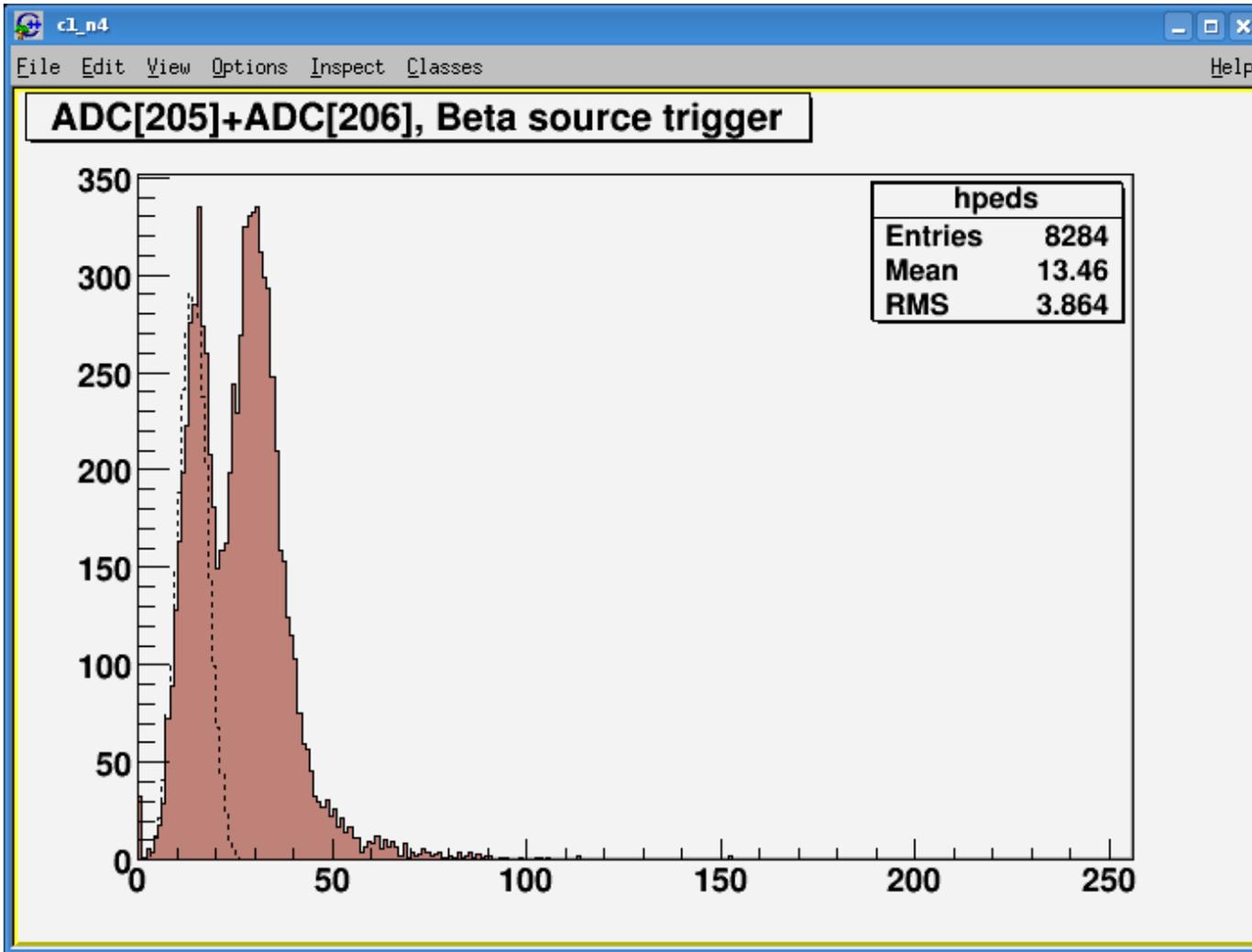
# FEM Schematic Diagram



# Strip FEM

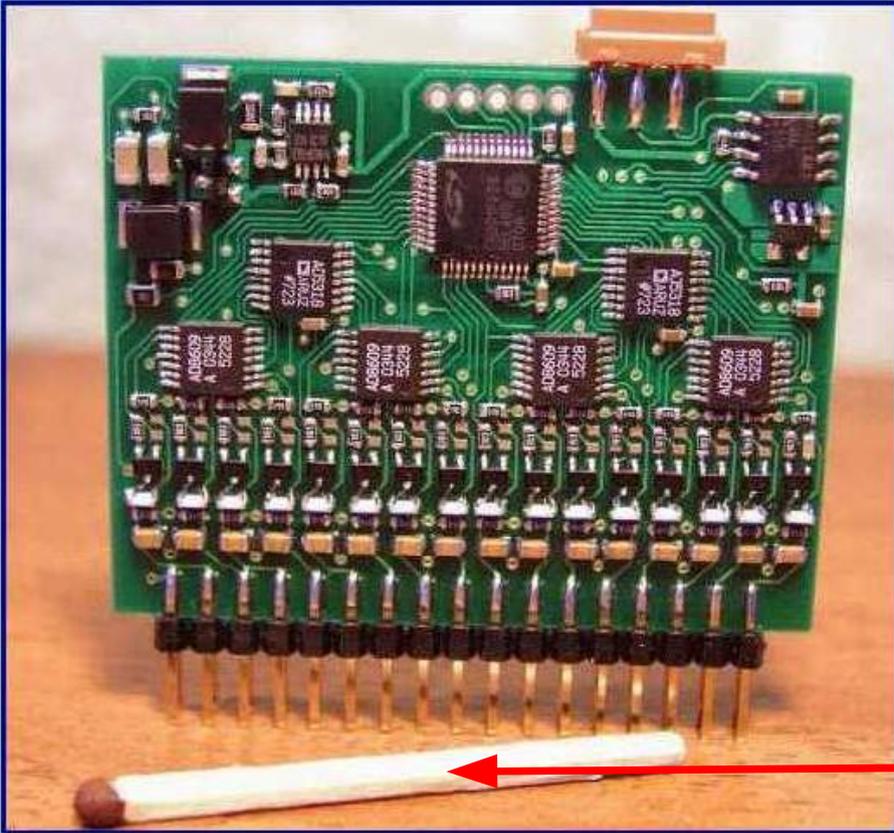


# Test with the Beta Source $\text{Sr}^{90}$



Sum of amplitudes from two adjacent strips. The dashed line – from the pedestal run. The MIP peak is clearly seen.

# Bias for Silicon Detector



Maximum output voltage -	<b>Up to 250V</b>
Output voltage regulation range -	<b><math>U_{max}/2 - U_{max}</math></b>
Precision of output voltage regulation -	<b>10 bit</b>
Stability of output voltages -	<b>0,005 %</b>
Temperature coefficient of output voltage -	<b>200 ppm/K</b>
Maximum average output current -	<b>Up to 5 mA</b>
Self-diagnosis of the BV channel -	<b>Yes</b>
Dimensions of 16- channel cell	<b>50x40x4 mm</b>
System bus - 6 line flat cable	
Maximum length of system bus -	<b>Up to 100 m</b>
Number of cells per system bus -	<b>Up to 127</b>
Number of cells per system controller	
SC508 -	<b>508 (8128 HV channels)</b>

Wooden match for comparison

8-channel Bias Module for Silicon Detectors  
Product of HVSys, Dubna, Russia

This system is already in use for RHIC polarimeters at BNL.

# Summary, Sys. Prototype Readiness

## Pads

- Preamplifier hybrids: manufactured and tested.
- Pad Micromodules: being assembled at Dubna.
- Motherboards and crate: ready
- ADC system: for prototype – use HBD ADCs, for production – new system is needed.
- L1 module: conceptual design

## Strips

- Strip Readout Card: new design ready for manufacturing.
- Strip Micromodules: will be assembled at BNL and wire bonded at FNAL or Helsinki.
- FEM: manufactured and tested
  - Slow Control and Data Taking: ready.
  - Bias voltage system: ordered.