

NCC Stripixels

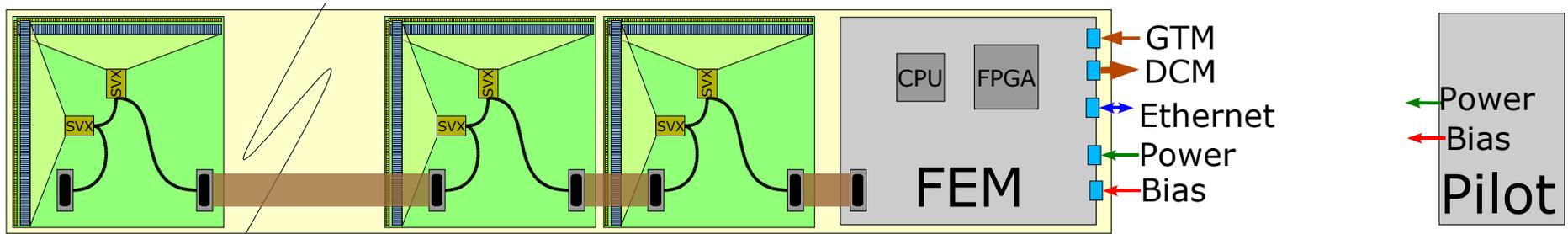
Strip length [mm]	64
Strip pitch [mm]	0.5
Strip thickness [mm]	0.6
Strip capacitance [pf]	< 10
Strip orientation	XY
Bias voltage [V]	< +200
Sensor height [mm]	64
Sensor width [mm]	64
Strips per sensor	256
Number of sensors	~ 366
Number of SVX4 chips	732
Total number of channels	93696
Occupancy	~ 1%

Readout Chain

Space limitation: The thickness of the assembled board should be less than 5 mm

Variant when strips are routed on two edges of a sensor

(single metal technology): The cable jumpers are needed.



Six or seven sensors with the readout hybrids are glued to a carrier board.

All SVX4 chips are daisy chained and connected to a FEM module.

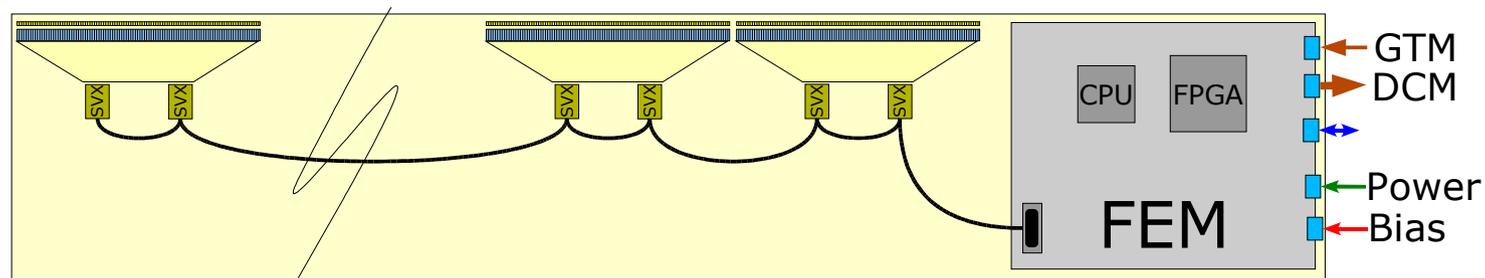
The FEM is 64mm*100mm*10mm board located on the carrier board.

The low voltage power and the bias voltage for sensor supplied by a pilot board mounted on the magnet.

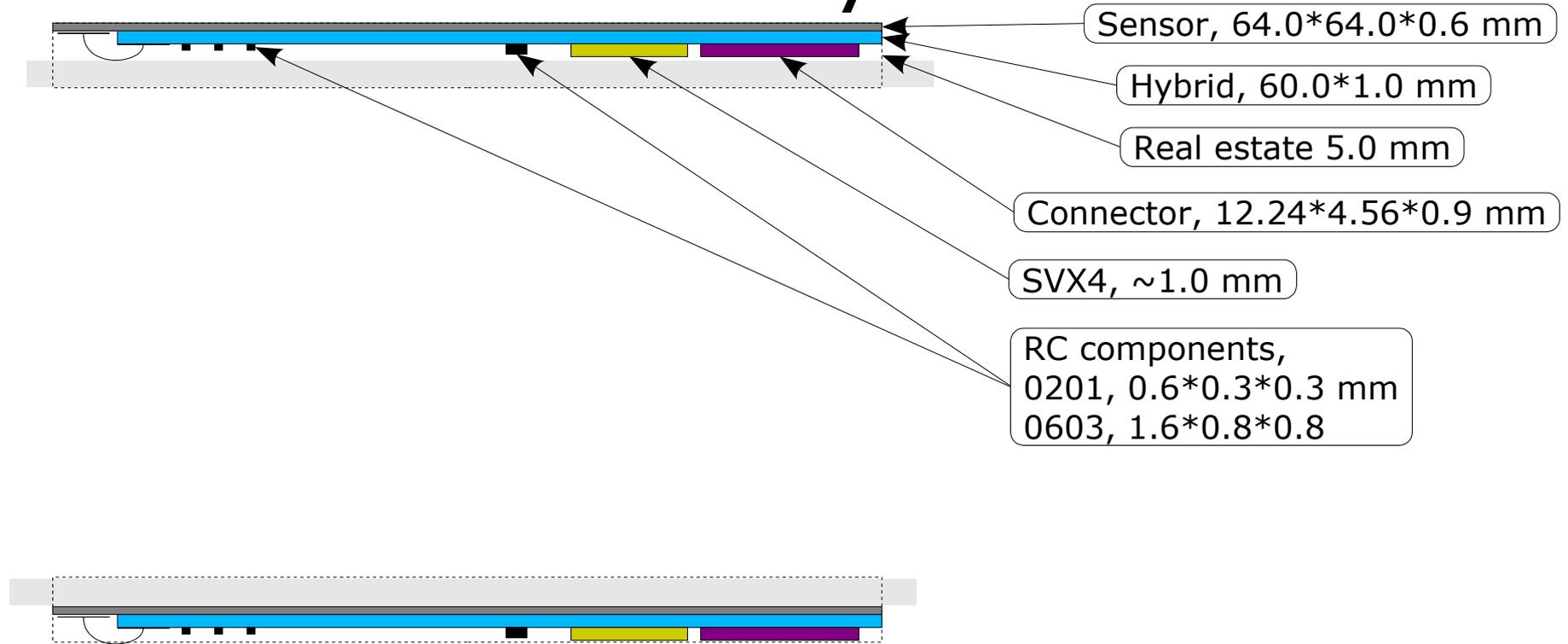
Only one bias voltage supply per ladder can be routed due to a limited number of wires.

Variant when strips are routed on one edge of a sensor

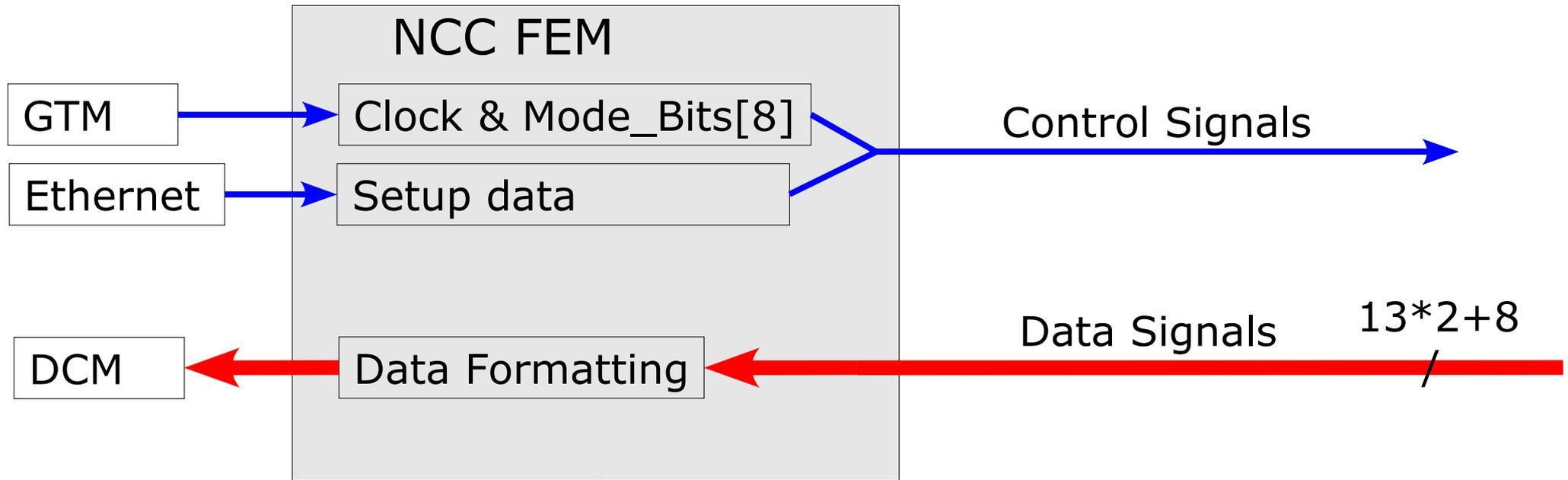
(double metal technology): Signals routed on the carrier board



Sensor+Hybrid



Readout Diagram



Under development

CPU: MFC5271, Ethernet, JTAG

OS: OpenTCP

Data traffic: XILINX Spartan3

Readout Conditions

These are the conditions that must be satisfied:

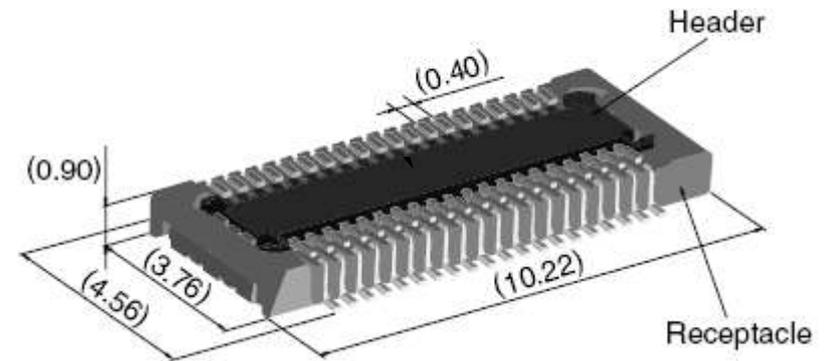
- 1) The system must be capable of handling multiple Level-1 triggers occurring while waiting for the first event to be digitized and sent into the FEM. The current requirement is to buffer 5 events, but the SVX4 is only capable of storing 4, so the one event should be buffered inside the FEM.
- 2) The digitization must be complete in 40 usec.
- 3) The data must be transferred to the FEM in another 40 usec.
- 4) The system must be capable of digitizing one event at the same time that it is transferring the first event so that as soon as one event is transferred we can start transferring the next event.

Readout Time

Back-end clock [Mhz]	53
Digitization time [us]	2.42
Readout time (no pedestal suppression)	
Number of hits	128
Number of clocks	129
Readout time of the single SVX4 [us]	2.43
Number of SVX4 in the chain	14
Data size [kB]	3.53
Readout time of the chain [us]	34.08

Digital Signal Bus

	Pad	A/D	I/O	Notes
1	BUSB<7>	Diff	I/O	
2	BUSB<7>	Diff	I/O	
3	BUSB<6>	Diff	I/O	
4	BUSB<6>	Diff	I/O	
5	BUSB<5>	Diff	I/O	
6	BUSB<5>	Diff	I/O	
7	BUSB<4>	Diff	I/O	
8	BUSB<4>	Diff	I/O	
9	BUSB<3>	Diff	I/O	
10	BUSB<3>	Diff	I/O	
11	BUSB<2>	Diff	I/O	
12	BUSB<2>	Diff	I/O	
13	BUSB<1>	Diff	I/O	
14	BUSB<1>	Diff	I/O	
15	BUSB<0>	Diff	I/O	
16	BUSB<0>	Diff	I/O	
17	OBDVB	Diff	I/O	
18	OBDV	Diff	I/O	
19	BECLKB	Diff	I	
20	BECLK	Diff	I	
21	FECLKB	Diff	I	
22	FECLK	Diff	I	
23	CHMODE	D	I	
24	BEMODE	D	I	
25	FEMODE	D	I	
26	CALSR	D	I	
27	L1A	D	I	
28	PIPERD2	D	I	
29	PIPERD1	D	I	
30	PARST	D	I	
31	PRIOUT	Diff	O	
32	PRIOUTB	Diff	O	
33	PRIIN	Diff	I	PRIINB is not routed. Corresponding pin on first SVX4 is pulled to an intermediate level



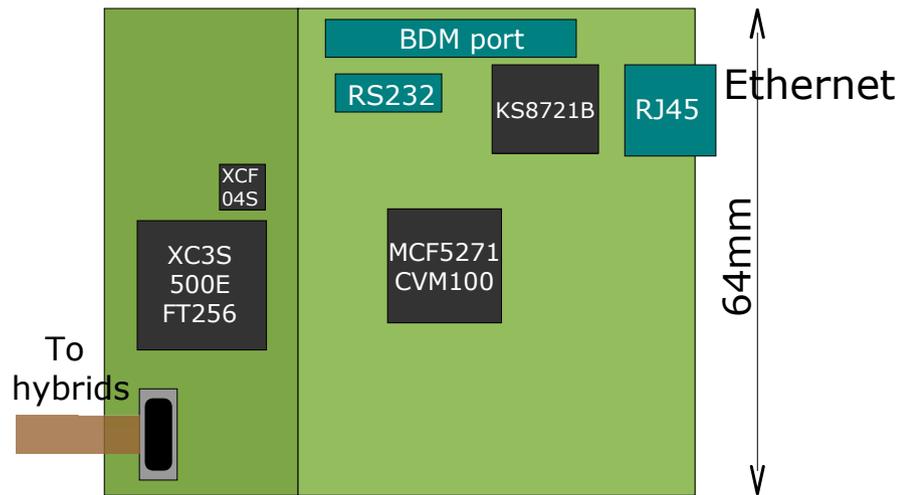
Connector Hirose DF30
40 positions shown

Analog Signal Bus

		D/A	I/O	V	
1	AVDD	A	I	2.5	Analog PS
2	Gnd!	A	I		Analog ground
3	Vddd!	A	I	2.5	Digital PS
4	Gnnd!	A	I		Digital ground
5	HV	A	O		HV bias
6	T1	A	O		Temperature sensor 1
7	T2	A	O		Temperature sensor 2
8	HVDiag	A	O		HV sensor
9	VCAL	A	I		
10	VTH	A	I		
11	Bias	A	I		Bypass capacitor
12	VRSet	A	I		Diagnostics
13	AREF	A	I		
14	IQUI	A	I		
15	D0Mode	D	I		
16	USESEU	D	I		
17	ISLOPE	A	I		
18	BNBR	D	I		
19	TNBR	D	I		

NCC-FEM (Front-End Module)

Draft



NCC-FEM board

Not shown:

- Power supplies and voltage regulators for AVDD & DVDD
- HV port
- Data port to DCM
- Synchronization from GTM

Hardware:

MCF5271 – ColdFire 100 Mhz CPU
64 KB SRAM, 8KB Cache, Ethernet, RS232, I2C, GPIO, JTAG. Cost: \$10.

XC3S & XCF – XILINIX Spartan3 FPGA, three models will fit: 250E, 500E or 1200E. Cost \$22 + \$8

KS8721B, RJ45 - Ethernet for slow control, FPGA programming, downloading,

RS232 and BDM – for debugging

Software: OpenTCP