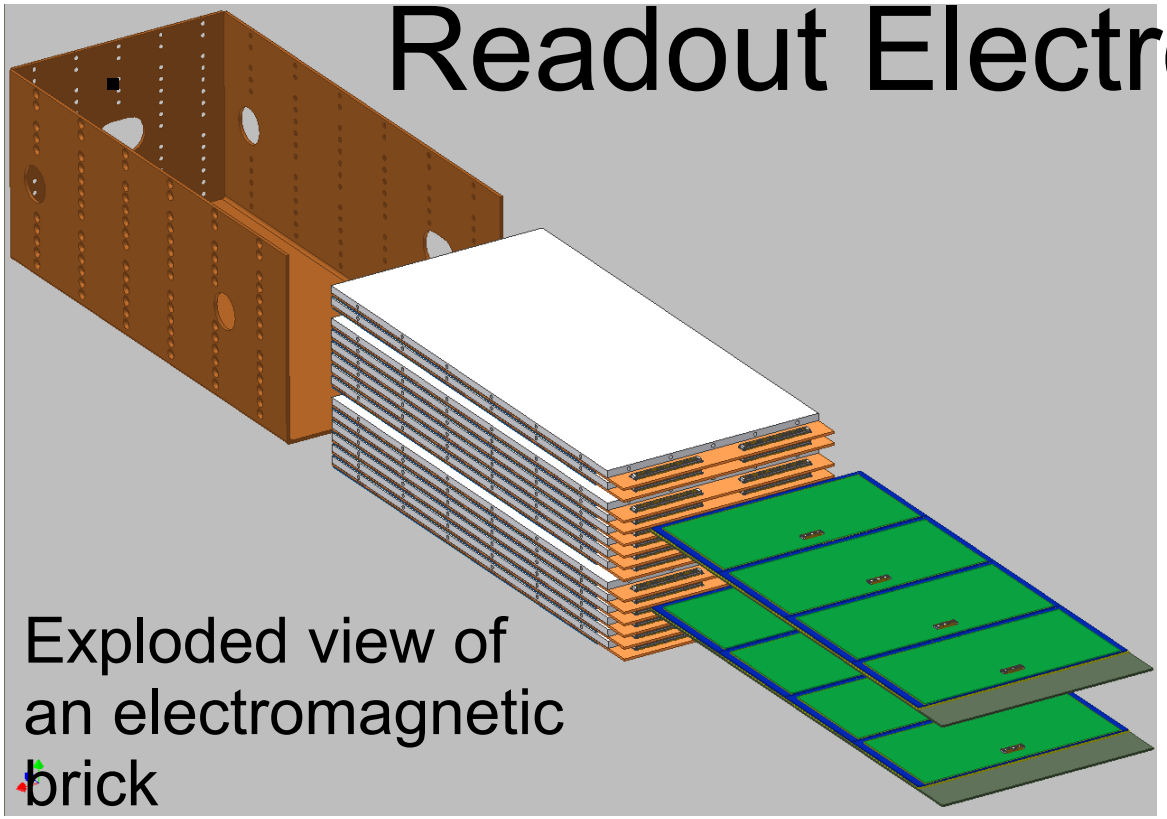
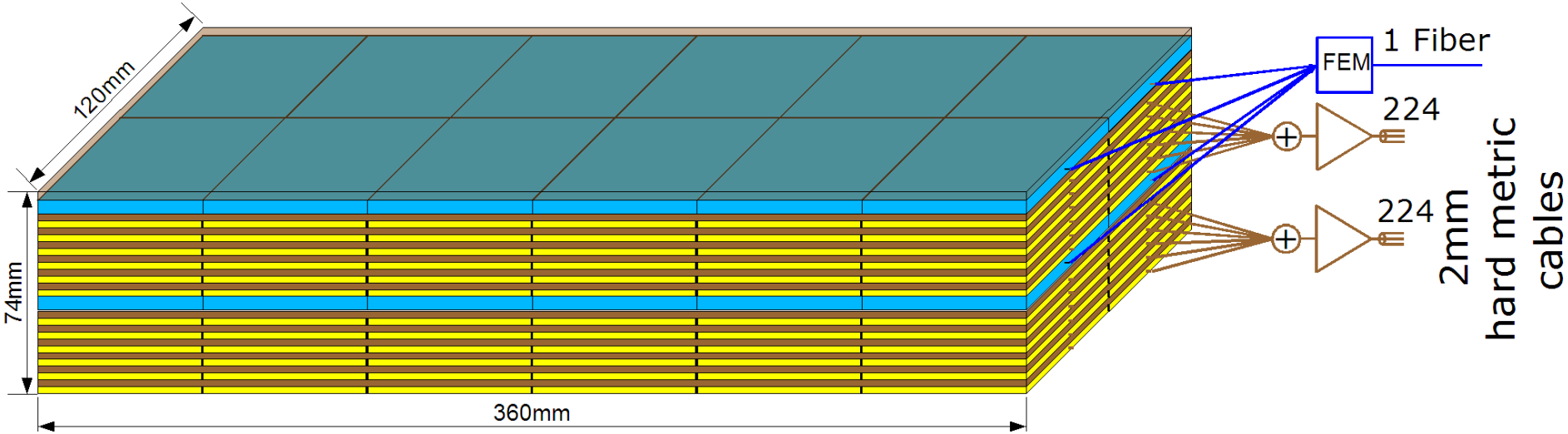
Readout Electronics for NCC





Part 1. Readout of Pixelated Sensors

Main contributors

- BNL Physics:
  Edward Kistenev, Andrey Sukhanov, Steve Boose, Ed Baker
- BNL ID:
  Zheng Li, John Triolo, Don Pinelli
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- Moscow, MSU:
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- Helsinki, Inst. Of Physics:
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- Yonsei University:
  Suhyeon Kim
- Stony Brook undergrad.:
  Ilya Sukhanov

Stripixel Sensor + SRC = SRM

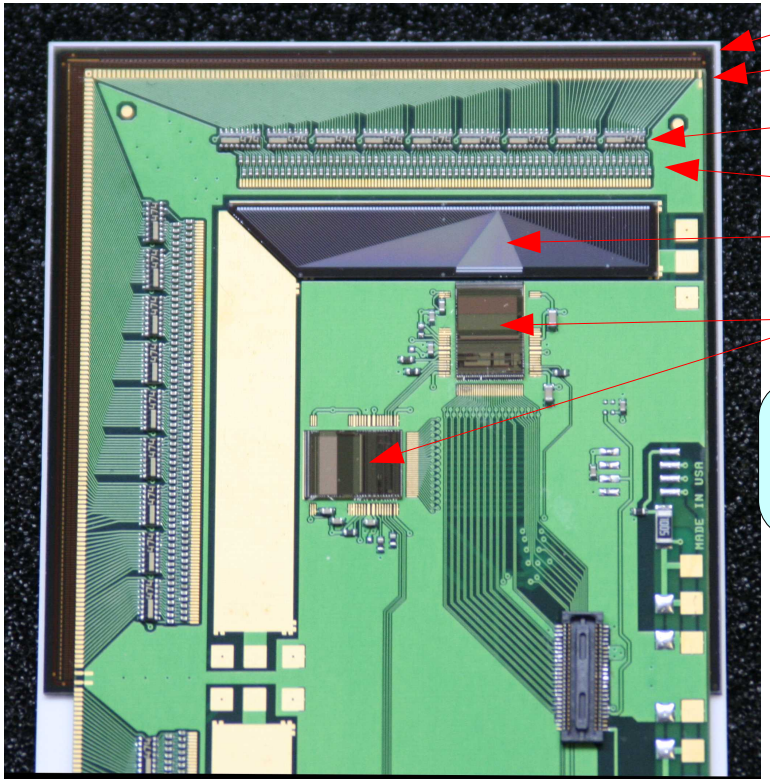
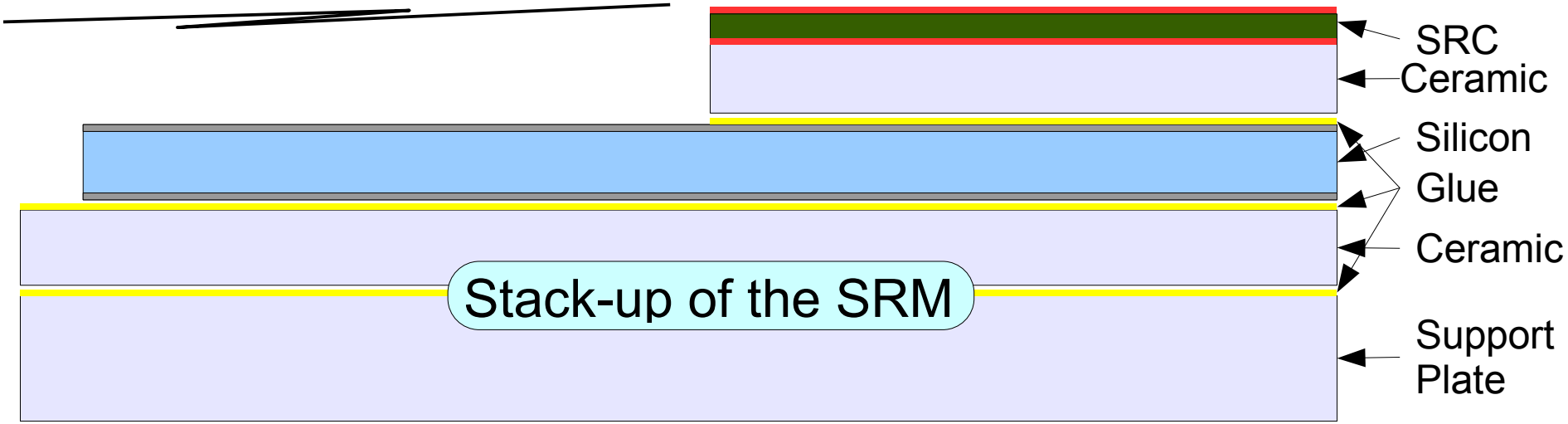
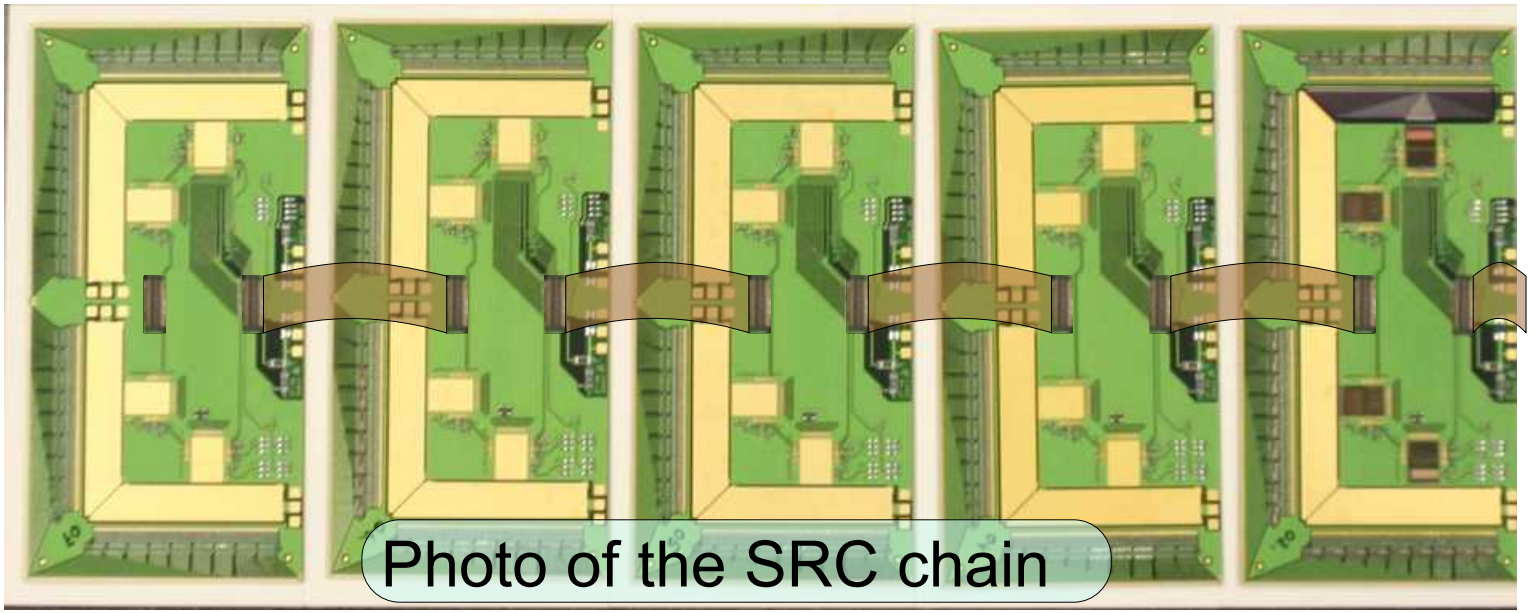


Photo of the SRC positioned on sensor



Stack-up of the SRM

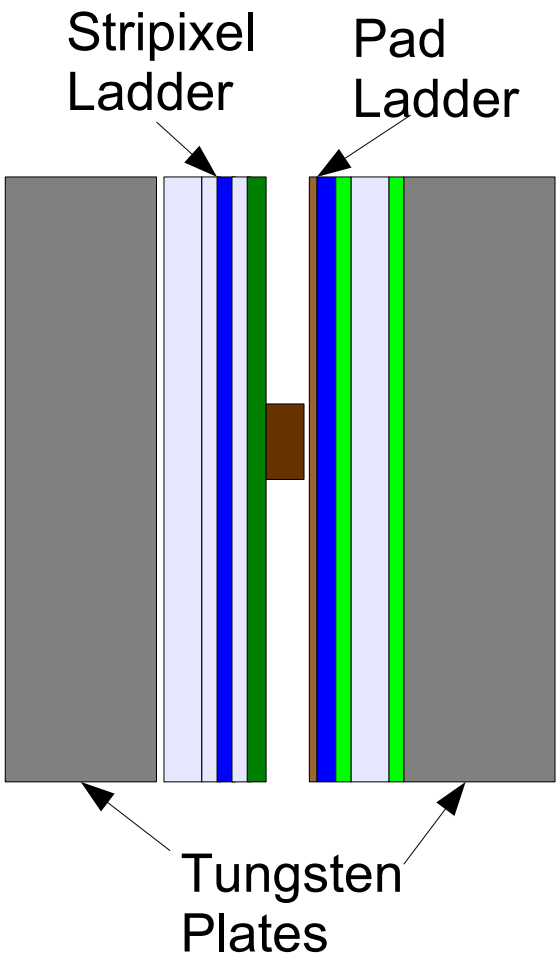
Stripixel Readout Chain



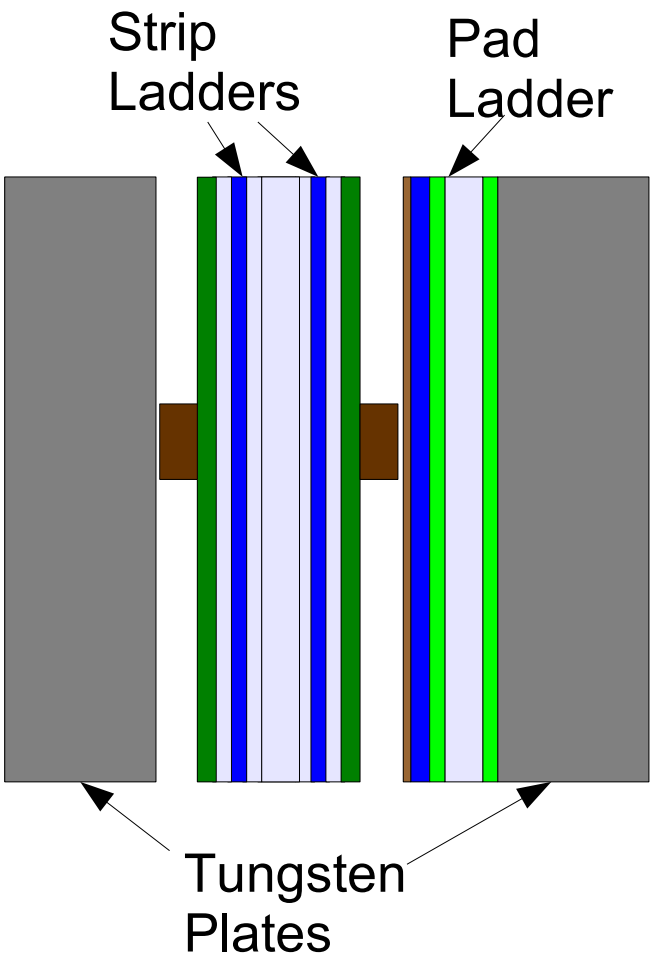
First version of Sensor Readout Card (SRC) is working.
Modifications required for final version:

- Two connectors
- More test points

Arrangement of Readout Ladders

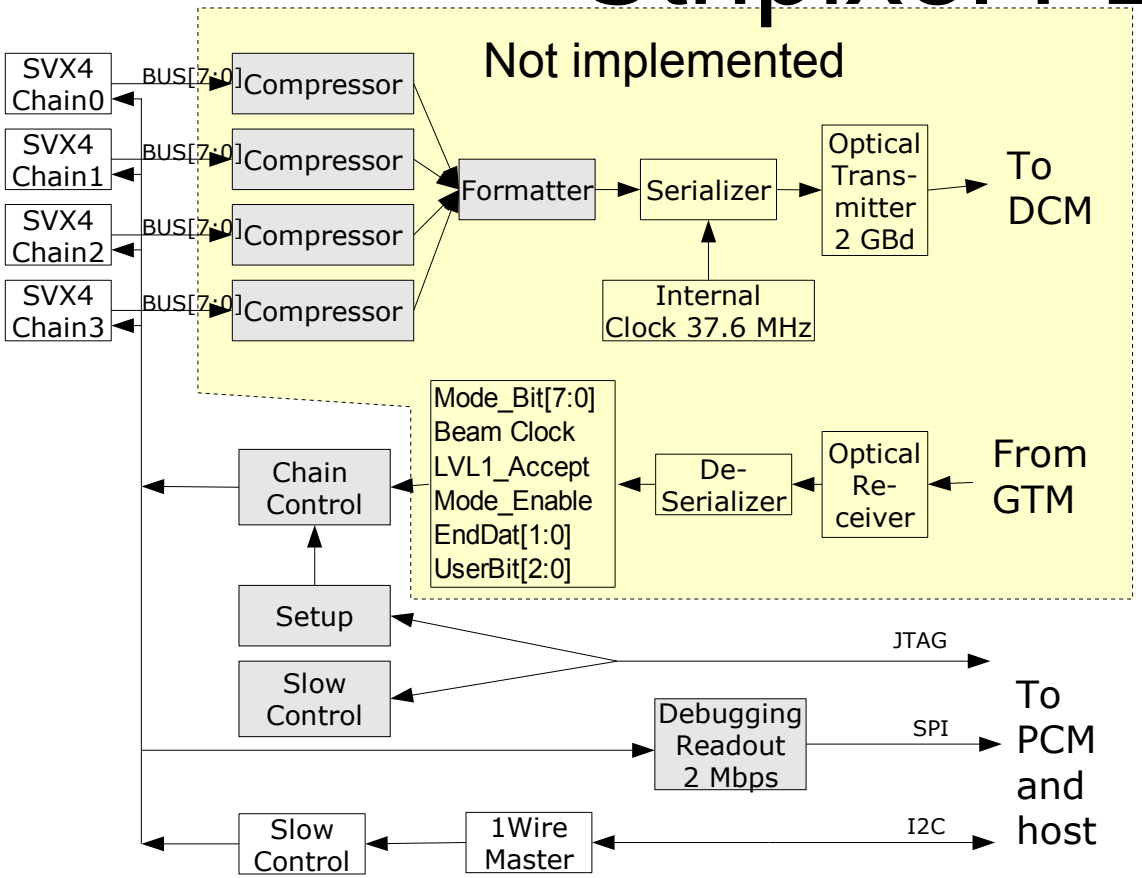


Best case scenario:
With stripixel sensors.



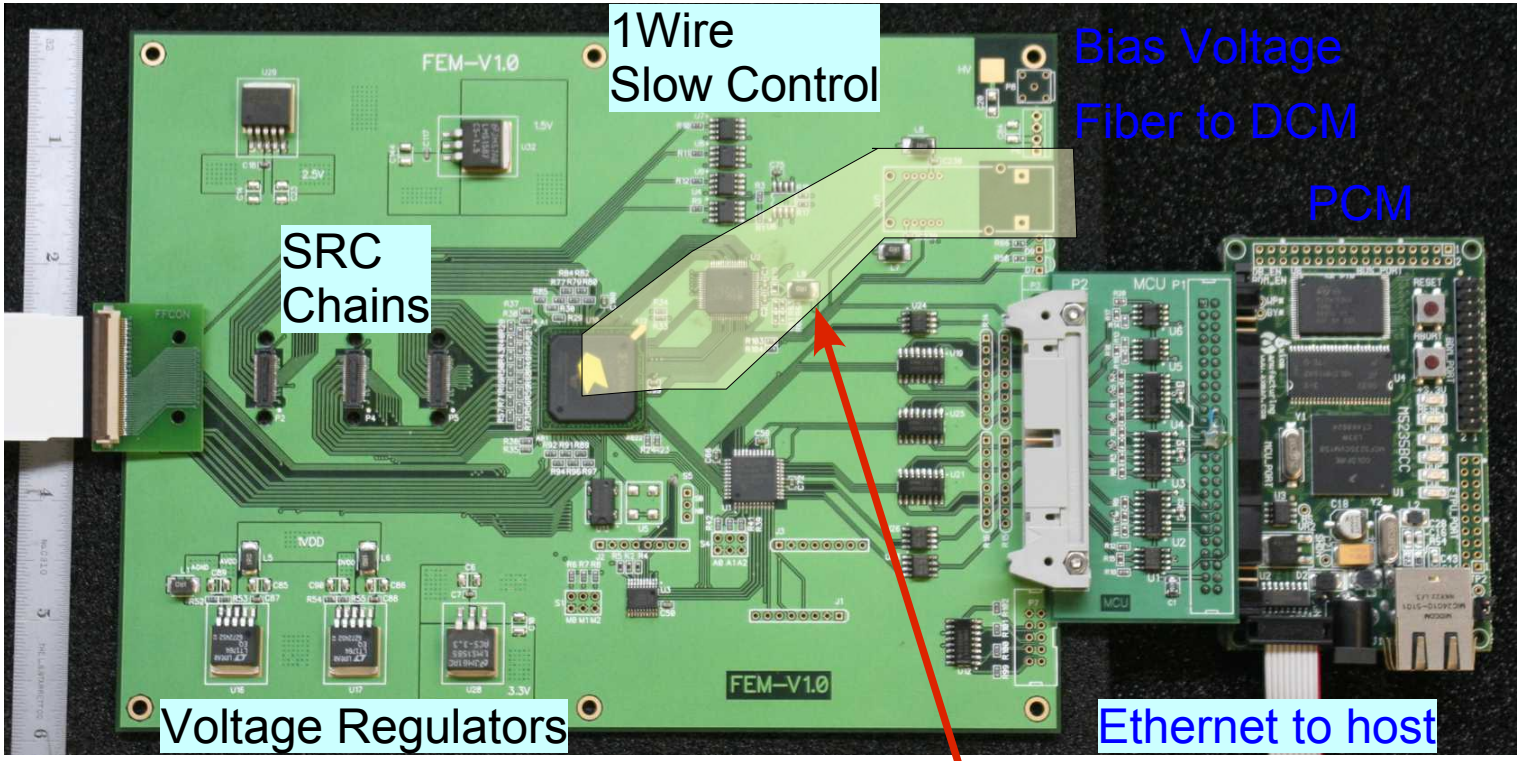
Backup solution:
If stripixel production failed then we will use single-sided strip sensors

Stripixel FEM



The block diagram of the FEM, the grey blocks – parts of the FPGA.
Remote FPGA configuration: test setup - from Power and Control Module (PCM), beam setup - from GTM link.

Stripixel FEM & PCM



All FEM functionality, except a fiber link to PHENIX DAQ, have been tested. No modifications required.
FPGA utilization: 10%.

- Throughput of the ethernet serializer to host: 2MByte/s.
- JTAG configuration over ethernet: STAPL/JAM, XSVF file formats
- Online configuration and monitoring using JTAG.

Data Size and Transfer Time

Size and Transfer Time of Stripixel Data from Single Electromagnetic Brick		
Raw event size, no pedestal suppression	14448	Bytes
Raw event size with channel ID removed	**7224**	**Bytes**
FEM readout clock, both edges used	40	Mhz
Collection time from 4 SVX4 chains on FEM	22.58	us
Data transfer rate to DCM	2.0	Gbps
Transfer time of raw event	**36.1**	**us**
Hit occupancy	5%	
Output data size, pedestal suppressed	722	Bytes
Transfer time of zero-suppressed event	**3.6**	**us**
Lossless Compression		
Compression factor for raw data	2.5	
Size of compressed event	2890	Bytes
Data transfer time of compressed event	**14.4**	**us**
Lossy compression		
Compression factor for zero suppressed data	3.0	
Event size, zero-suppressed & compressed	241	Bytes
Transfer time, zero-suppressed & compressed	**1.2**	**us**

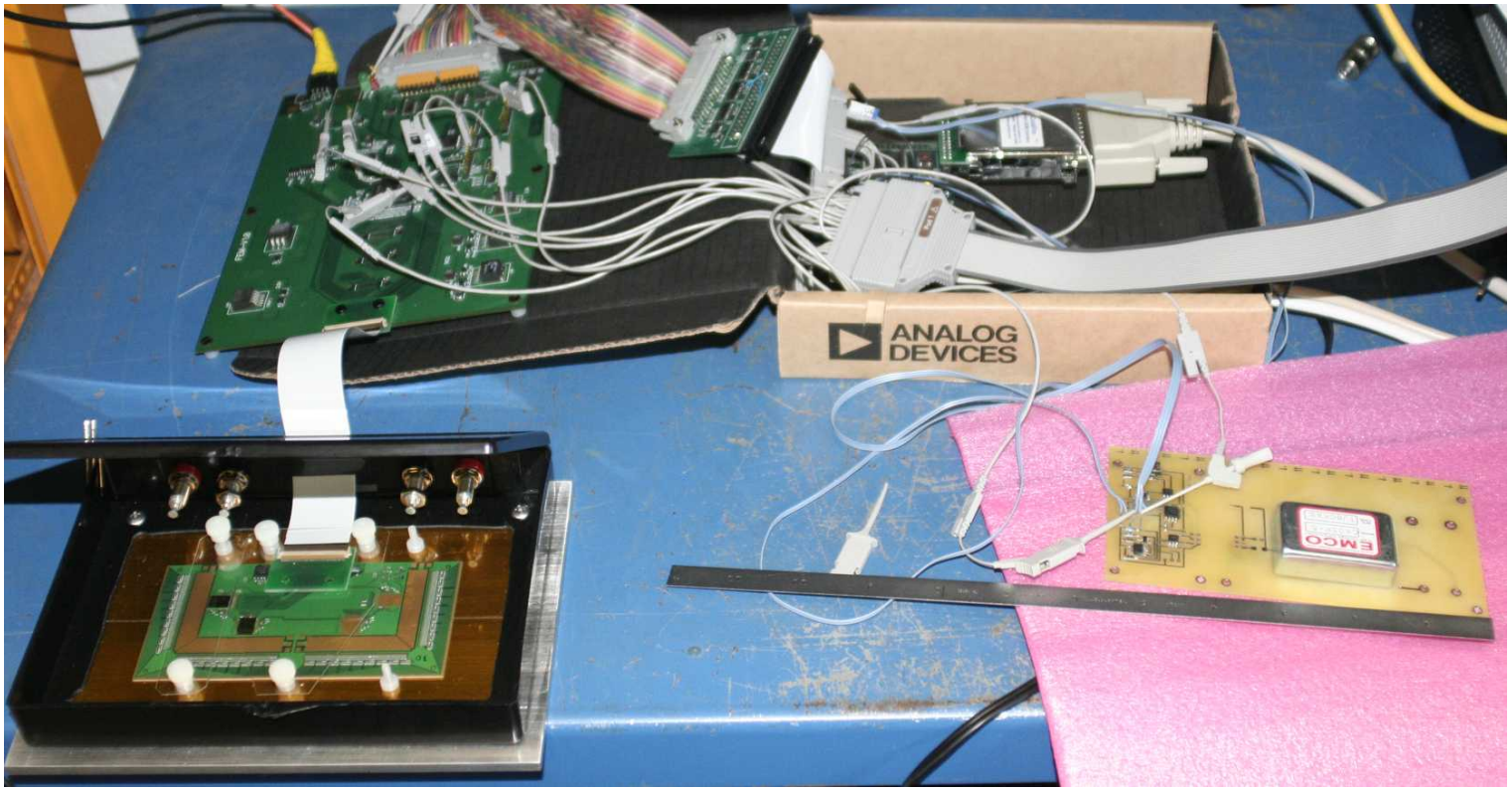
Data compression algorithm developed. Combination of
- Single Side Growth Huffman Tree
- Run Length Encoding

If dynamic pedestal suppression of SVX4 can handle the common mode noise

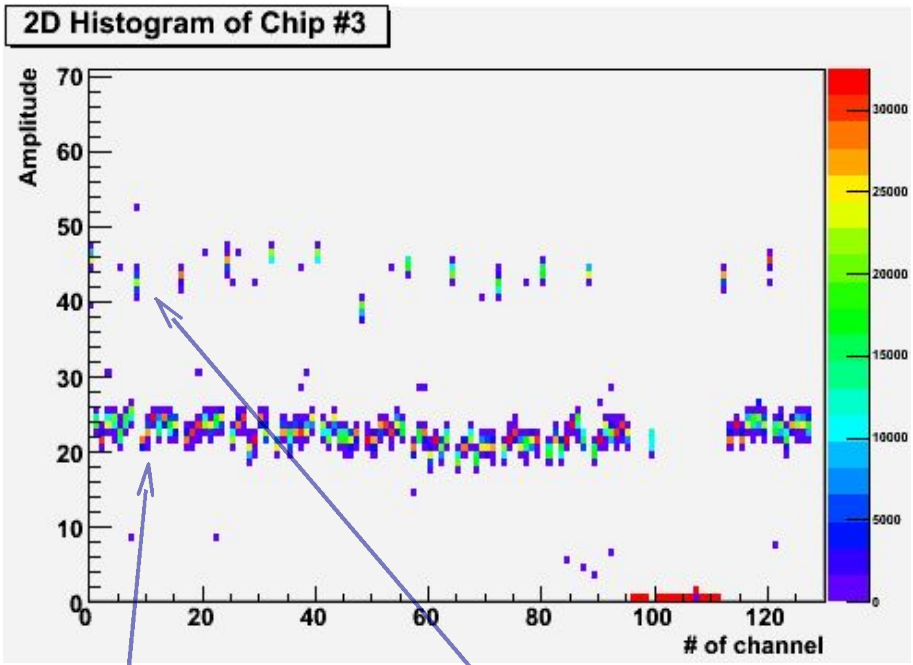
If we have to use compression

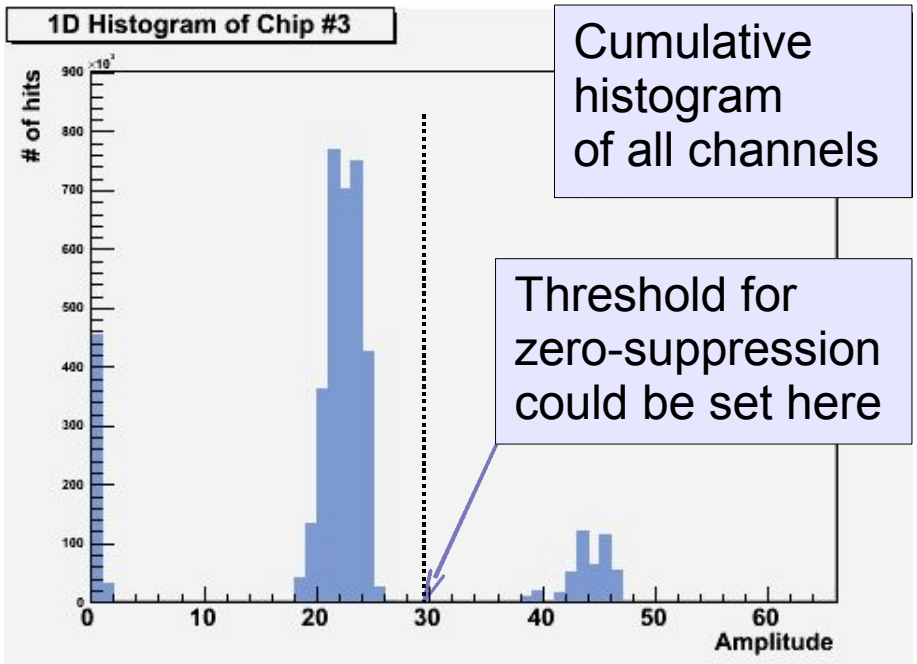
Best case scenario

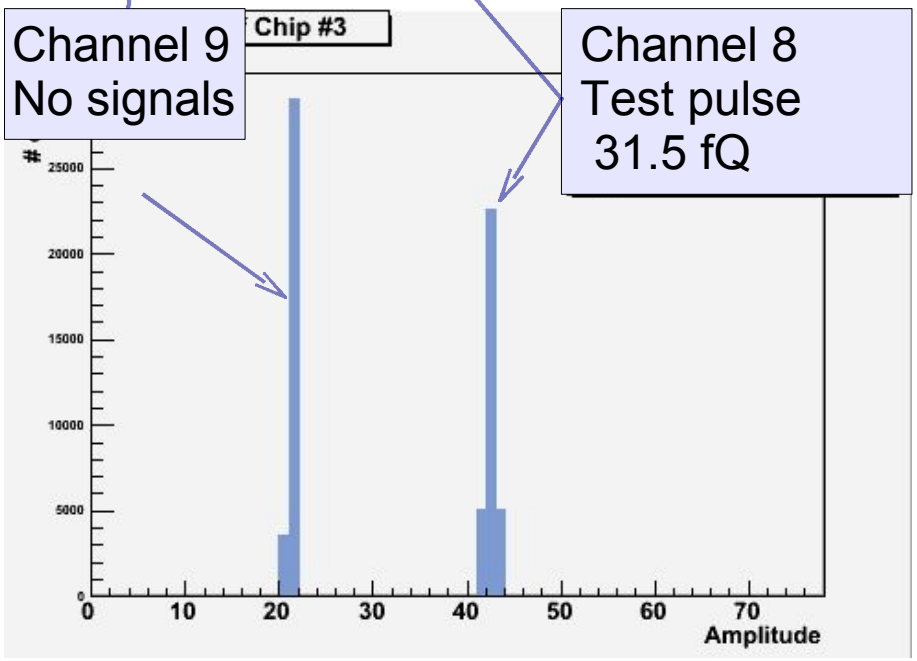
Test Setup



Test Pulse Spectra

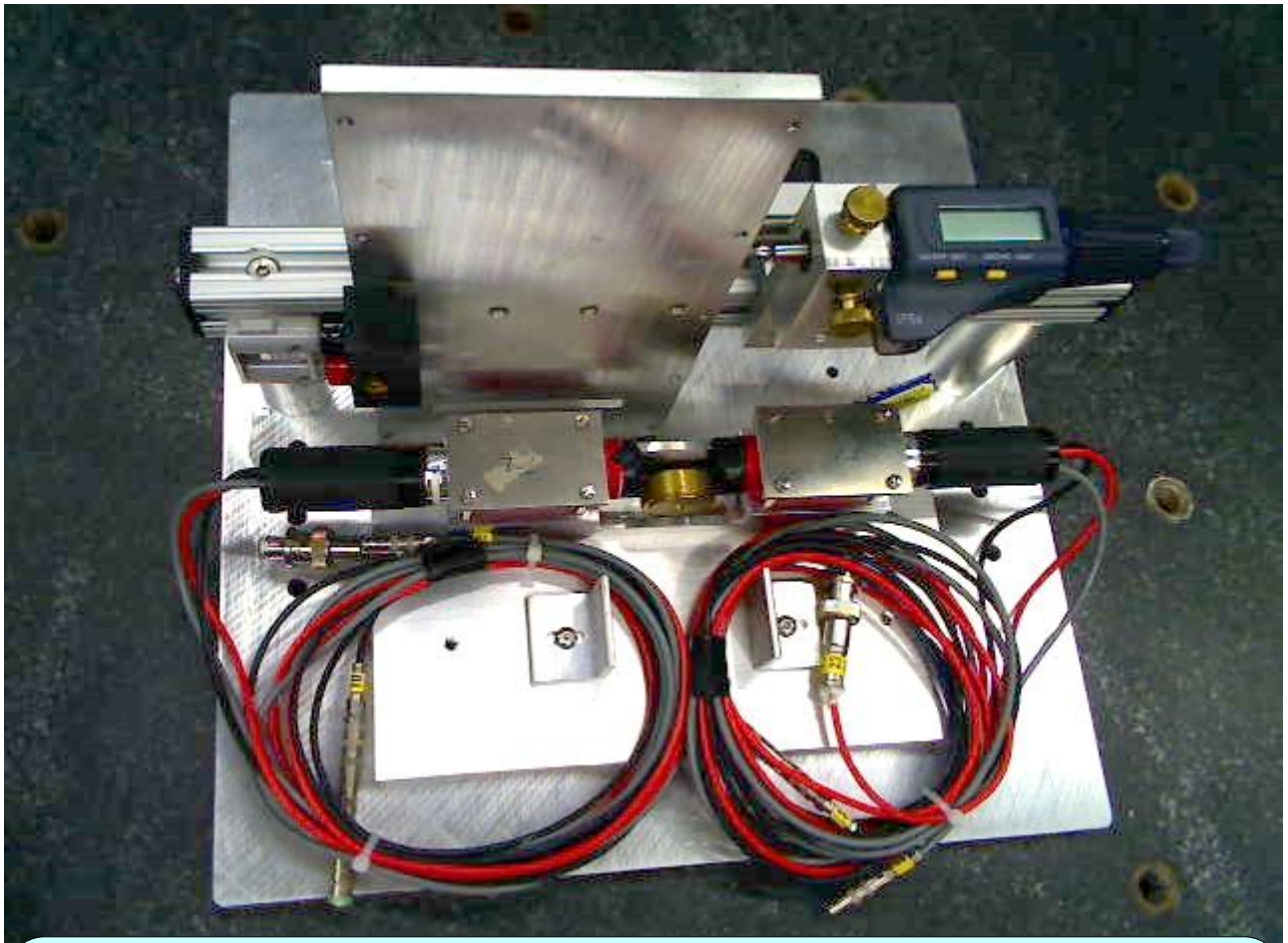






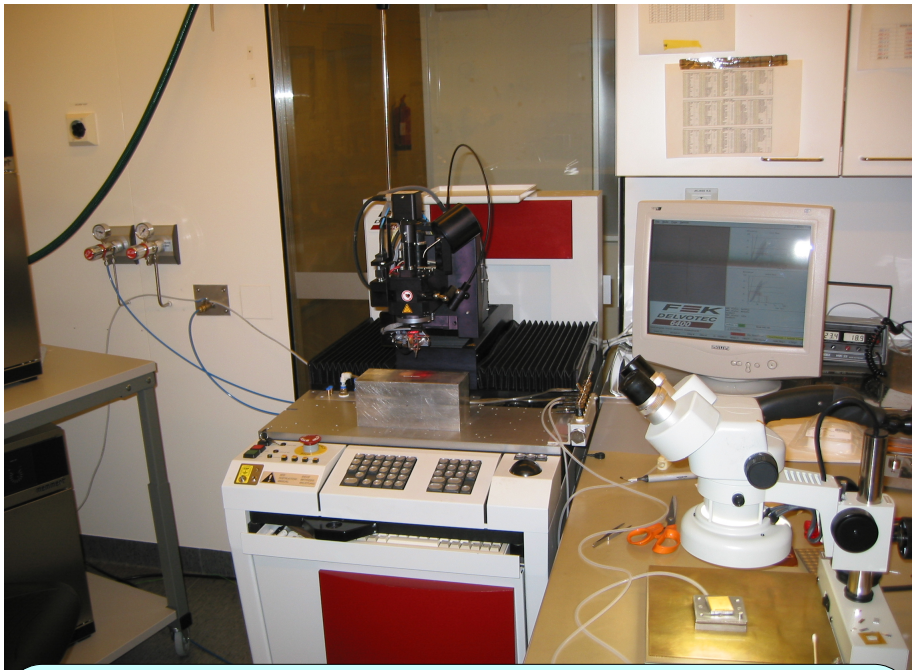
The signal spectra from 128 channels of one SVX4 chip, sensor is not attached. The test pulse of 31.5 fQ (1.26V on 25fF) is applied to every 8th channel. Signal/Noise > 20.

Next Steps. Testing With Beta-Source

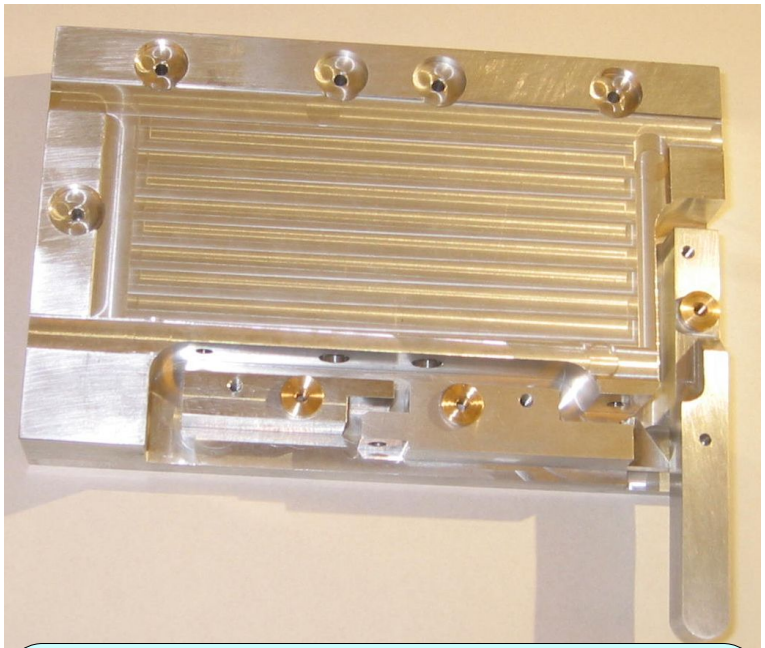


Stand for testing stripixel modules with beta-source.
Prepared by Ed Baker, BNL, Physics

Next Steps. Assembly Lines in Helsinki and Dubna



Wirebonding station at Institute of Physics, Helsinki.



Jig for stripixel assembly for use in Dubna.

Part 2. Readout of Pad Sensors

Main Contributors

- BNL, Physics:
  Edward Kistenev, Andrey Sukhanov, Steve Boose
- BNL, ID:
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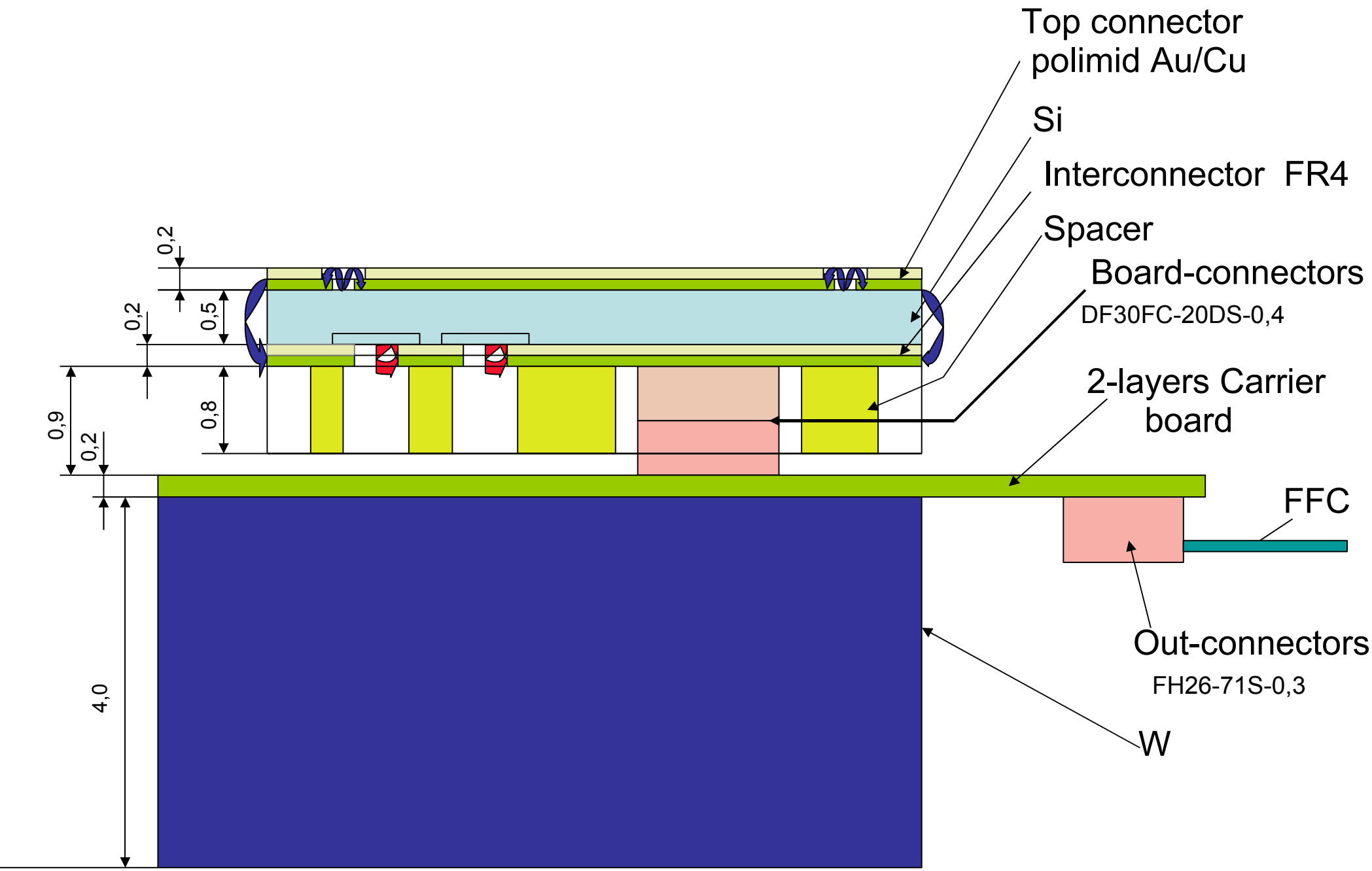
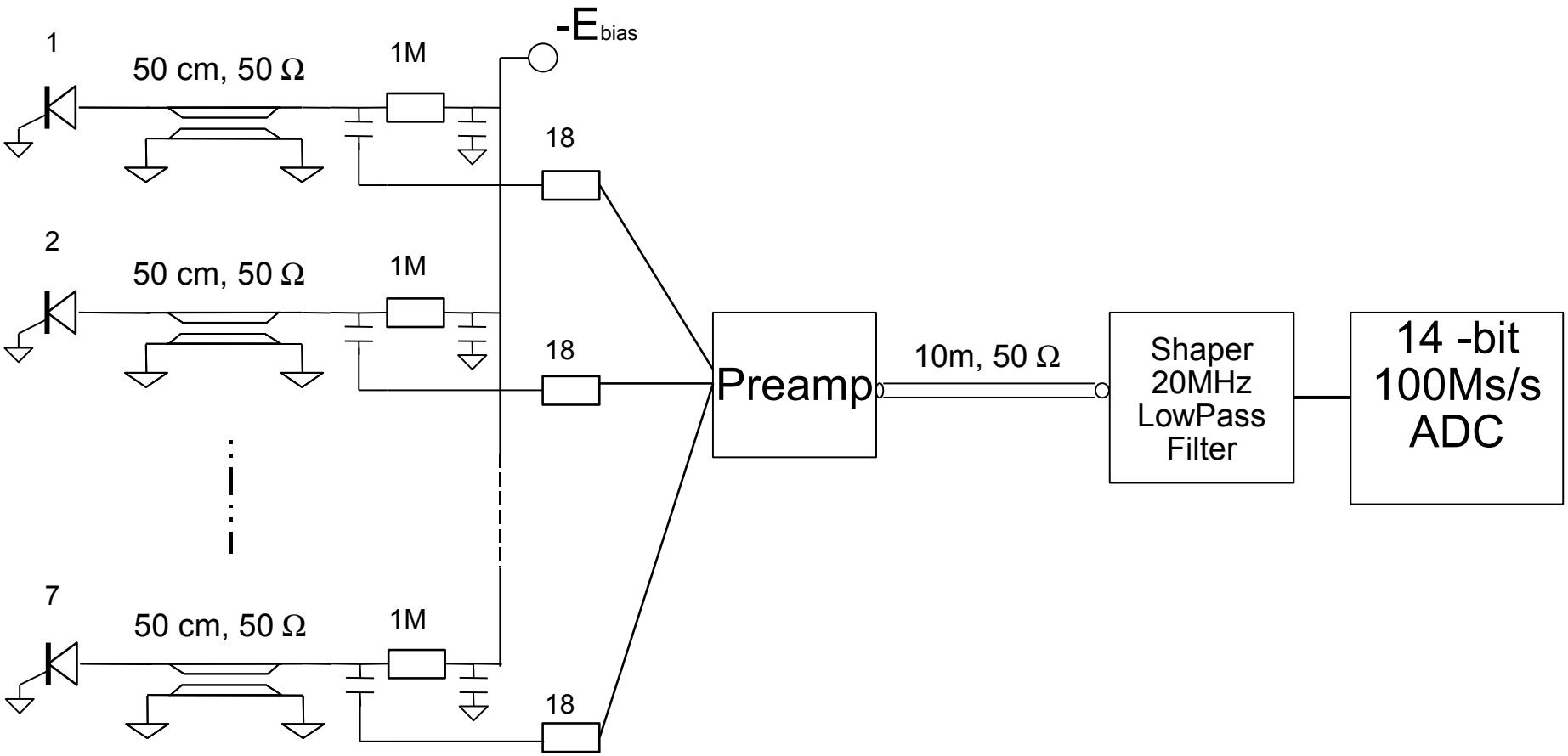
- Dubna, LPP:
  Nikolay Zamiatin
- Nevis Labs:
  Cheng-Yi Chi
- Moscow, MSU:
  Mikhail Merkin, Alexander Voronin

Presentation of Sergey Basilev

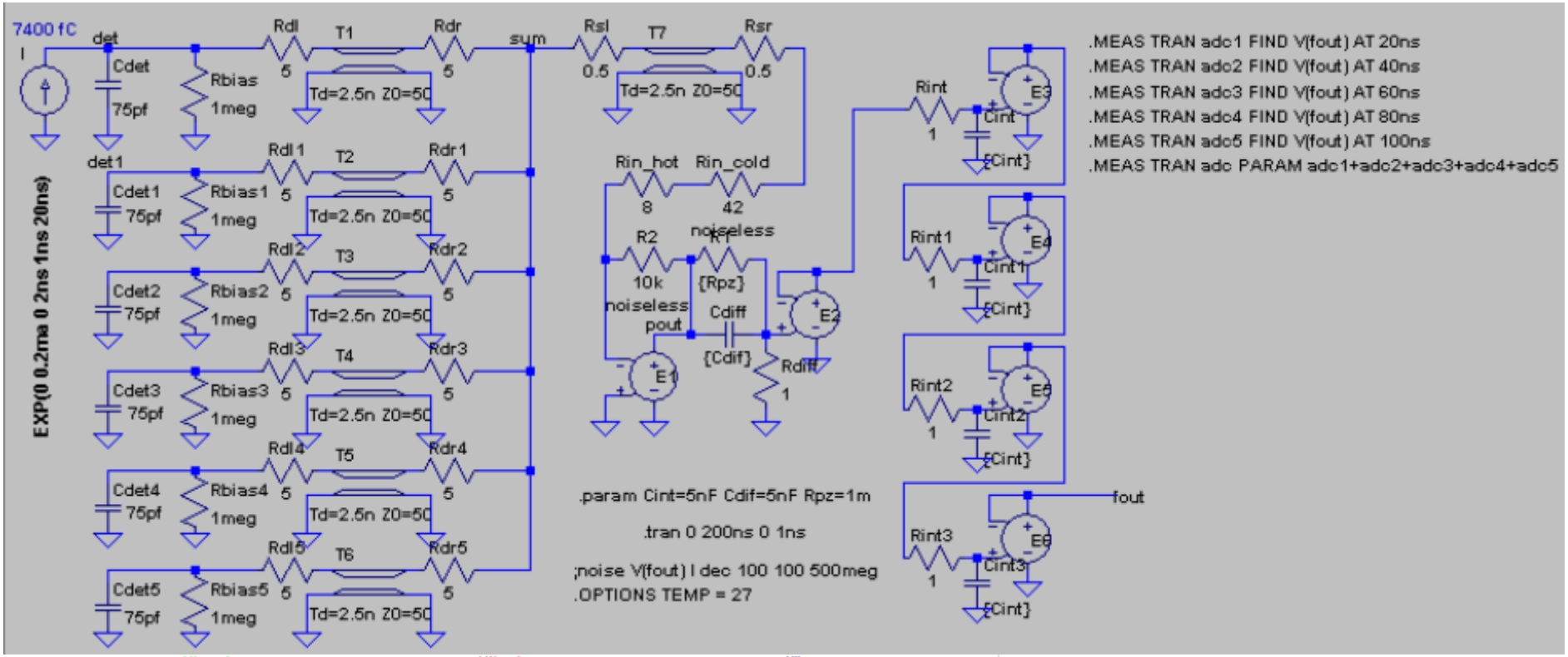
Pad Sensor Sampling Layer

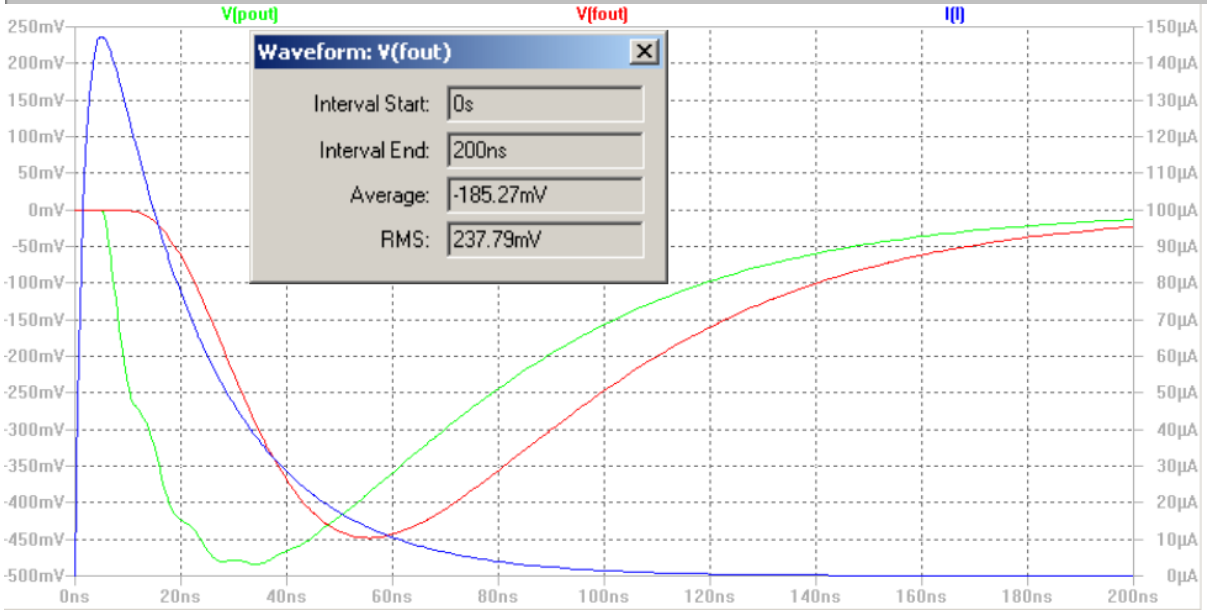


Analog Chain of Pad Sensors



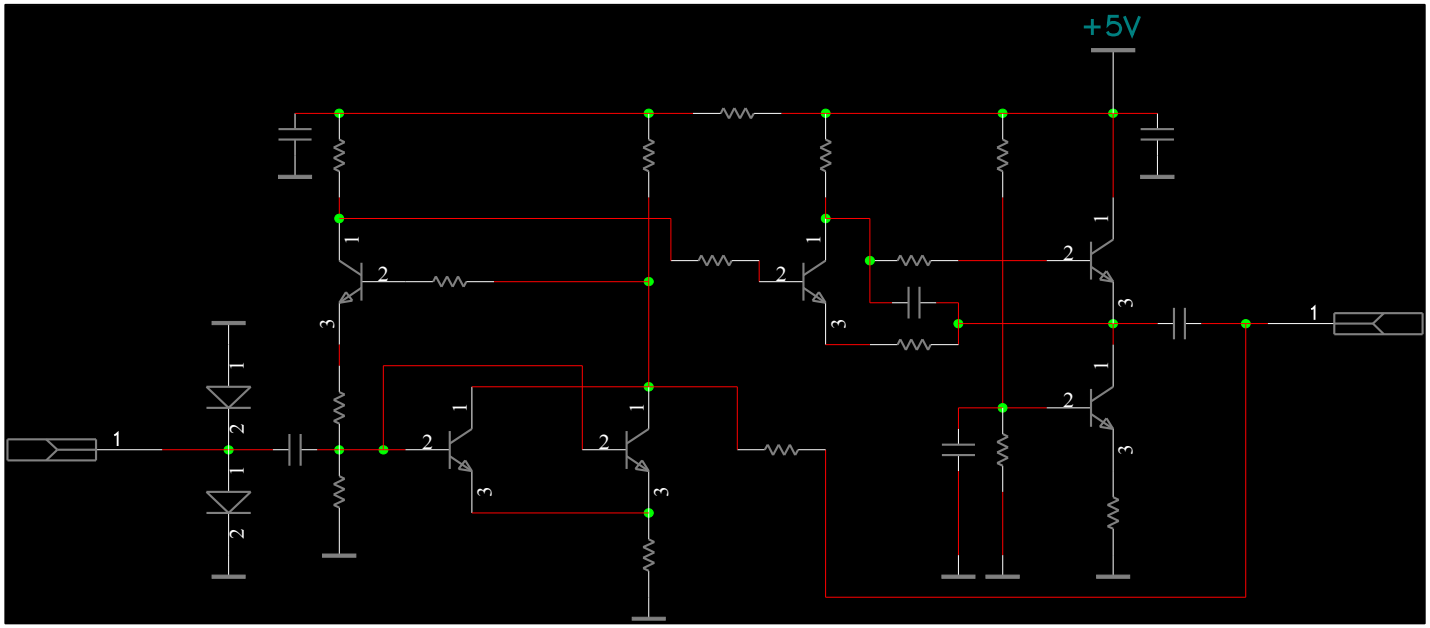
Simulation of Summation Scheme



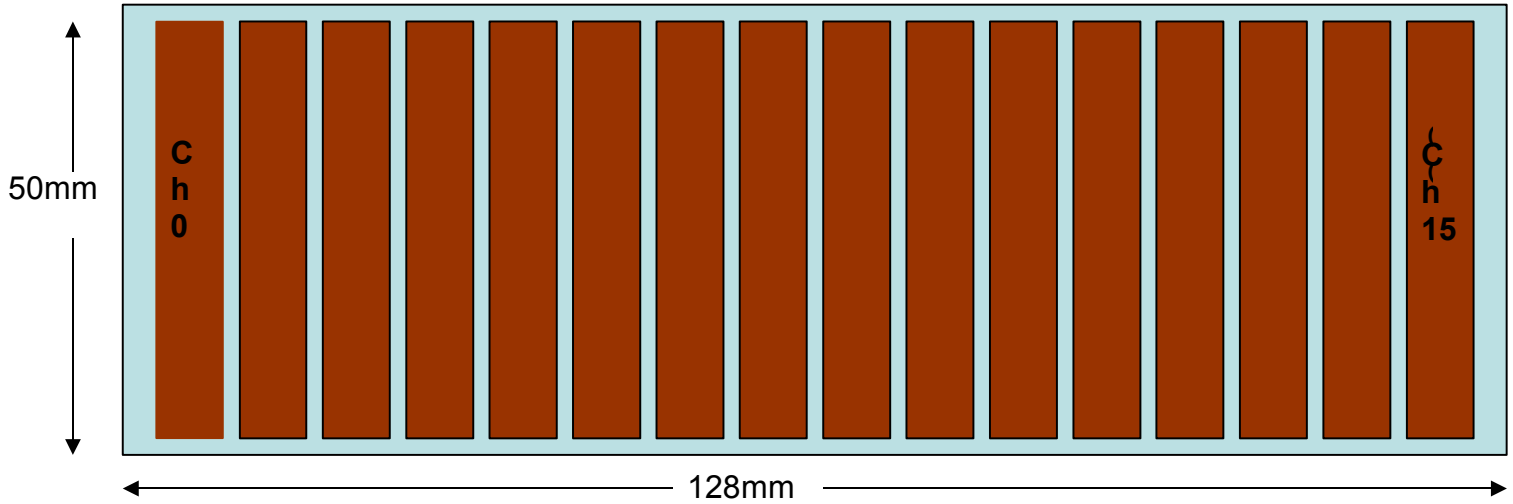


LTSpice simulation of summation scheme with ideal preamplifier and RC(4) filter. (CR and pole-zero cancellation are disabled)

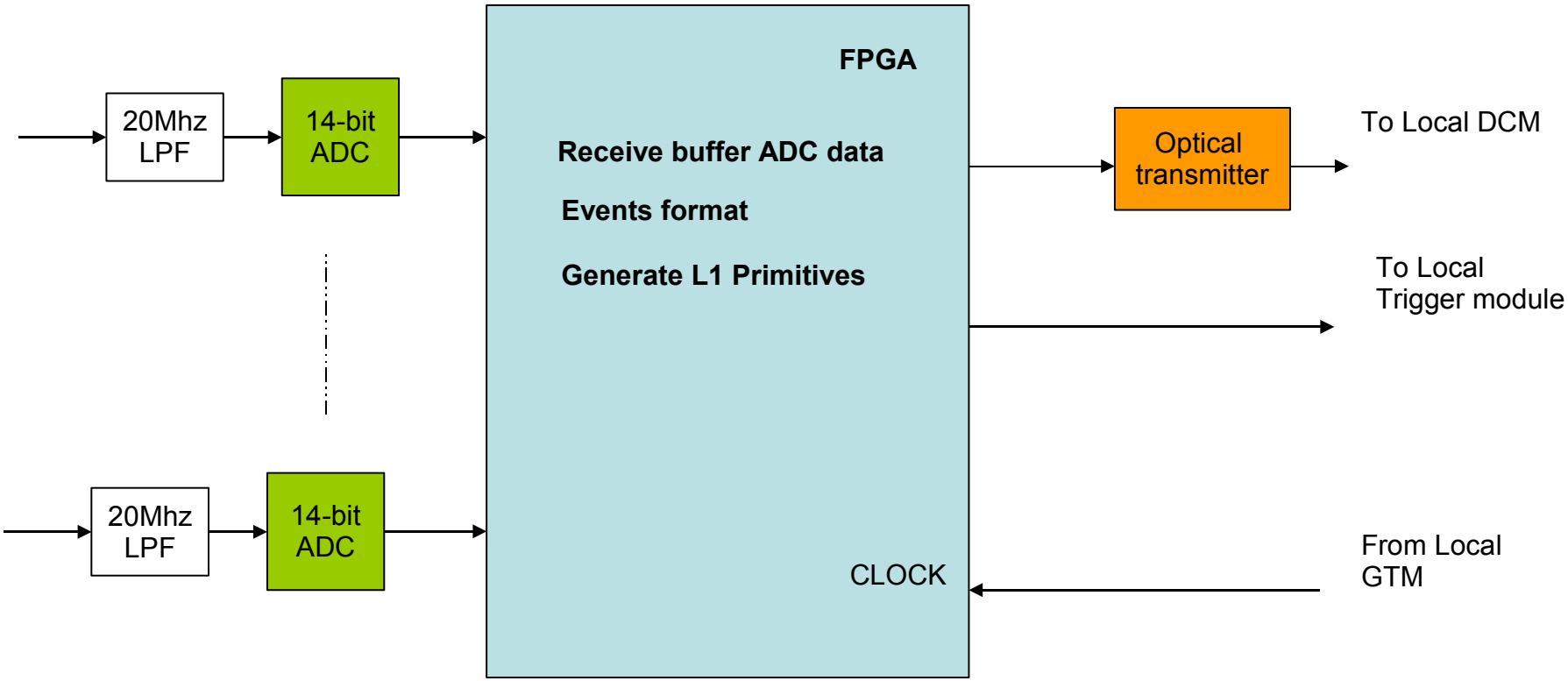
Schematics of Modified Preamplifier



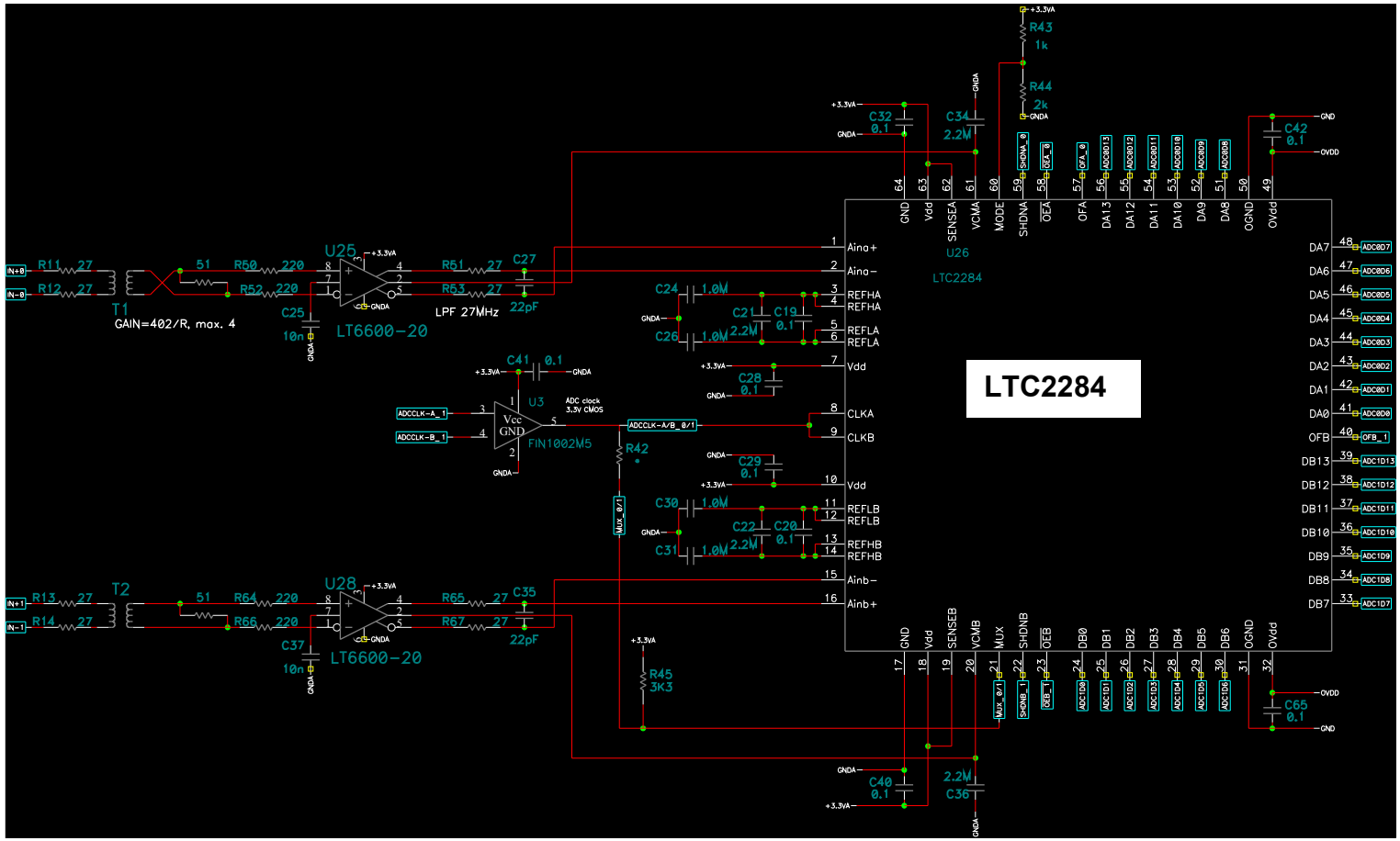
Board spacing for 16-ch Preamp.



Digital Chain of Pad Sensors



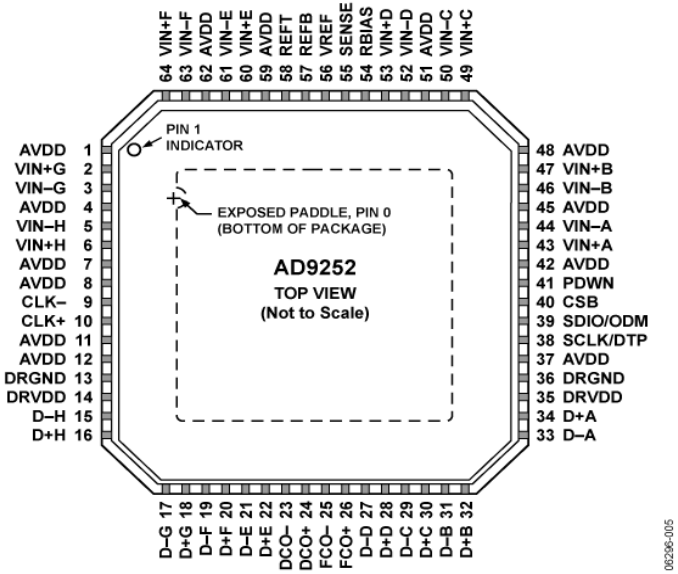
Input Part of 16-channel ADC



Better ADC Chip AD9252

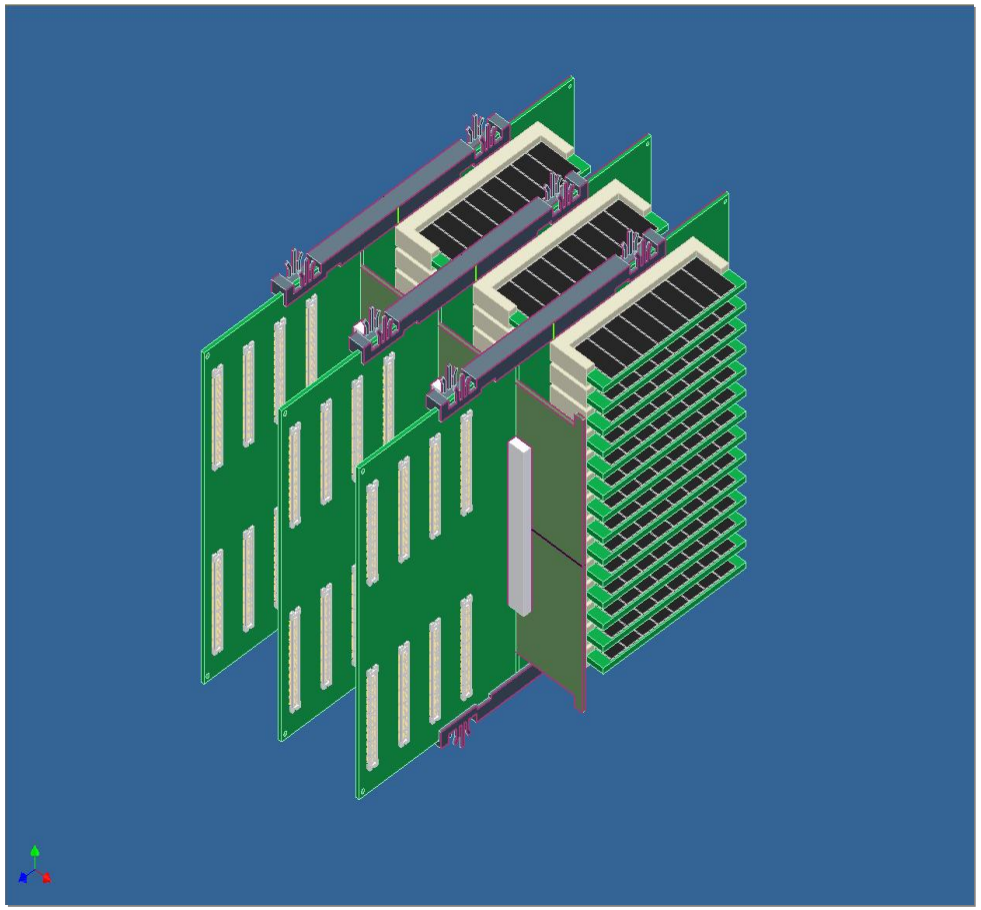
AD9252 Octal, 14-bit, 50 MSPS Serial LVDS 1.8 V A/D Converter

- 8 ADCs integrated into 1 package
- 93.5 mW ADC power per channel at 50 MSPS
- SNR = 73 dB (to Nyquist)
- Excellent linearity
  DNL = ±0.4 LSB (typical)
  INL = ±1.5 LSB (typical)
- Serial LVDS (ANSI-644, default)
  Low power reduced signal option, IEEE 1596.3 similar
- Data and frame clock outputs
- 325 MHz full power analog bandwidth
- 2 V p-p input voltage range
- 1.8 V supply operation
- Serial port control
  Full-chip and individual-channel power-down modes
  Flexible bit orientation
  Built-in and custom digital test pattern generation
  Programmable clock and data alignment
  Programmable output resolution
  Standby mode



64-LEAD LEAD FRAME CHIP SCALE PACKAGE [LFCSP_VQ]
9 mm × 9 mm BODY, VERY THIN OCTAL
(CP-64-3)

Readout Crate



Summary and Plans. Stripixels.

- Readout of SVX4 chain is working. Proper response from calibration pulses have been measured.
- One test station is assembled.

Plans:

- Make measurements with attached pitch adapters and sensor.
- Implement slow control for bias monitoring.
- Make measurement with applied bias voltage.
- Test with beta source at BNL.
- Assemble two more test stations.
- Test with alpha source in Dubna.
- Production of final version of SRC.
- Assembly of 2 stripixel+strip ladders for full prototype.
- Install stripixel+strip ladders at PHENIX for rad. damage tests.

Summary and Plans. Pads.

- Convenient assembly procedure is developed, at allows for easy replacement of sensor modules.
- Preamplifier with proper polarity and single power supply tested on the breadboard.
- Layout of all components of the sensor subassembly and for carrier board is finalized.
- Schematics for 16-channel 14-bit ADC is ready.

<u>Plans:</u>

- Manufacture all components of subassembly module and carrier board.
- Manufacture summing board.
- Manufacture preamplifier.
- Assemble pad sensors readout chain including sensor subassembly, summing board and preamplifiers.
- Production and assembly of ADC boards.
- Tests of the full readout chain

Backup Slides. Power Consumption.

Power consumption

<u>Inside EM brick</u>
SVX4: 0.3W, 24*2 chips per brick = 30 W

<u>Electronic enclosure</u>
IO82X: <0.1W/ch, ~400 ch per brick = 40 W