NCC FEM Specification

There are 7 bricks in the NCC halfdisk. There are two Si-strip ladders in the brick. One FEM module reads out two Si-strip ladders. The Si-strip ladders may contain 5,6 or 7 SEMs (Silicon-End Modules). Each SEM contains two Si-strip sensors, each sensor is read out by two SVX4 chips.
The two readout chains are combined together and are fed to a SPARTAN FPGA. The FPGA buffers the event in input buffer, compresses the data stream using Huffman Coding, stores the result in the output buffer and sends it through the optical transceiver to the NCC FEM.

The FEM connects to the PHENIX DAQ over a small-form-factor (SSF) optical transceiver (preferably 2.125 GBPS HFBR-5720AL). The receiving part of it is connected to a PHENIX GTM module, while transmittter part – to a PHENIX DCM module.

The FEM receives form GTM following signals:

Phenix Synchronization Signals	
Mode_Bit[7:0]	8
Beam Clock 9.4 Mhz	1
LVL1_Accept	1
Mode_Enable	1
EndDat[1:0]	2
UserBit[2:0]	3
Reserved[3:0]	4
Total	20 Bit

Table 1.

These signals are deserialized using a serdes chip (preferably TLK2501). The clock is defined by a Phenix GTM, it is four times the Beam Clock, i.e 37.6 Mhz. This clock is recovered by the serdes chip, the clock jitter is guaranteed to be less than 40 ps.

Time budget

Digitization and Readout Time		
SVX4 Front-End Clock	37.6	Mhz
Digitization time	3.4	us
Longest SVX4 chain	16	
Number of SVX4 chains per BEM	4	
SVX4 Back-End Readout Clock	37.6	Mhz
Number of SVX4 chains per BEM	4	
Chain size for calibration run	4128	Bytes
Receiving time for calibration run	54.89	us
Occupacy	5%	
Average chain size	236.8	Bytes
Average Readout Time	3.15	us

Table 2.

Data Transfer Time		
Beam Clock 9.4 Mhz	9.4	Mhz
GTM GLINK Clock	37.6	Mhz
SVX4 Back-End Clock	53	Mhz
Input data size, without pedestal suppression	14448	Bytes
Output data size, without pedestal suppression	7284	
Compression factor for unsuppressed data	2.5	
Compressed output data, calibration run	2914	Bytes
Hit occupancy	5%	
Output data size, pedestal suppressed	829	Bytes
Compression factor for suppressed data	3	
Output data size, suppressed & compressed	276	Bytes
DCM receive clock	37.6	Mhz
Data transfer time, calibration run	77.49	us
Data transfer time pedestal-suppressed and compressed	7.35	us

Table 3.

The digitization with 37.4 Mhz Front-End clock will take 3.4 us
For normal data taking with pedestal suppression and Huffman compression the estimated data size from the single brick is 276 bytes. With DCM GLINK clock of 37.4 Mhz this data will be transferred in **7.35 us**. This is fits safely into PHENIX DCM data taking window (ENDAT) of **40 us.**

Note. Even for calibration runs when pedestal suppression is switched off the data size will be reduced from 14.5 Kbytes to 3.0 KB by removing ChannelID bytes from the SVX4 data and applying Huffman compression. The data transfer time in this case will be 77.5 us which can be handled by single DCM by occupying two ENDAT windows of the DCM.

FPGA Selection

Memory Requirements

BEM Memory Requirements		
Number of ladders in brick	2	
Max Number of SEM in a Ladder	7	
Number of SVX4 in SEM	4	
Max Number of SVX4	56	
Number of channels	7168	
Max data size per SVX4	258	Bytes
Max input data size	14448	Bytes
Number of input buffers	1	
Output data size unsuppressed	7284	Bytes
Compression factor for unsuppressed data	2.5	
Output data compressed	2914	Bytes
Hit occupancy	5%	
Output data size, pedestal suppressed	829	Bytes
Compression factor for suppressed data	3	
Output data size, suppressed & compressed	276	Bytes
Size of the pedestal memory	7168	Bytes
Size of the Huffman coding map	512	Bytes
Total memory requred	**29412**	**Bytes**
	235296	**Bits**

Table 4.

FPGA	Dist RAM [Kbits]	Block RAM [Kbits]	DCM	FT256 IO USER	FT256 IO DIFF	Price	Source
XC3S500E	73	360	4	190	77	?	
XC3S1200E	136	504	8	190	77	?	
XC3S400	56	288	4	173	76	$27.76	digikey
XC3S1000	120	432	4	173	76	$47.87	digikey

Table 5. Spartan FPGA.

XC3S400 has enough memory resources.

Number of LVDS pairs.

According to table3 the FEM should process data from four SVX4 chains in parallel. This will require

1. Data transfer bus 4*9 = 36 LVDS pairs.
2. Common clocks BECLK, FECLK. = 2 LVDS pairs
3. PRIOUT[0] 4*1 = 4 LVDS pairs
4. Optional PIOUT[3:1] 4*3 = 12 LVDS pairs

In total it is 40 obligatory and 12 optional pairs
The XC3S400 has 76 pairs.

Ports

SVX4_Chain[3:0] ports

These ports carry signals only, the power, HV and ground for SVX4 will be routed separately on the LDR board.
The longest SVX4 chain is 16 SVX4 chips, see table 2. For better reliability the chain control signals PRIIN and PRIOUT are broken into four groups (PRIIN3:0, PRIOUT3:0) each serving one SEM module. This adds flexibility to bypass any group for configuration or readout.

SVX4Chain Port			
Pin	Signal	Pin	Signal
1	PRIIN1	2	PRIOUT1B
3	PRIOUT2B	4	PRIOUT1
5	PRIOUT2	6	PRIOUT0B
7	PRIIN2	8	PRIOUT0
9	1WIRE	10	BUS7B
11	1VDD	12	BUS7
13	BECLKB	14	BUS6B
15	BECLK	16	BUS6
17	L1A	18	BUS5B
19	CALSR	20	BUS5
21	PRD2	22	BUS4B
23	PRIIN0	24	BUS4
25	FEMODE	26	BUS3B
27	PRD1	28	BUS3
29	BEMODE	30	BUS2B
31	CHMODE	32	BUS2
33	PARST	34	BUS1B
35	PRIOUT3B	36	BUS1
37	PRIOUT3	38	BUS0B
39	PRIIN3	40	BUS0
41	AGND	42	ODBVB
43	DVDD	44	ODBV
45	DVDD	46	GND
47	DVDD	48	FECLKB
49	GND	50	FECLK

JTAG ports

JTAG_COMMON Port		
1	VCC	
2	GND	
3	TCK	
4	TDI	Connected to
5	TDO	Connected to
6	TMS	

JTAG_IN Port	
1	TDI

JTAG_OUT Port	
1	TDO

JTAG_COMMON port connects PCM (Power and Control Board) to all FEMs in parallel. JTAG_IN and JTAG_OUT are daisy chained.

DEBUG PORT

DEBUG Port			
1	SCL	1	I2C Clock
2	SDA	1	I2C Data
3	I2C_CS	1	I2C Chip Select.
4	CLKOUT	1	
5	QSPI_CLK	1	
6	QSPI_DIN	1	
7	QSPI_DOUT	1	
8	QSPI_CS[2:0]	3	
11	IRQ	1	

This port is to control the FEM boards from the PCM. It provides

1. I2C link to 1WIRE Master chips on all FEM modules
2. QSPI link to set and read internal registers of all FEM modules.

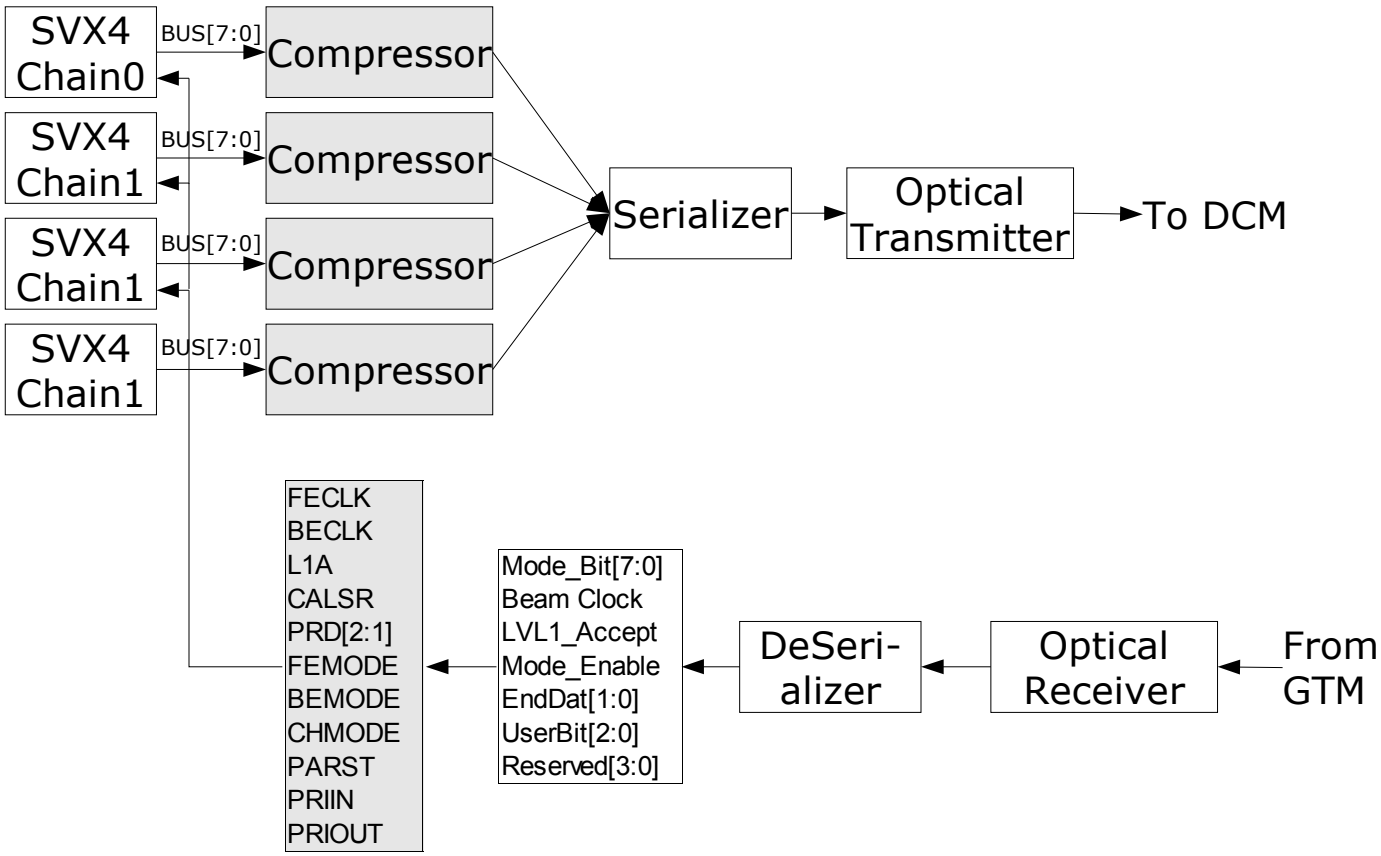

Fig 1. FEM Block Diagram

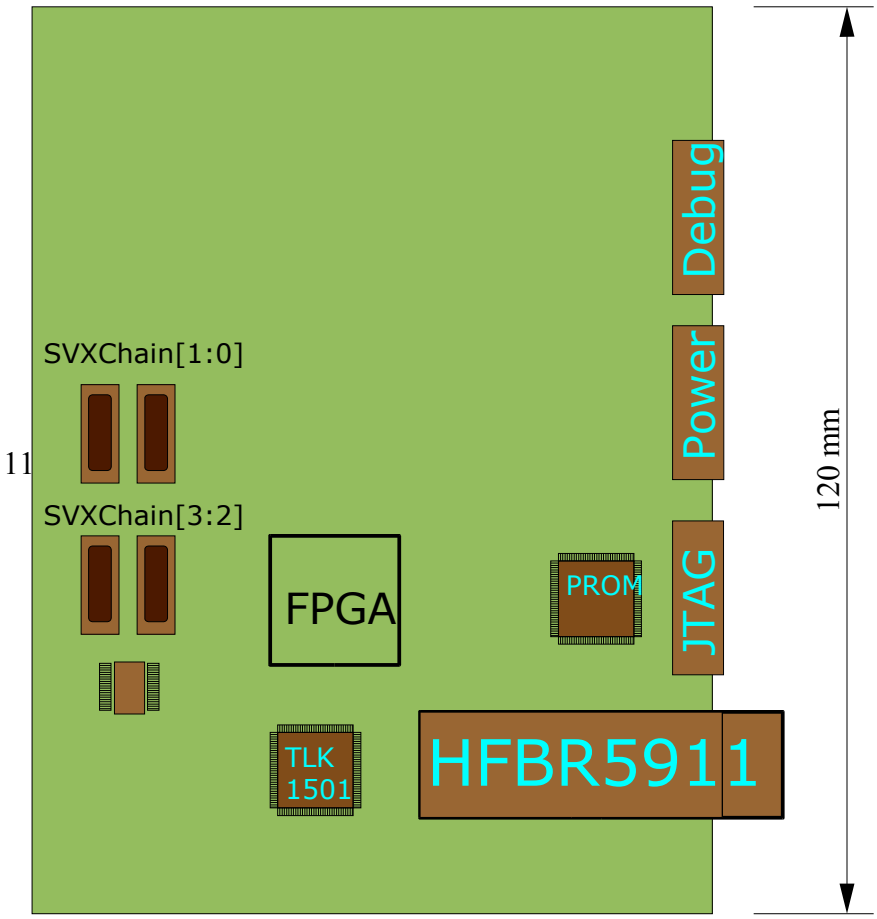

Fig. 2. FEM dimensions