Chapter 4

LINE TERMINATING PREAMPLIFIER

4.1 Introduction

As explained in Chapter 2, in order to maximize the signal-to-noise ratio for the readout of high capacitance noble liquid calorimeters, it has been common practice to use very short connections between the detector and the preamplifier so as to minimize the inductance (and capacitance) of the connection itself [59]. In Chapter 2 Section 3.2.2 and in [21], it was shown that, under certain circumstances, as good, or even slightly better signal-to-noise ratios could be achieved with a transmission line connecting the detector to the preamplifier. This can be true, provided that:

1. the shaping time is of the order of, or shorter than the transmission line propagation time. Pile-up considerations (see 2-4) mandate a short shaping time for the readout of calorimeters at hadronic collider experiments;

2. the reactance of the detector capacitance is of the order of the transmission line characteristic impedance at the center frequency of the shaping filter which in the time domain translates into the requirement that the input time constant, determined by the detector capacitance and the transmission line impedance be not long compared to the shaping time.

To prevent multiple reflections, the transmission line must be terminated in its characteristic impedance at the preamplifier [23]. A physical resistance should not be used as it would normally be the dominant noise source. Conventionally [20], an “electronically cooled” termination is used, created by an operational amplifier with capacitive feedback, whose input resistance is, approximately:

$$\frac{C_p}{g_m \; C_f} \qquad 4\text{-}1$$

where C_p is the dominant pole capacitance of the operational amplifier, C_f is the feedback capacitance and g_m is the input element transconductance.

This solution works well, provided that the input signal amplitude is not so large as to produce significant changes in the input amplifier transconductance. In the case of liquid argon calorimeters on high energy accelerators, this may not be the case, since signal currents may approach 10 mA and the corresponding voltage signal at the preamplifier input can substantially change the transconductance. A solution to stabilize the input impedance by means of an additional feedback loop has been published [60], but it is not optimized for low power.

The preamplifier configuration presented in [21], and reproduced here as Figure 4-1, is better

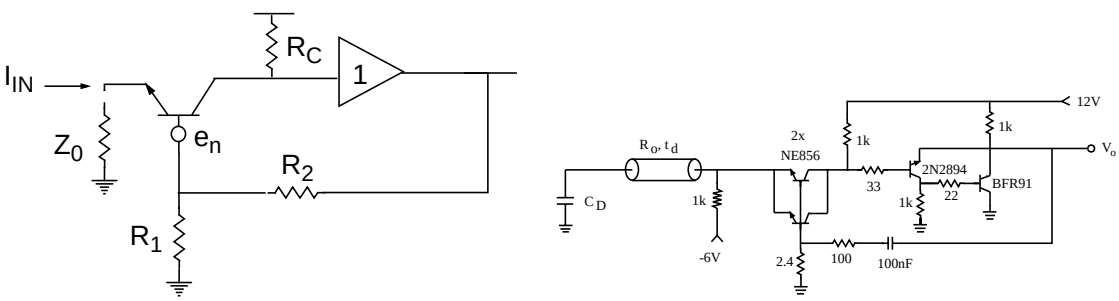


Figure 4-1. Circuit schematic of the transmission line terminating preamplifier described in [21]. It has a power dissipation of 140 mW.

adapted to these high dynamic range applications.

Summing the voltages from ground to base and from base to emitter of the input transistor, we find the input voltage $V_{in} = r_e \, I_{IN} + R_1/(R_1 + R_2) \, R_C \, I_{IN}$ where $r_e = 1/g_m$ is the dynamic input impedance and β is assumed infinity to disregard the small portion of the input current flowing into the base. The input impedance is computed as:

$$Z_{IN} = \frac{1}{g_m} + \rho \;\; R_C \qquad 4\text{-}2$$

where $\rho = R_1/(R_1 + R_2)$ is the feedback ratio. By adjusting ρ, the input impedance can be matched to the cable impedance.

The input transistor current is chosen to be high (about 4 mA) for low noise and to render the first term in Equation 4-2, which varies with signal amplitude, small compared to the second term.

Although this circuit works relatively well, it has a few drawbacks:

1. in the case of low impedance transmission lines (25 Ω), a very large input current would be necessary to make the first term in expression 2 small enough to achieve 1% non-linearity;
2. a high power supply voltage is required to prevent the input transistors from saturating with a large signal current, particularly if the dc current is also large. This leads to high power dissipation, limits the choice of input transistors and excludes the use of most integration technologies;
3. great care is required to prevent the input stage from oscillating at a high frequency (~ 1 GHz) since transistors with high f_T are required for a low value of the base spreading resistance $r_{bb'}$ and stopper resistors would add too much noise.

4.2 Reduced Power, High Linearity Line Terminating Preamplifier

To circumvent these drawbacks, a different circuit configuration was devised [61, 62] which, by assigning the functions of low noise and large dynamic range to different transistors, insures a better linearity while also allowing a reduction of the power dissipation.

Figure 4-2 shows a simplified schematic of the circuit. It consists of two nested feedback loops: an “inner” loop (T_1, T_2) which has the role to stabilize the input impedance against signal-induced changes, and an outer loop (unity gain buffer and series feedback on the emitter of T_2). The transistor T_2 amplifies the base-emitter voltage by a factor $G = g_{m2} \times R_{C2}$, effectively reducing the input impedance of T_1 (the first term in Equation 4-2) by the same factor. The outer loop adjusts the input impedance to the desired value as in the second term of Equation 4-2. The equivalent input impedance is, therefore:

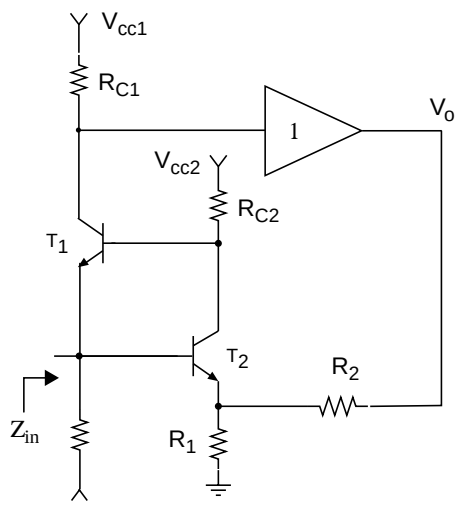


Figure 4-2. Simplified circuit diagram of the line terminating preamplifier. The external feedback loop increases the input impedance of the T_1 - T_2 inner loop to the value: $Z_{in} = (1/g_{m1} + R_{E1})/G + R_{C1} \times R_1/(R_1 + R_2)$.

$$Z_{IN} = \frac{1/g_{m1}}{G} + \frac{R_{C1}}{1 + R_2/R_1} \qquad 4\text{-}3$$

The circuit will be analyzed in more detail in the following paragraphs.

4.2.1 The Inner Feedback Loop

The role of the inner feedback loop (Figure 4-2) is:

A. to provide a low power, low noise input stage;

B. to stabilize the input impedance against signal induced charges and thus improve the integral non-linearity of the overall circuit.

The first goal is achieved by powering T_2, which is the dominant noise source from a reduced power supply (V_{CC2} = 3 V) with high current ($I_{C2} \cong$ 7 mA) to reduce the power dissipation. The second goal is the result of the local feedback.

Referring to Figure 4-3, the input impedance on the emitter of T_1 is:

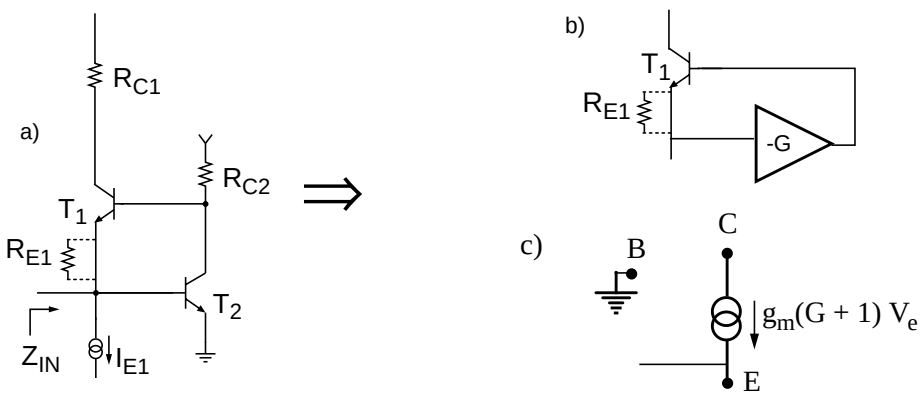


Figure 4-3. Feedback loop used to reduce the input impedance component dependent on the signal. The transistor T_2 and its collector resistor R_{C2} amplify the base-emitter voltage of the input transistor T_1. Hence, T_1 input impedance is reduced by the loop gain G. The resistor, R_{E1} (~ 100 Ω) in series with the emitter is necessary to stabilize the loop. The resulting input impedance is: $Z_{in} = (1/g_{m1} + R_{E1})/G$.

$$Z_{IN} = \frac{V_{E1}}{I_{E1}} = \frac{1/g_{m1}}{1 + G} \qquad 4\text{-}4$$

where $G = g_{m2} \; R'_{C2}$, and $R'_{C2} = R_{C2} \; // \left(\frac{\beta_1}{g_{m1}} + R_{E1}\right)$

Since $\beta_1/g_{m1} \cong 100 \times 25\ \Omega = 2500\ \Omega >> R_{C2}$ for 1 mA bias current we have $R'_{C2} \cong R_{C2}$ for a value of $R_{C2} = 200\ \Omega$. The gain G for $I_{C2} = 7$ mA bias and $R_{C2} = 200\ \Omega$ is $G = V_T / I_{C2} \times R_{C2} = 56$.

4.2.2 Stability of the Inner Loop

The stability is studied by means of the open loop transfer function $G_L(s)$ by opening the loop on the base of T_2 as in Figure 4-4. The input (emitter of T_1) is loaded by a capacitance simulating the detector C_D ~ 1 nF. A lengthy analysis of the equivalent circuit of Figure 4-4 under the assumption that $\beta_1 \to \infty$, r_{ce1}, $r_{ce}2$ are large with respect of the other resistors and by disregarding non-dominant terms yields:

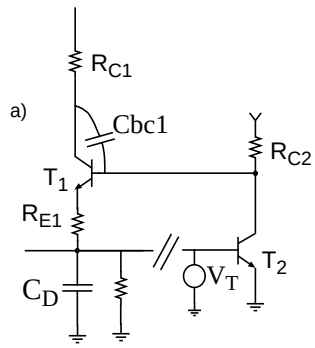


Figure 4-4. Open loop circuit for the study of the stability.

$$G_L(s) = \frac{\beta_2 R_{C2}}{r_{be2} + R_{E1}} \frac{1 + sR_{C1}C_{bc1}}{\left(1 + s\ \frac{C_D r_{be2}(1 + g_{m1}\ R_1)}{g_{m1}(r_{be1} + R_{E1})}\right) \times \left(1 + s\ \frac{C_{bc1}R_{C1}(1 + g_{m1}(R_{E1} + R_{C2}))}{1 + g_{m1}R_{E1}}\right)} \qquad 4\text{-}5$$

Figure 4-5 shows the root locus plot of the function 1-G_L(s) as the value of the resistor R_{E1} is varied from 0 to 500 Ω. At low R_{E1} values, the poles are complex conjugates with a large imaginary part leading to excessive ringing of the closed loop response. A value of R_{E1} ~ 100 Ω yields

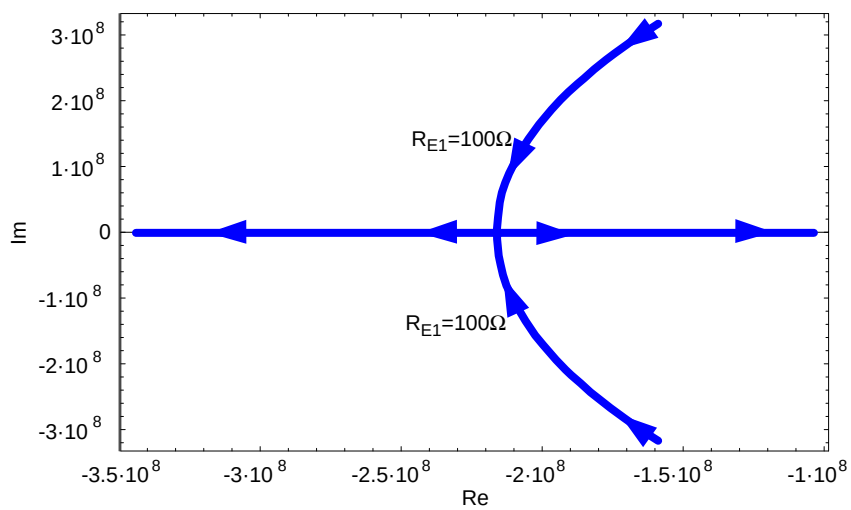


Figure 4-5. Root locus plot of the function 1 - G_L(s) as the resistor R_{E1} in Figure 4-4 is changed from 0 Ω to 500 Ω.

poles closer to the real axis with acceptable ringing, even more so when the pole due to stray ca-

pacitance on the collector of T_1 is taken into account. When the R_{E1} resistor is taken into account, the input resistance at the emitter T_1 becomes:

$$Z_{IN} = \frac{1/g_{m1} + R_{E1}}{G} \qquad 4\text{-}6$$

for G>>1. It can also be seen that R_{E1}, by degenerating the emitter of T_1, further reduces the variation of Z_{IN} as the signal current increases thus improving the integral non-linearity. Last, but not least, a resistive element in series with the emitter protects T_1 in case of a discharge in the detector injects a large charge into the preamplifier. This requirement will be discussed in more detail later.

4.2.3 Noise Analysis of the Inner Loop

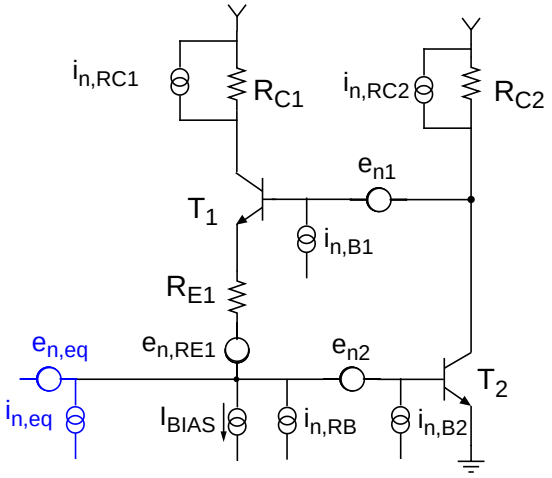


Figure 4-6. Equivalent circuit for noise calculation of the inner loop.

In general, the noise of a two-port network can be described by its equivalent series and parallel noise generators [53]. We now compute these equivalent noise generators for the inner feedback loop.

Let us consider the simplified inner feedback loop of Figure 4-6,where the noise sources have been shown.

It is easy to see that all the noise sources that contribute directly to the noise on the collector of T_2 may be represented by an equivalent noise generator on the base of T_2 divided by the loop gain G. The noise on the collector of T_2 can be expressed by:

$$e^2_{n,\,c2} = (i^2_{n,\,Rc2} + i^2_{n,\,B1})\ R^2_{C2} + e^2_{n1} + e^2_{n,\,RE1} \qquad \text{4-7}$$

assuming $\beta_2 >> 1$ so that the impedance into the base of T_2, $\beta_2/g_{m2} >> R_{E1}$ and where

- $i^2_{n,\,Rc2} = 4K_BT/R_{C2}$ is the thermal noise of R_{C2}
- $i^2_{n,\,B1} = 2qI_{B1}$ is the shot noise of the base current T_1
- $\frac{g_m e_n}{1/2} = 4TK_B\frac{1/2}{g_{m1}}$ is the equivalent series noise of the shot noise of the collector current of T_1

All of these noise sources can be represented by an equivalent noise source on the base of T_2:

$$e^2_{n,\,c2,\,equiv} = \frac{e^2_{n,\,c2}}{g^2_{m2}R^2_{C2}} = \frac{e^2_{n,\,c2}}{G^2} \qquad \text{4-8}$$

again assuming $\beta_1 >> 1$ so that the impedance into the base of T_1 is large compared with R_{C2}. From Equation 4-8, it can be seen that these noise contributions appear divided by the loop gain G, and are therefore second order terms when compared with $e^2_{n2} = 4K_BT\left(\frac{1/2}{g_{m2}} + r_{bb'2}\right)$, the noise generator representing the shot noise of the collector current T_2 and the thermal noise of its base spreading resistance.

Let us now compute the equivalent series noise generator $e_{n,eq}$, outside of the feedback loop, of e_{n2}. Its expression can be obtained by constructing the equivalent Thevenin generator of e_{n2}. To this extent we need to compute the unloaded voltage swing of the emitter of T_1 due to e_{n2}. The equivalent circuit is shown in Figure 4-7.

$$\begin{cases} V_{be1} = V_{b1} - V_{e1} = -(G+1)V_{e1} + e_{n2}\cdot G \\ g_{m1}V_{be1} + V_{be1}/r_{b1} = 0 \quad \Rightarrow V_{be1} = 0 \end{cases} \qquad \text{4-9}$$

which yields:

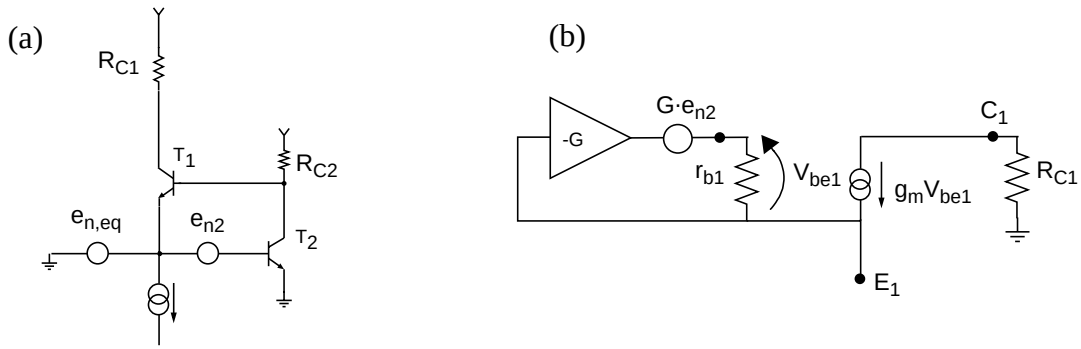


Figure 4-7. Simplified circuit for the calculation of the equivalent series noise voltage generator $e_{n,eq}$ of the generator $e_{n,2}$ (a) and its equivalent circuit (b).

$$V_{e1} = e_{n2} \cdot \frac{G}{G+1} \cong e_{n2} \qquad \text{4-10}$$

The equivalent noise generator will be, therefore:

$$e^2_{n,\,eq} \cong e^2_{n2} = 4K_BT\left(\frac{1/2}{g_{m1}} + r_{bb'2}\right) \qquad \text{4-11}$$

For a bias current of T_2, I_{C2} = 7 mA and an $r_{bb'2}$ = 2 Ω (achieved by paralleling two devices), we have

$$e_{n,\,eq} = [4K_BT(1.6\Omega + 2\Omega)]^{(1/2)} = 0.25\ \text{nV}/\sqrt{\text{Hz}} \qquad \text{4-12}$$

The equivalent parallel noise generator can be computed by shorting the input and calculating the noise current of the various sources. Assuming $\alpha_1 = 1$, the noise current $i^2_{n,\,Rc1} = 4K_BT/R_{C2}$ will give a full contribution, as well as the current sources connected to the base of T_2, namely the shot noise of the base current of T_2 and the thermal noise of the bias resistor R_{BIAS}. We have, therefore:

$$i^2_{n,\,eq} = \frac{4K_BT}{R_{C2}} + \frac{4K_BT}{R_{BIAS}} + 2qI_{B2} \qquad \text{4-13}$$

Assuming R_{C1} = 620 Ω, R_{BIAS} = 4 kΩ, and $I_{B2} = I_{C2} / \beta_2$ = 7 mA/150 = 47 μA, we have:

$$i_{n,\,eq} = 6.8\ \text{pA}/\sqrt{\text{Hz}} \qquad \text{4-14}$$

or the noise of an equivalent parallel noise resistor:

$$R_n = R_{C1} \,//\, R_{BIAS} \,//\, \frac{2\ V_T}{I_{B2}} = 620\ \Omega \,//\, 4\ \text{k}\Omega \,//\, 714\ \Omega = 306\ \Omega \qquad \text{4-15}$$

4.3 The Outer Loop

Another feedback loop (see Figure 4-2) is needed to achieve the desired input impedance. The input impedance can be computed by analyzing the equivalent circuit of Figure 4-8.

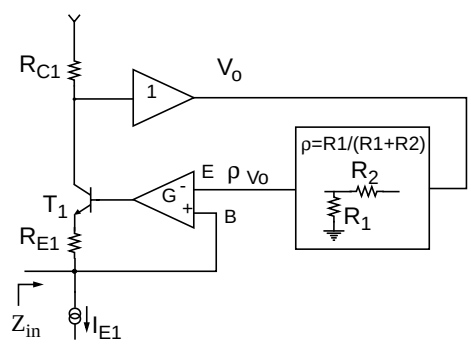


Figure 4-8. Equivalent representation of the circuit of Figure 4-3 for the calculation of the input impedance Z_{in} presented at the input.

which is the same circuit of Figure 4-3, with the outer feedback loop added. It is shown in Appendix A that the impedance looking into the emitter of T_2 is:

$$R_{E2} = 1/g_{m2} + R_{C2} \cong R_{C2} = 200\ \Omega \qquad \text{4-16}$$

and is, therefore, high with respect of R1 // R2 (R1 = 2.4 Ω for noise reasons, as it will be explained later). The load effect of R_{E2} on the feedback network can, therefore, be disregarded.

Defining $\beta = R_1/R_2$ as the feedback factor, we can write:

$$V_{OUT} = (V_{IN} - V_{OUT}\ \beta)\ G\ \frac{g_{m1}}{1 + g_{m1}R_{E1}}\ R_{C1} \qquad 4\text{-}17$$

which yields:

$$\frac{V_{OUT}}{V_{IN}} = \frac{G\ R_{C1}}{1/g_{m1} + R_{E1}} \Big/ \left(1 + \beta\ \frac{G\ R_{C1}}{1/g_{m1} + R_{E1}}\right) = \frac{\tilde{A}}{1 + \beta\tilde{A}} \qquad 4\text{-}18$$

where

$$\tilde{A} = \frac{G\ R_{C1}}{(1/g_{m1} + R_{E1})} = -A \qquad 4\text{-}19$$

is the opposite of the “forward” gain, as can be calculated looking at Figure 4-9.

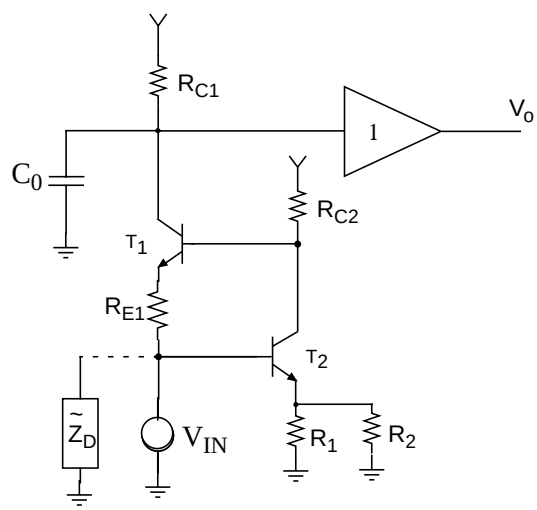


Figure 4-9. Simplified schematic for the calculation of the forward gain. The degeneration on the emitter of T_2 due to the loading effect of the feedback network must be taken into account.

$$A = \frac{V_{OUT}}{V_{IN}} = -\frac{I_{IN} \times R_{C1}}{V_{IN}} = -\frac{1}{V_{IN}}\frac{V_{IN}}{Z_{IN,\,OL}}\ R_{C1} = -R_{C1}\ \frac{G}{1/g_{m1} + R_{E1}} \qquad 4\text{-}20$$

by means of Equation 4-4, where:

$$G = \frac{R_{C2}}{1/g_{m2} + R_1 // R_2} \qquad 4\text{-}21$$

is the gain of the T_2 transistor taking into account the emitter degeneration due to the feedback network loading.

The closed loop input impedance can be calculated (assuming $\beta_1 \rightarrow \infty$, so that $\alpha_1 = 1$) as:

$$Z_{IN,\,CL} = \frac{V_{IN}}{I_{IN}} = \frac{V_{IN}}{I_{C1}} = \frac{V_{IN}}{V_{OUT}/R_{C1}} = \frac{1 + \beta\tilde{A}}{\tilde{A}} R_{C1} = (1 + \beta\tilde{A})Z_{OL} \qquad 4\text{-}22$$

which is the familiar expression of a series feedback amplifier input impedance.

By means of Equation 4-19, we have:

$$Z_{IN,\,CL} = \frac{(1 + g_{m1} R_{E1})}{G} + \beta R_{C1} = Z_{OL} + R_{C1} \frac{R_1}{R_1 + R_2} \qquad 4\text{-}23$$

The closed loop input impedance is, therefore, due to a small term ($Z_{OL} \sim 1.6\ \Omega$) weakly dependent on g_{m1}, which changes with the signal level, and a larger term, due to the feedback which is independent of the signal. When the bandwidth limitation, due to the capacitance C_0 on the gain point, the collector of T_1 (see Figure 4-9) is taken into account, one can see that a pole zero cancellation can be achieved by a small inductor in series with R_1:

$$Z_{IN} = \frac{1}{G}\left(\frac{1}{g_{m1}} + R_{E1}\right) + \frac{R_1 + sL_1}{R_1 + R_2 + sL_1} \frac{R_{C1}}{1 + sR_{C1}C_0} \qquad 4\text{-}24$$

By equating the time constant of the pole τ_0 and the zero $\tau_z = L_1/R_1$, it follows that:

$$Z_{IN} = \frac{1}{G}\left(\frac{1}{g_{m1}} + R_{E1}\right) + \frac{R_1}{R_1 + R_2} \frac{R_{C1}}{1 + sR_{C1}\left(C_0 \frac{R_1}{R_1 + R_2}\right)} \qquad 4\text{-}25$$

and the bandwidth is extended by a factor $1/\beta = (R_1+R_2)/R_1$.

4.3.1 Noise of the Outer Loop

It is a fundamental property of feedback circuits not to change the signal-to-noise ratio, except for the loading effects of the feedback itself and of course for the noise added by the feedback elements [18, 63]. This result stems from the fact that the feedback changes both the signal and noise transfer functions by the same factor, so that, even though the rms value of the noise at the output is indeed different, the signal-to-noise ratio remains unchanged.

The feedback network R_1-R_2 in the outer loop is made of resistive elements, so its effect on the noise is just the additional noise of these resistors. Since $R_1 << R_2$, it will be the dominant noise source. Also since the impedance seen into the emitter of T_2 is much larger than R_1, the equivalent noise generator of R_1 has the same effect as the noise generator in series with the base of T_2. The total equivalent series noise generator is thus given by Equation 4-11 with an additional term due to R_1, namely:

$$e_{nTOT,\,eq}^2 \cong e_{n2}^2 + 4K_BTR_1 = 4K_BT\left(\frac{1/2}{g_{m1}} + r_{bb'2} + R_1\right) \qquad \text{4-26}$$

For a bias current of T_2, $I_{C2} = 7$ mA, $r_{bb'2} = 2\ \Omega$ (achieved by paralleling two devices), $R_1 = 2.4\ \Omega$ and a stray resistance $R_{stray} \cong 0.3\ \Omega$ in series with the inductor L_1, we have

$$e_{nTOT,\,eq} = [4K_BT(1.6\Omega + 2\Omega + 2.4\Omega + 0.3\Omega)]^{(1/2)} = 0.32\ \text{nV}/\sqrt{\text{Hz}} \qquad \text{4-27}$$

A more precise calculation taking into account the second order terms that have been disregarded in Equation 4-27 gives a value of $0.35\ \text{nV}/\sqrt{\text{Hz}}$. The equivalent parallel noise generator is the same as in Equation 4-14, $i_{n,\,eq} = 6.8\ \text{pA}/\sqrt{\text{Hz}}$. The SPICE calculated equivalent series and parallel noise generators are shown in Figure 4-10, in good agreement with the calculated values.

4.3.2 Stability of the Outer Loop

The stability of this circuit topology has also been studied in [64].

According to the Nyquist criterion for stability [65], the closed loop circuit will be stable if the Nyquist diagram of the open loop transfer function $-G_L = \beta\tilde{A}$ does not encircle the critical point

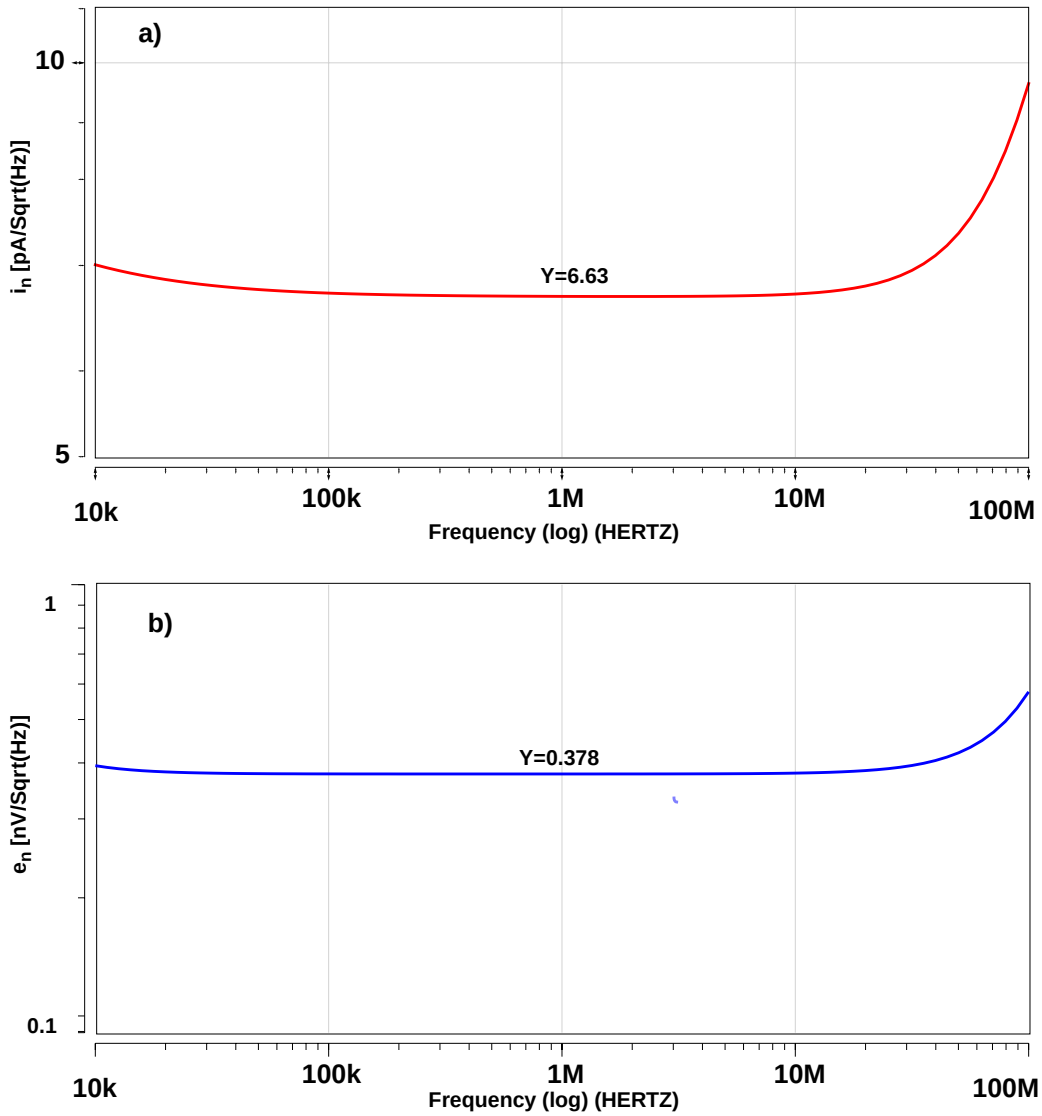


Figure 4-10. SPICE calculated parallel (a) and series (b) noise generators for the line terminating preamplifier. The component values are the ones in Figure 4-14.

(- 1 + j 0) in the complex plane in a clockwise direction. This is equivalent to the statement that the Nyquist plot of $1 + \beta\tilde{A}$ should not encircle the critical point (0 + j 0) of the complex plane.

While the direct measurement of the open loop transfer function requires modifications to the circuit, by recalling the relationship between the input impedance and the loop gain $Z_{IN,CL} = (1 + \beta\tilde{A})Z_{OL}$, one can express the Nyquist criterion in a form that lends itself to a direct measurement.

The stability criterion can be applied to the function $Z_{IN,CL}$ since the zeroes of $1 + \beta\tilde{A}$ are also the zeroes of $Z_{IN,CL,}$ assuming that Z_{OL} has no zeroes in the right half-plane, or equivalently that the open loop input admittance $1/Z_{OL}$ is a "stable" function, with no poles in the right half plane. This is the case if the inner loop is a stable circuit.

The Nyquist criterion can, therefore, be restated as:

> *"The closed loop circuit is unconditionally stable if the Nyquist plot of $Z_{IN,CL}$ will not encircle the critical point (0 + j 0) in a clockwise direction."*

This statement, of course, gives a condition of stability for the circuit of Figure 4-9, whose input is unloaded. When the preamplifier is connected to a detector, represented by the impedance $\tilde{Z}_D$ in Figure 4-11 - a, the effect of loading must be taken into account. By building the equivalent

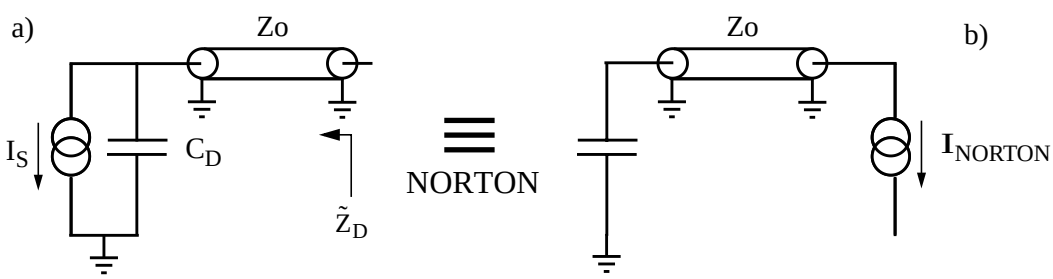


Figure 4-11. Equivalent Norton circuit of the detector connection to the preamplifier.

Norton circuit of the detector cable combination, as in Figure 4-11-b, one can calculate the output voltage as:

$$V_{OUT} = I_{NORTON} \; (Z_{IN,CL} \,//\, \tilde{Z}_D) \; \frac{1 + \beta\tilde{A}}{\tilde{A}} = I_{NORTON} \; \frac{1}{Y_{IN,CL} + \tilde{Y}_D} \; \frac{1 + \beta\tilde{A}}{\tilde{A}} \qquad 4\text{-}28$$

where $\tilde{Z}_D$ is the impedance seen looking into the transmission line connected to the detector. For an ideal lossless line [27] we have:

$$\tilde{Z}_D = Z_0 \; \frac{Z_D + jZ_0 \mathbf{tan}(\omega t_d)}{Z_O + jZ_D \mathbf{tan}(\omega t_d)} = j \; \frac{-1/(\omega C_D) + jZ_0 \mathbf{tan}(\omega t_d)}{1 + (\mathbf{tan}(\omega t_d))/(\omega Z_0 C_D)} \qquad 4\text{-}29$$

Equation 4-28 and [4-20], [4-22] allow the reformulation of the Nyquist criterion to assure the stability of the overall circuit when connected to a detector:

"The closed loop circuit, connected to an input load Z_D, will be stable if:

- *it is stable when unloaded, i.e., the Nyquist plot of $Z_{1N,CL}$ does not encircle (0 + j 0) in a clockwise direction;*
- *the Nyquist plot of the input admittance does not encircle the critical point (0 + j 0) in a clockwise direction".*

The quantity $Y_{IN,CL} + \tilde{Y}_D$ is the total input admittance of the preamplifier connected to a detector, and can be measured directly, even though the resulting Nyquist plot can be difficult to interpret.

An immediately applicable sufficient condition for stability can be deducted starting from Equation 4-28 and by recalling (Equation 4-22) that $(1 + \beta\tilde{A}) = Z_{IN,CL}/Z_{OL}$:

$$V_{OUT} = I_{NORTON}\ \tilde{A}\ \frac{Z_{OL}\tilde{Z}_D}{Z_{IN,CL} + \tilde{Z}_D} \qquad \text{4-30}$$

Provided that $\tilde{A}$ and Z_{OL} have no poles in the right half plane (which is always true for $\tilde{Z}_D$, a passive network), the stability can be gauged by the Nyquist plot of $Z_{IN,CL} + \tilde{Z}_D$, which must not encircle the critical point (0 + j 0). This quantity does not lend itself to an easy direct measurement though, since when the detector capacitance is connected through a line, only the ground near the detector is readily available, and this is not enough for injecting a voltage signal in series with $\tilde{Z}_D$. The measurement of $Z_{IN,CL} + \tilde{Z}_D$ at the preamplifier input is also not easy since it requires a floating voltage source. By recalling that for an ideal line connected to a pure capacitance, $\tilde{Z}_D$ is purely imaginary, a sufficient condition for stability is that the real part of $Z_{IN,CL}$ be always positive, since this precludes the encirclement of (0 + j 0).

Even if the line has losses, they will introduce a positive real term in the impedance $\tilde{Z}_D$, further enhancing the stability.

An easily applicable sufficient condition for stability of the outer loop can therefore be stated as [64]:

> *"The closed loop circuit, for any input loading condition, will be stable if the real part of the closed loop unloaded input impedance $Z_{IN,CL}$ is always positive."*

The real and imaginary parts of the measured input impedance of the three versions of the preamplifiers are plotted in Figure 4-12, and it can be seen they satisfy the stability condition.

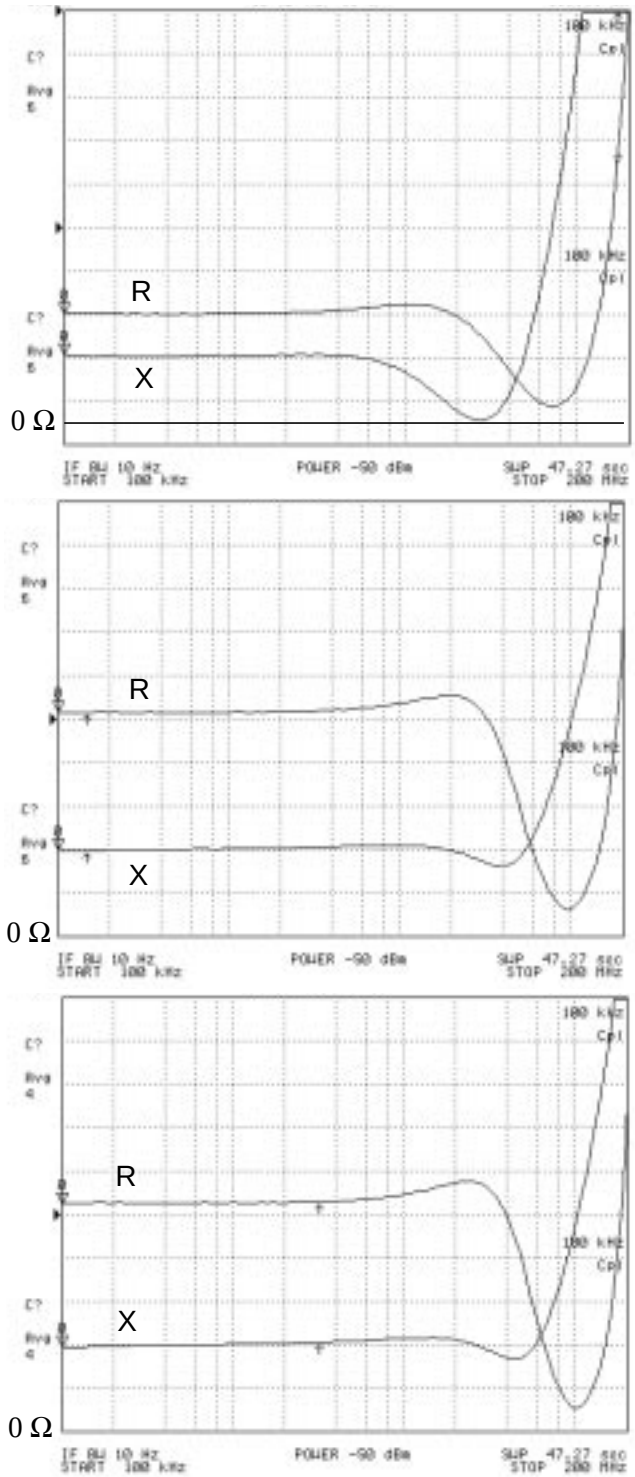
As an example of an unstable circuit, the case of an earlier version of the circuit, with a slower output buffer, is presented in Figure 4-13. When the circuit is loaded with a C_D = 1 nF at the input and the output 50 Ω termination is removed (which increases the gain), the circuit indeed becomes unstable and the critical points are encircled.

All types of preamplifiers have been tested for stability, both in the nominal condition and in a variety of failure modes of the connections (output open or shorted, input open, shorted or connected to various lengths of transmission line open or shorted at the end) and it has always been unconditionally stable.

4.4 The Output Buffer

Figure 4-14 shows the full schematic (power filtering and input discharge protection omitted) of the 25 Ω, high gain (1 kΩ transresistance) preamplifier. The output buffer has been realized as a White follower [66, 67] biased through a PNP current source: different transresistances for the circuit can be realized by simply changing the value of $R_{C1,}$ without having to readjust the bias of the White follower. The White follower consists of an NPN-PNP pair and is used as a low output impedance, low bias current output buffer.

Its signal transfer function can be studied by referring to the simplified schematic of Figure 4-15-a. If $\beta_2 \rightarrow \infty$ and $R_{C1} \rightarrow \infty$, so that the open loop gain is very high, all the current to



Ch. 1 R 20 Ω/div
REF 90 Ω
50.277 Ω

Ch. 2 X 10 Ω/div
REF 80 Ω
633.99 mΩ

Ch. 1 R 5 Ω/div
REF 25 Ω
25.699 Ω

Ch. 2 X 10 Ω/div
REF 30 Ω
-396.01 mΩ

Ch. 1 R 5 Ω/div
REF 25 Ω
25.219 Ω

Ch. 2 X 10 Ω/div
REF 30 Ω
-685.14 mΩ

Figure 4-12. Measured real and imaginary part of the unloaded input impedance of the three versions of the line terminating preamplifier. The real part of the impedance is always positive, thus assuring stability

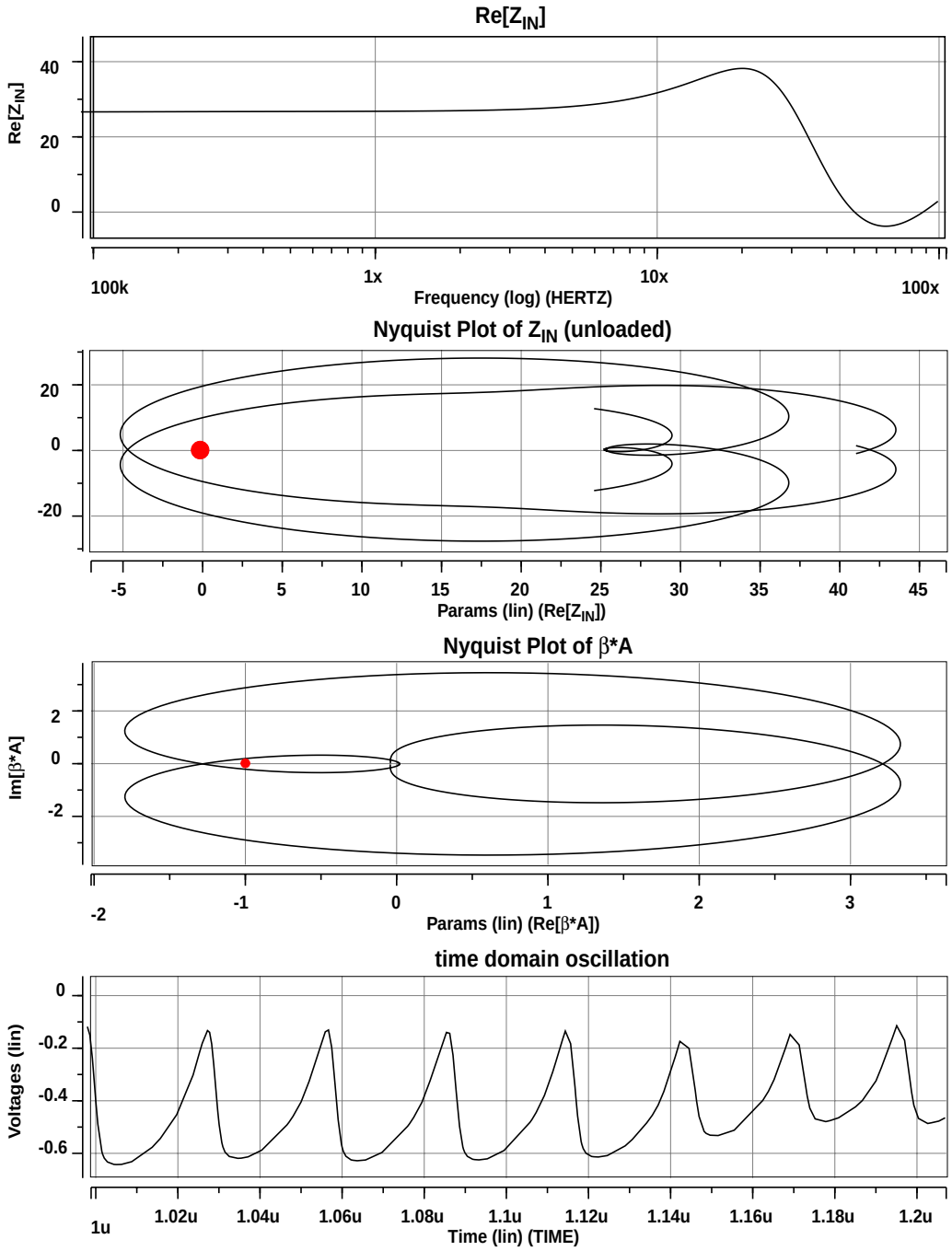


Figure 4-13. Stability plots for an earlier version of the 25 Ω line terminating preamplifier equipped with a slow buffer, with a capacitor of 1 nF connected directly at the input. The output 50 Ω termination has been removed, which causes an increase of the gain sufficient to make the circuit oscillate.

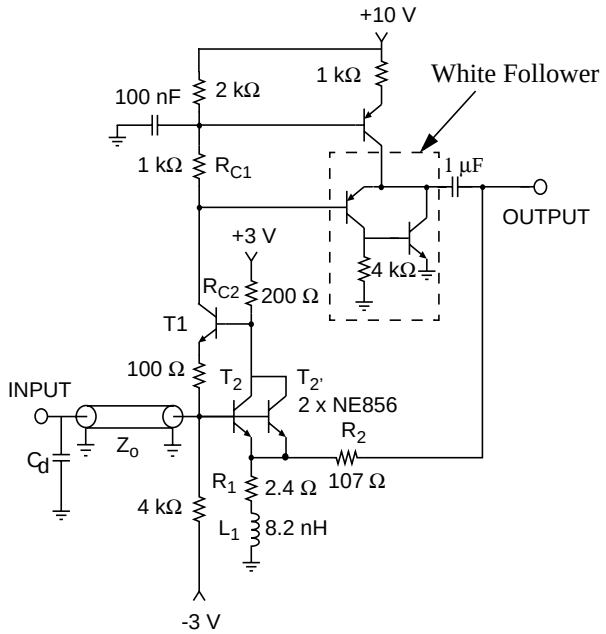


Figure 4-14. Full schematic of the line terminating preamplifier for Z_{in} = 25 Ω and a maximum input current of 5 mA. Power supply filtering and discharge protection network not shown.

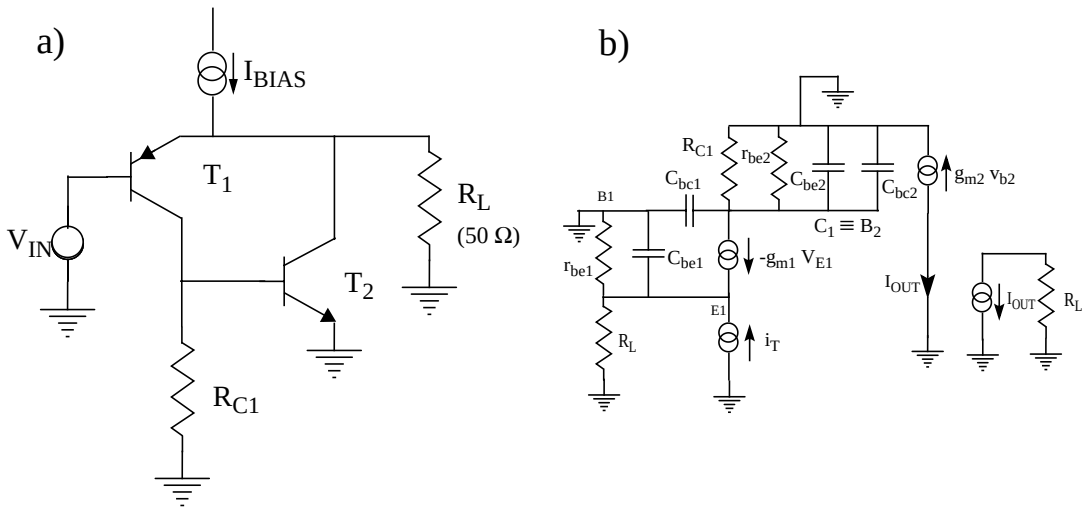


Figure 4-15. Simplified schematic of the White follower (a) and equivalent circuit for the calculation of the open loop gain (b). The loop has been opened at the emitter of T_1 and for simplicity the collector of T_2 has been grounded.

the load will be delivered by T_2. The collector current of T_1 (which provides the base current of T_2) need not change, and therefore its base-emitter voltage will be constant, or namely

$$V_{OUT} = V_{IN} \tag{4-31}$$

The White follower thus acts as a unity gain buffer. Since $I_{C1} \cong I_{E1}$ does not change, the collector current of T_2 will be

$$i_{C2} = \frac{v_{IN}}{R_L} \tag{4-32}$$

Since modern bipolar transistors have consistently high β (for a NE856 transistor $\beta_{NOM} = 150$ and $\beta_{MIN} = 100$), the collector current of T_1 will indeed be very low, so that it can be biased at low standing current ($I_{C1} \cong 200\ \mu A$).

Let us now analyze the feedback loop. The feedback voltage V_{OUT} is added in series with the base emitter voltage of T_1: it is thus a series-series feedback. The input impedance will be high, increased by the feedback, while the output impedance will be low.

Like all circuits in which a low output impedance is realized by means of feedback, the output impedance will be inductive, making the circuit dangerously unstable when driving capacitive loads. The stability of the circuit can be analyzed by studying the open loop transfer function, as in Figure 4-15-b, in which for simplicity the collector of T_2 is connected to ground. The open loop transfer function is computed as the ratio I_{OUT}/I_T:

$$\begin{aligned}
&\frac{v_{E1}}{\dfrac{r_{be1} \,//\, R_L}{1 + sC_{be1}r_{be1} \,//\, R_{LO}}} + g_{m1}v_{E1} = -I_T \\
&\frac{v_{B2}}{r_{be2} \,//\, R_{C1}}(1 + sr_{be2} \,//\, R_{C1}C_T) = g_{m1}v_{E1} \\
&I_{OUT} = g_{m2}\ v_{B2}
\end{aligned} \tag{4-33}$$

where $C_T = C_{be2} + C_{bc2} + C_{bc1}$.

By defining:

$$R'_L = R_L \,//\, r_{be1} \cong R_L$$
$$R'_{C1} = R_{C1} \,//\, r_{be2} \qquad \text{4-34}$$

and solving for $G_L = I_{OUT}/I_T$, we have:

$$G_L = -g_{m1}g_{m2}R'_{C1}\,\frac{R'_L}{1 + R'_L g_{m1}}\,\frac{1}{(1 + sR'_{C1}C_T)\left(1 + sC_{be1}\dfrac{R'_L}{1 + R'_L\ g_{m1}}\right)} \qquad \text{4-35}$$

The open loop transfer function has a dominant pole at time constant:

$$\tau_1 = R'_{C1}C_T \cong R'_{C1}C_{be2} \qquad \text{4-36}$$

since C_{bc1} and C_{bc2} are much smaller than C_{be2}. Figure 4-16 shows the root lows plot of G_L as the

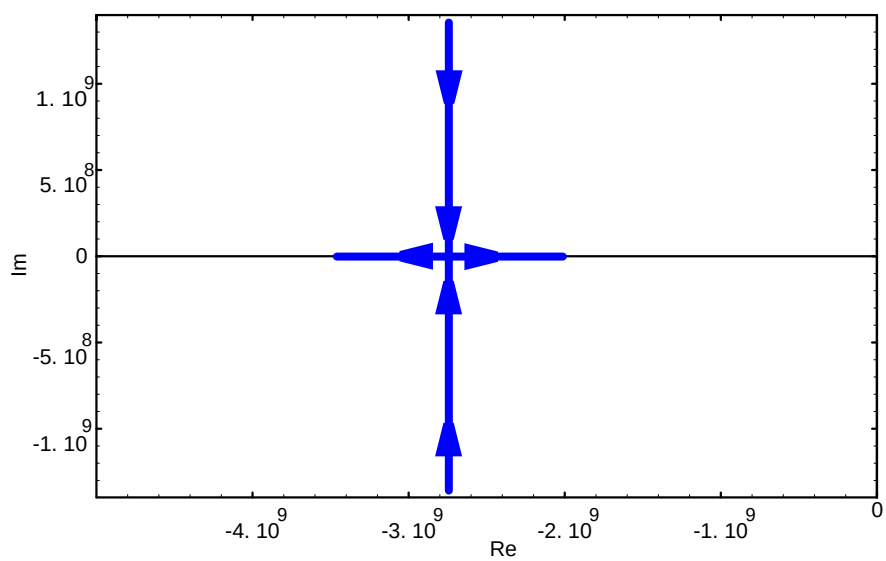


Figure 4-16. Root locus plot of the open loop gain of the White follower varying the capacitance C_{be2}. The poles become real for C_{be2} = 6.5 pF, requiring an additional capacitance of 1.5 pF in addition to the internal capacitance of T_2.

parameter C_{be2} is changed. It can be seen that the poles of the closed loop transfer function could become complex conjugate, or the circuit could even become unstable once the higher order poles

are taken into account. On the other hand, reducing R_{C1} (and R'_{C1}) to reduce the loop gain is not very effective since also the dominant pole is moved to higher frequency.

To effectively reduce the frequency of the dominant pole is best to increase C_{be2}, or, as it has been done, to add a capacitance between collector and base of T_2.

4.4.1 Equivalent Noise Current Simulation

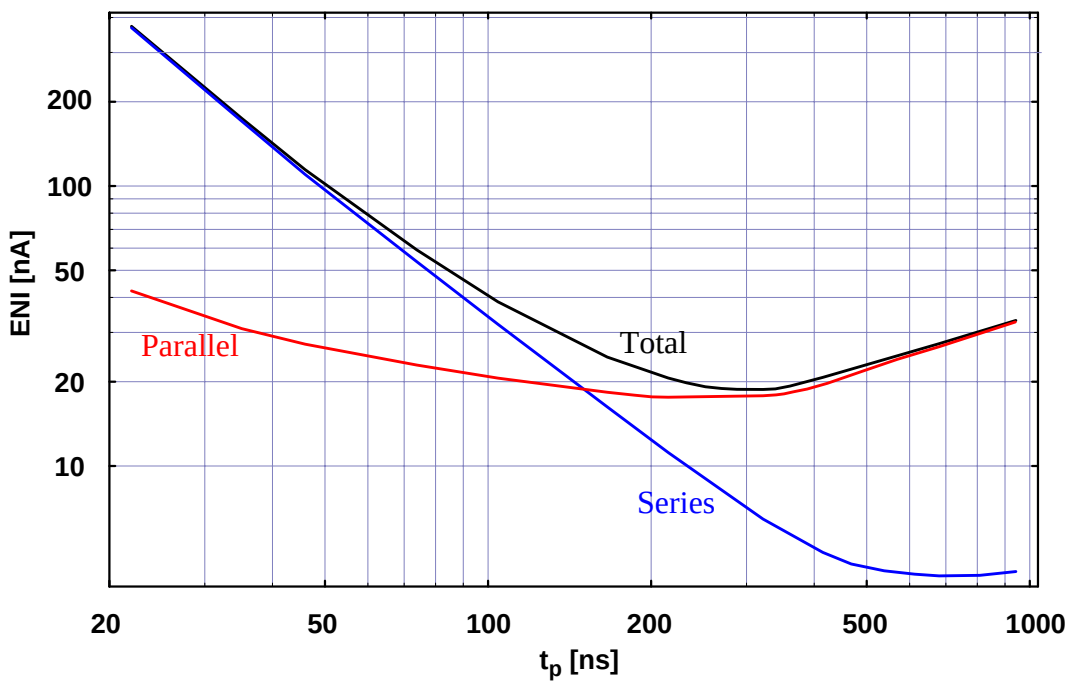


Figure 4-17. SPICE simulated ENI for the circuit of Figure 4-14 with t_d = 16 ns and C_D = 1.5 nF. The transmission line is supposed ideal and β = 100, the worst case value.

The SPICE simulated equivalent noise current (ENI) is shown in Figure 4-17 for the circuit of Figure 4-14, in good agreement with the ENI values expected from the calculation presented in Chapter 2.

4.5 Performance of the Line Terminating Preamplifier

4.5.1 Advantages of the New Configuration

Figure 4-18 shows the full circuit schematic.

The major advantage of the proposed configuration is that the functions of providing low noise and high dynamic range are separated and assigned to different transistors. The pair of input transistors (Q_2 and Q'_2, corresponding to T2, T2' in Figure 4-14, connected in parallel to reduce the base spreading resistance) operate at high current (~ 7 mA) for low noise, but from a low supply voltage (3 V) and, therefore, has modest dissipation. Q_1, which absorbs the input current, has a low dc bias current (~ 1 mA). Even with high collector voltage its dissipation is moderately low.

The loop gain of the input stage is about 33. Variations of the input impedance with signal current (due both to a change in the $1/g_{m1}$ term and the gain G in Equation 4-23 are now reduced to about $\Delta Z_{IN} = 0.6\ \Omega$ or 2.4% for $Z_{IN} = 25\ \Omega$ and an input current of 5 mA. In the previous configuration, the resistance change with signal was about 4.5 Ω or 18%.

A slight noise improvement, with respect to the previous circuit has been measured. This is partly due to the fact that the bias resistor defining the current in T_1 is now larger (4 kΩ, because of the lower DC current) and also to the lower series noise achieved by increasing the bias current of the input transistor pair. Further noise reduction might be possible by monolithic integration of the circuit. Fast, low noise bipolar processes which have a V_{CEO} voltage typically less than 5-6 V are now usable. The size of the input transistor could, therefore, be increased, thus decreasing the net value of $r_{bb'}$ To benefit from such a reduction, the value of R_1 must also be decreased.

4.5.2 Design Requirements

The warm preamplifier requirements and specifications are described in detail in the Atlas Liquid Argon Technical Design Report [16, Sec. 10, 401-410].

The preamplifiers are the first amplification stage in the LAr readout architecture, which set the noise performance of the calorimeter. They amplify the analog signal generated at the calorimeter electrodes. As the signal duration is long compared to the shaping time, a current preamplifi-

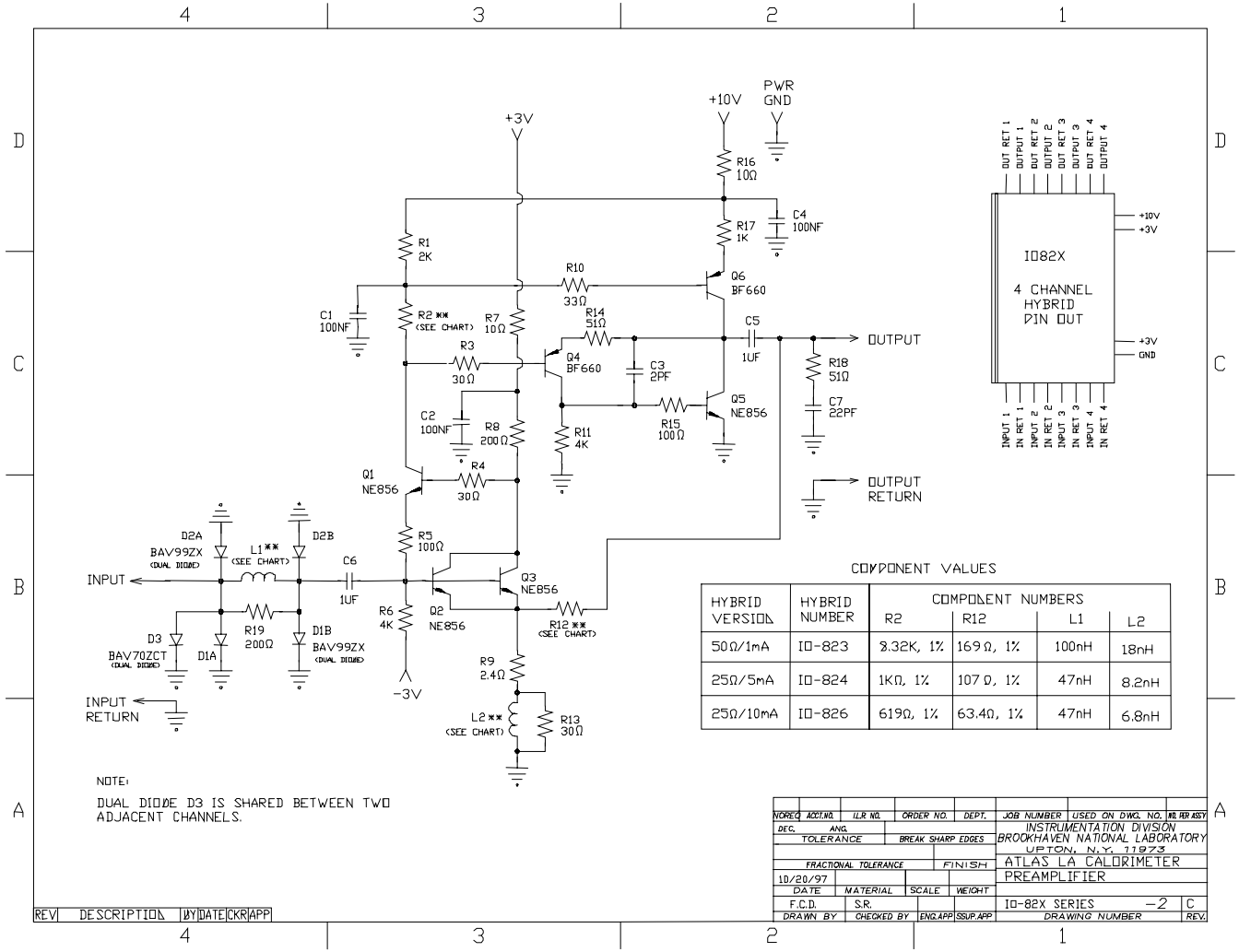


Figure 4-18. Circuit schematic of the IO82x series of preamplifiers.

ers which provide a voltage output directly proportional to the input current has been chosen as explained in Chapter 2.

More than one type of preamplifier is needed to achieve an optimum performance. The detector capacitance, the maximum energy deposited per readout tower as a function of rapidity, together with the need of a maximum output signal of about 3-4 V, determine how many preamplifier types are needed.

Table 4-1 identifies what type and how many preamplifiers are needed for each calorimeter

Table 4-1 Types and quantities of the preamplifiers needed in the ATLAS calorimeters.

Type	**Cal. Section**	**C_D [pF]**	**I_{max} [mA]**	**Z_{in} [Ω]**	**Transimp. [Ω]**	**No. of channels (*)**
IO823	Front & Presampler	160 - 500	1	50	3 k	94336
IO824	Middle & Back (low current)	300 - 2000	5	25	1 k	43904
IO826	Middle & Back (high current)	400 - 2000	10	25	500	35608
IO824	Forward Calorimeter FCAL	300 - 2000	5	25	1 k	4992

*. The number of hybrids is equal to the number of channels divided by four.

section. It summarizes the capacitance (C_D); the maximum currents (I_{max}) estimated for the various detector sections, as well the input impedance (Z_{IN}) and the transimpedance of the preamplifiers. Three preamplifier types will be needed in the experiment. They are identified with the drawing numbers, IO823, IO824 and IO826, or with their Z_{in}, I_{max} combination.

The most important requirements can be summarized as follow:

- Noise: as low as possible with respect to pile-up.
  R_{noise} = 10 Ω
  ENI (typical values) see Table 4-2.
- Uniformity: TDR: < 5% in amplitude for trigger sums.
  TDR: < +/- 2 ns timing

Table 4-2 Noise specifications for the Atlas preamplifiers

Type	ENI [nA]
IO823	< 65 @ C_D = 400 pF, t_p = 40 ns
IO824 IO826	< 270 @ C_D = 2200 pF, t_p = 40 ns
IO824 IO826	< 150 @ CD = 1500 pF, t_p = 40 ns

- Power Dissipation: TDR: < 100 mW/ch
- Environment: must tolerate
  - γ-rays: 20 Gy/year (2 krad/year)
  - neutrons: 10^{12} n/cm^2/year
- Reliability: < 0.5% missing channels per year
- ESD discharge: must withstand 4 mJ multiple discharge without damage (i.e. 2 kV on 2 nF typical)
- Stability: must be stable even in the presence of faults in the signal chain (short, open)
- Output impedance: must be able to drive a 50 Ω load (i.e. the shaper input impedance)
- Dynamic range: up to 10 mA, depending on rapidity range

4.5.3 Experimental Characterization

Results of the experimental characterization, quality assurance and production statistics have been reported in [61, 68]

Signal

Figure 4-19 a,b show the preamplifier and shaper response to the liquid argon signal (a triangular current pulse with a duration t_d = 400 ns and initial current I_0 = 1 mA) of the preamplifier with Z_{in} = 50 Ω. The preamplifier rise time (10% to 90%) is about 45 ns, dominated by the input time

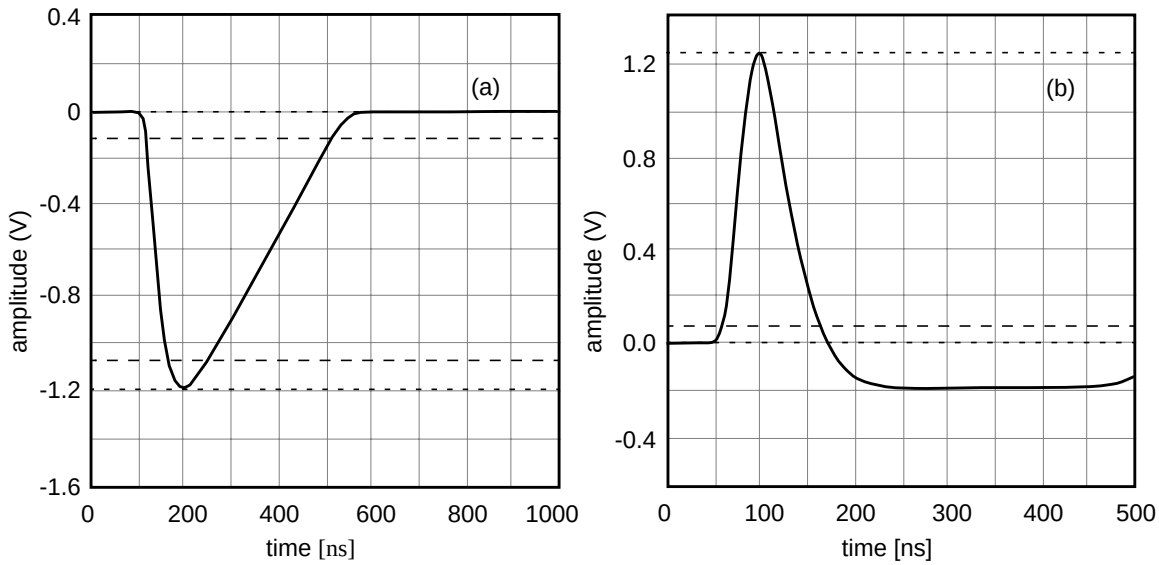


Figure 4-19. Preamplifier response (a) and shaper response (b) for a LAr type triangular current pulse of duration t_d = 400 ns. The other parameters are: I_0 = 1 mA, C_d = 400 pF, Z_{in} = 50 Ω, T_{line} = 77 K. The 10%-90% rise time is about 45 ns. The shaper response is for a CR-RC^2 filter with a 40 ns peaking time (5%-100%) for a LAr excitation.

constant $\tau_{in} = C_D \times Z_0$ = 400 pF × 50 Ω = 20 ns. The shaper is a CR - RC^2 filter with a time constant τ_{SH} ~ 20 ns. The liquid argon signal peaking time is about 40 ns (5% to 100%).

Linearity

The integral non-linearity is defined as the maximum deviation of the peak voltage after shaping with respect to a best fit line, normalized to the maximum amplitude (peak voltage at the maximum dynamic range), namely:

$$\mathrm{INL} = \frac{V_p - \mathrm{fit}}{V_p\big|_{max}} \qquad 4\text{-}37$$

The worst case condition is for the case of C_D = 0, since due to the absence of the input time constant Z_0 C_D, the signal will be faster and any slew rate effect will be magnified. Possible non-linearity effects will be more severe for the Z_{1N} = 25 Ω preamplifier since the change of the

first term in Equation 4-22 over the dynamic range will be proportionally larger and is shown in Figure 4-20.

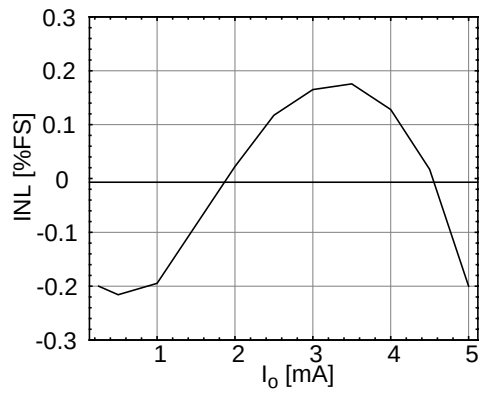


Figure 4-20. Integral non-linearity of the line terminating preamplifier over the full dynamic range for the 25 Ω, 5 mA preamplifier. The measured value is ± 0.2%.

The non-linearity has also been measured with a detector capacitance C_D = 1.5 nF connected to the preamplifier with a transmission line of t_d = 16 ns electrical length and was found to be less than ± 0.1%, or at the resolution limit of the measurement setup. These very low values of integral non-linearity confirm that the preamplifiers are free of slew-rate or driver saturation problems and that the reflections, due to the change of the input impedance with the signal, are of negligible importance after filtering.

Noise

Figure 4-21 shows the measured series noise spectrum for a IO823 preamplifier. The average value is $e_n = 0.37\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$, in good agreement with the simulation and calculation.

Figure 4-22 shows the measured ENI for a IO824 (25 Ω, 1 mA) with and without a t_d = 16 ns transmission line between detector and preamplifier. The measurement has been performed at room temperature by parralleling two pieces of RG174 50 Ω coaxial line in order to achieve a 25 Ω characteristic impedance. The skin effect resistance is approximately 0.4 Ω at 10 MHz, equivalent to the case of a higher loss line at cryogenic temperature. At C_D = 400 pF the ENI is approximately equal to the case of no cable only at short peaking times, worse at longer peaking

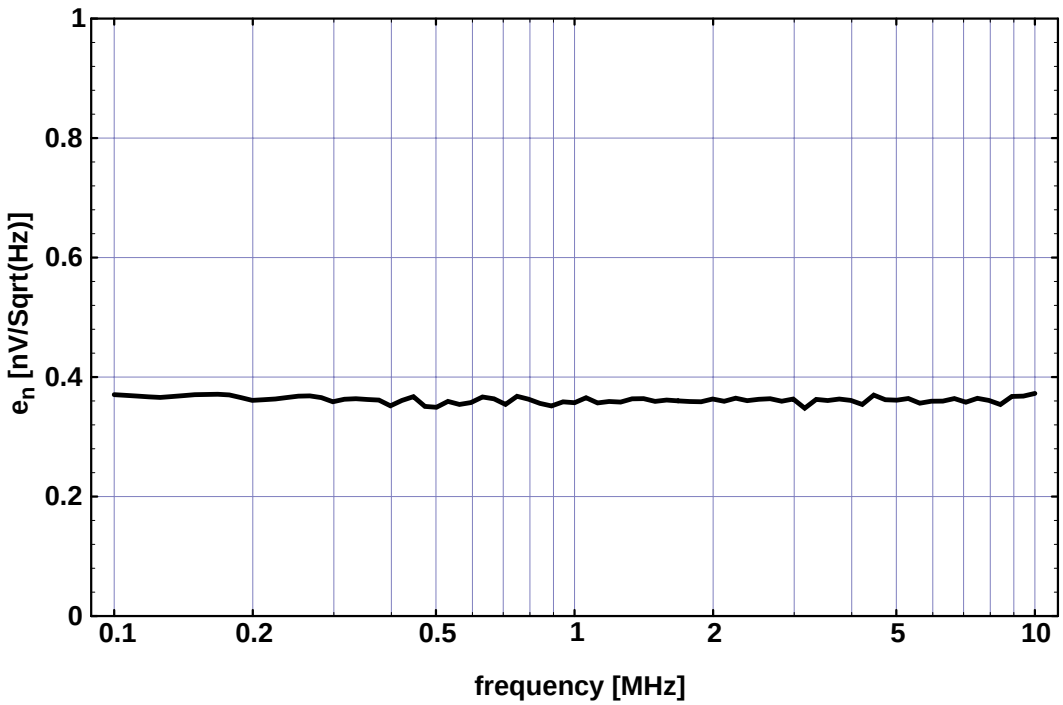


Figure 4-21. Measured series noise spectrum of the IO823 (50 Ω, 1 mA) preamplifier. The average value is 0.37 nV/$\sqrt{\mathrm{Hz}}$.

times. At C_D = 1500 pF the ENI in the case of the 16 ns line is better up to about $t_{pk} \cong 50$ ns, and only slightly worse for longer shaping times.

Figure 4-23 compares the 25 Ω and 50 Ω at C_D = 400 pF and 1500 pF. At low capacitance, the 50 Ω case is always better than the 25 Ω case as explained in Chapter 2. At higher capacitance the 25 Ω case yields a lower ENI up to about t_{pk} = 60 ns, due to the shorter input time constant which yields a larger signal. At longer shaping times, outside the range of the ATLAS calorimeter readout, the 50 Ω case would be again slightly better. The ATLAS collaboration has decided to use a 50 Ω preamplifier and cable for the readout of the low capacitance front section, and 25 Ω preamplifiers for the larger capacitance middle and back sections.

Ionizing Radiation Tolerance

The main mechanism of ionizing radiation damage in semiconductor devices is by positive charges trapped on the surfaces of insulating layers and interfaces. Therefore, bipolar devices are much

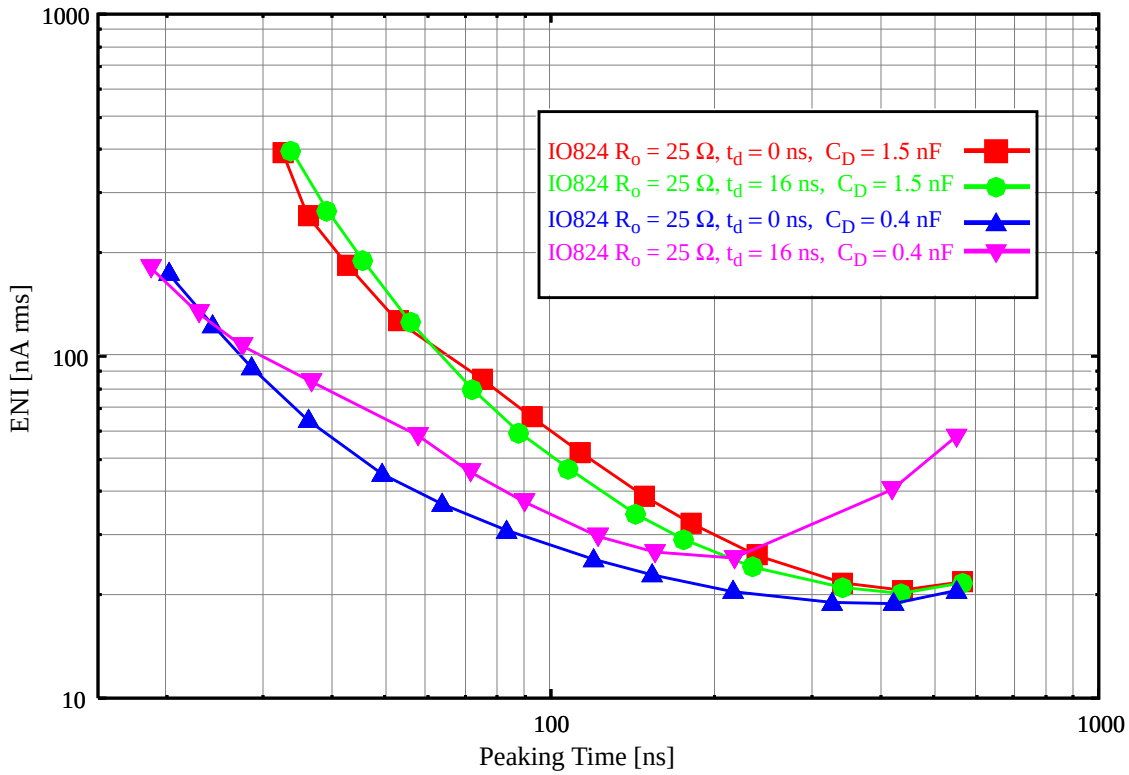


Figure 4-22. Measured ENI with and without a t_d = 16 ns transmission line at two different detector capacitances. The measurement has been performed at room temperature with two RG174 coaxial cables paralled to achieve a 25 Ω characteristic impedance.

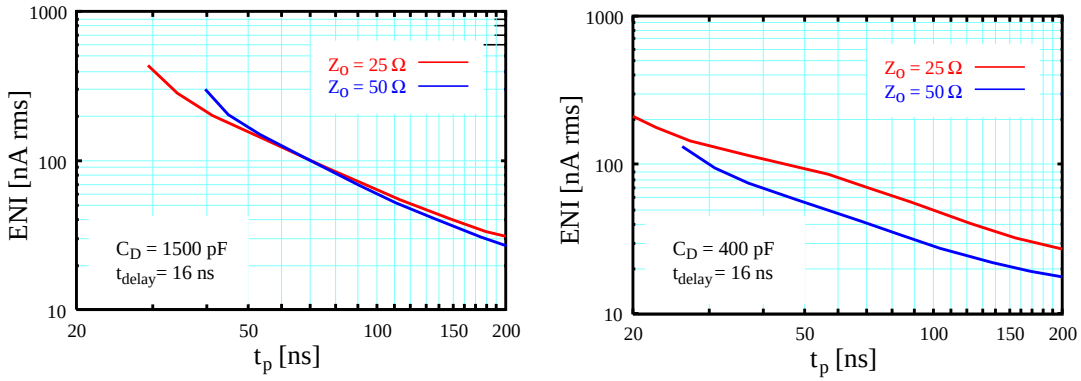


Figure 4-23. Comparison of the 25 Ω and 50 Ω cases at low and higher detector capacitance. The length of the line is t_d = 16 ns.

less sensitive than MOS since they are junction devices which do not depend on a Si-SiO_2 interface for their operation. Trapped charges on BJT surface layers produce an inversion layer which effectively increases the volume where recombination can occur. This results in an increased surface state generation-recombination current that reduces the current gain of the device. The effects are larger at low current levels, since they are mostly surface currents and are, therefore, affected to a larger extent.

Since the extent of the damage for a given dose depends strongly on the quality of the surface (contaminants, broken bonds) and of the oxide, it varies greatly from device to device and there is no general equation based on material properties and device parameters to quantify the relationship of degradation versus dose and dose rate [69]. Degradation of gain due to ionizing radiation is minimized at the collector current levels corresponding to the maximum β region of an unirradiated device [70]

Expected gamma doses over the life of the preamplifiers is estimated to be approximately 200 GY (2×10^4 rad) silicon. It is expected that the total possible dose would be no more than 5 times this number or 10^5 rad. Two hybrid preamplifiers (one each of the 25 Ω and 50 Ω types) under power were exposed to a total of 10^5 rad. Both hybrids were measured for gain, peaking time, ENI, and input impedance before irradiation and after total doses of 5×10^4 and 10^5 rad of ^{60}Co gamma radiation. Gain, peaking time, and ENI changed by less than the measuring error for both hybrids after 10^5 rad. Average input impedance (of 4 channels) at selected doses for the two devices is shown in Table 4-3.

Table 4-3 Input impedance versus γ-dose

	unirradiated	5×10^4 rad ^{60}Co	10^5 rad ^{60}Co
IO823	51.3 Ω	50.1 (2.3% change)	48.8 (4.9% change)
IO824	25.4 Ω	25.3 (0.4% change)	25.2 (0.8% change)

The circuits, are however, fully operational even after total doses in excess of 1 Mrad. At higher doses the device which is most sensitive to radiation damage is the first transistor of the White follower (Q4 in the schematic of Figure 4-18), which is operated at only 200 μA.

Neutron Irradiation Effects

Bipolar devices, as their name implies, operate with both majority and minority carriers, and they therefore exhibit a greater sensitivity to neutrons than their MOS counterparts. The principal damage mechanism by incident neutrons on bipolar devices is the creation of lattice defects which introduce trapping energy states, which cause a reduction of the minority carrier lifetime. This directly affects the current gain β by causing recombination of minority carriers as they are transported through the base into the collector. A second, less important effect is the change in resistivity of the silicon itself, as dopant atoms are inactivated as they are kicked off the lattice. Since the neutron damage changes fundamental properties of the bulk silicon in a predictable way, a quantitative expression that describes the β degradation versus fluence has been developed. This is the well established Messenger-Spratt equation [69]:

$$\Delta\left(\frac{1}{\beta}\right) \equiv \frac{1}{\beta} - \frac{1}{\beta_i} = \frac{\Phi_n}{\omega_T} \cdot K \qquad \text{4-38}$$

where Φ_n is the neutron fluence, ω_T the transition angular frequency and K is the damage constant. From Equation 4-38, it can be seen that fast bipolar transistors are intrinsically neutron hard: their thin base and the field aided transport in the base minimize the majority carrier recombination. For this reason, fast transistors (the NE856 has a $f_T \cong 5$ GHz and the BF660 $f_T \cong 800$ MHZ) have been chosen.

Preamplifier hybrids have been irradiated at the Lowell University neutron irradiation facility, with neutrons of average energy of 1.1 MeV up to a fluence of 2×10^{13} n/cm^2. The Lowell facility is uniquely suited for neutron irradiation device studies, thanks to its very low γ-ray contamination, estimated to less than 1 krad at the 2×10^{13} n/cm^2 fluence.

No changes in gain, peaking time, ENI and input impedance larger than the measurement error (about 0.5%) were measured. Preamplifier hybrids were also irradiated by other members of the ATLAS collaboration at the SARA facility in Grenoble [71] up to a fluence of 1×10^{14} n/cm^2 (1 MeV equivalent). The SARA facility has a non-negligible gamma contamination, so the irradiated hybrids also received a 3.6 kGy (360 krad) total dose. Their results, reported in [58], can

therefore be regarded as “worst case”, closer to a “real life” situation in which the circuits will be subjected to both ionizing radiation and neutrons. The SARA irradiation results for hybrids equipped with fast BJTs, are summarized in Table 4-4.

Table 4-4 Change of measured parameters measured after a 1×10^{14} n/cm^2 neutron fluence and a total dose of 3.6 kGy (360 krad) (from [58]).

Type	Gain	ENI	Z_{IN}
IO823	-7%	No change	-7%
IO824	-3%	No change	-3%

High Voltage Protection

Since the calorimeter requires a drift field established by means of an applied high voltage ($\cong$ 2 kV) across the gap, there is the possibility of discharges into the preamplifier. The specification of the preamplifier require the capability to survive multiple 4 mJ discharges without damage. Since series resistive elements cannot be used to dissipate the discharge energy for noise reasons, protection is achieved by means of diodes which turn “ON” to protect the base-emitter junction of T_2 and a series inductor, which, by presenting a large impedance to a fast impulse, limits the maximum current (see Figure 4-18.). The transistor T_1 is further protected by the 100 Ω resistor in series. The preamplifier has been able to withstand over 1,000 discharges when connected by the minimum length of cable (2 m) with no degradation. A full study of the HV protection is presented in [72].

4.6 Preamplifier Realization

The preamplifiers have been manufactured by means of thick film hybrid technology. This technology is well-known, with predictable time schedule for production and high reliability, as proven in many high-energy physics experiments and applications where high reliability is required. Moreover each device can be chosen to optimize its function (e.g. low noise) and many different

type of devices (NPN, PNP, decoupling capacitors, etc.) are available. The channel density allows for the larger size of the circuit.

Use of a more advanced monolithic technology was rejected because of the higher development costs (a complementary bipolar process featuring low noise, radiation resistant transistors would be necessary) and higher risks associated with the research and development, both in terms of performance and schedule.

The hybrid design has been carried out with very conservative design rules (10 mils line, 10 mils separation) to both expand the pool of manufacturers and to improve the production yield. The layout is shown in Figure 4-29.

The preamplifier characteristics meet and exceed the specifications. Figure 4-24 illustrates peaking time, amplitude and noise distributions for the preamplifiers IO823 (Z_{IN} = 50 Ω, I_{MAX} = 1 mA) and IO824 (Z_{IN} = 25 Ω, I_{MAX} = 5 mA).

All the preamplifier parameters are within +/- 3σ from the average value.

A pre-production run of 97 units (388 channels) of IO823 (Type A) preamplifiers and 84 units (366 channels) of IO824 (Type B) has been burned-in and its performance has been measured and analyzed.

Measurements were performed with the conditions summarized in Table 4-5.

Table 4-5 Experimental conditions for the pre-production tests.

	IO823 (50 Ω, 1 mA)	IO824 (25 Ω, 5 mA)
Detector Capacitance (C_d)	330 pF	1.5 nF
Cable Length (ns)	16	19
Cable Type	RG174 (Z_0 = 50 Ω)	2 x RG174 in parallel (Z_0 = 25 Ω)

On a different production run also the input impedance has been measured and characterized on 50 preamplifiers (200 channels) each of IO823, IO824 and IO826 preamplifiers.

The parameters measured are (see Table 4-6, 4-7) are:

- Gain
- Peaking time
- Noise
- Input Impedance

Table 4-6 IO823 - 50 Ω, 1 mA

Parameter	Average	Tolerance	rms	% within +/-3 σ
Gain	981.8 mV	+/-1.13%	3	99%
Peaking Time	45.8 ns	+/-0.34 ns (+/- 0.7%)	0.14 ns	100%
ENI	49.3 nA	+/-3%	0.54 nA	99.2%
Z_{IN}	51.4 Ω	+/-2.9%	0.6 Ω	100%

Table 4-7 IO824 - 25 Ω, 1 mA

Parameter	Average	Tolerance	rms	% within +/-3 σ
Gain	612 mV	+/- 1.5%	3.3 mV	100%
Peaking Time	52.6 ns	+/- 0.7 ns (+/- 1.3%)	0.3 ns	100%
ENI	124 nA	+/- 1.9%	0.8 nA	100%
Z_{IN}	25.8 Ω	+/- 1.8%	0.17 Ω	100%

The histograms of the distributions are presented in Figure 4-24.

4.6.1 Burn-in Study

The first series of hybrids produced (200 units), after being tested for electrical functionality, was subjected to 168 hours of an environmental stress screening (or burn-in) at ambient temperature to identify and eliminate deficiencies and early failures. Moreover few hybrids (eight units randomly chosen) were fully characterized in term of gain, peaking time and noise before and after burn-in to detect any possible variation of performances due to ageing effects.

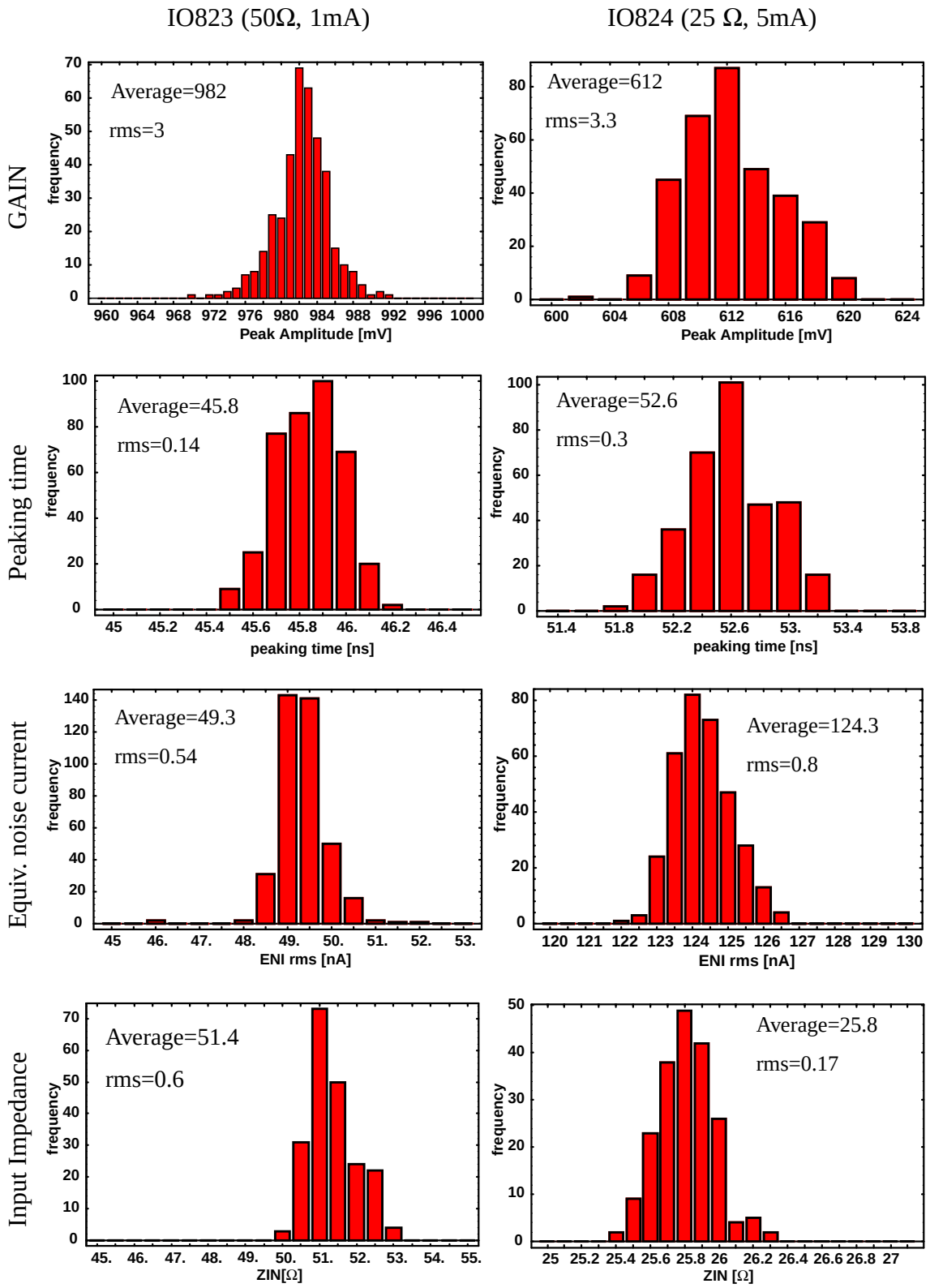


Figure 4-24. Production statistics of important parameters of the IO823 and IO824 preamplifiers.

At the conclusion of the burn-in only one channel failed to meet specification. The unit failed because a PNP transistor (Q4) in the white follower broke during burn-in. After replacing the transistor the channel was tested again and it met all specifications.

The hybrids that were fully characterized before burn-in did not show any performance variation due to the environmental stress.

The burn-in results brought to the conclusion that the environmental conditions adopted for the test were not sufficient to rule out all the early failure mechanisms. A more extensive burn-in study was adopted for the batch of hybrids produced for the first full module of the calorimeter. The temperature was elevated to ~ 70 ^{o}C and the time were extended up to 432 hours. The combination of elevated temperature and extended time did not increase the number of failures. The only source of failures for thick-film hybrids was a cold solder joint.

Under the assumption that the same failure mechanism will be the only ones in the full production of the ATLAS hybrids, was concluded that a burn-in of 168 hours at an elevated temperature of 70-80 ^{o}C, will be used to eliminate all causes of infant mortality. A higher burn-in temperature/shorter time is not achievable because some of the components used in the preamplifiers are not rated for temperatures higher than 100 ^{o}C, namely the inductors.

4.6.2 Reliability Evaluation

The reliability of the hybrids has been evaluated based on the internationally recognized method of calculating electronic equipment reliability given in “Military Handbook MIL-HDBK-217”, published by the US Department of Defense. This standard uses a series of models for various categories of electronic components to predict failure rates that are affected by environmental conditions, quality levels, stress conditions and various other parameters. These models are fully detailed in MIL-HDBK-217. Most of the models in MIL-HDBK-217 use ten or more parameters for the calculation of the component failure rate. Commercially available programs, such as “Milstress” from ITEM software have been written to facilitate the calculation of failure rates and it was used for this study.

The TDR specification for channel failure rate is “0.5% missing channels per year” or “868 missing channels per year”. If the worst case condition is taken, i.e. one channel missing means a full hybrid missing, the maximum tolerable failure rate per hybrid is “217 missing hybrids per year” or 0.57 frmh (where frmh stands for failure per million hours of operation) or 1.75 10^6 hours “mean time between failure” (MTBF). The technology/component/design adopted for the hybrids has to be evaluated against this benchmark.

The reliability prediction presented in this section is for guidance, the purpose of this calculation is to establish, by means of a consistent and uniform method, the reliability of what has to be considered a “mature design”. The calculation is based on the two methods known as “Part Count” and “Part Stress Analysis” and the following assumptions have been made:

- Most of the details used in the project are known, in term of material and components.
- In a hybrid package, resistors and inductors are considered to contribute insignificantly to the overall hybrid failure rate and for this reason are assumed to have a failure rate of zero.
- The hybrid temperature has been assumed to be known and equal to 30 ^{o}C.
- The power dissipation of each hybrid component has been estimated from an actual hybrid sample and from design analysis. It has been compared with the maximum power from the component data sheet to obtain the “stress factor” for each individual hybrid component. The stress factor has been always rounded up to the second figure.
- The hybrid quality has been chosen equal to “class B microelectronic” as defined in Mil883-C screening procedure method 5004.9, namely an electronic apparatus not subject to vibrations.
- The quality of the individual components used for the manufacturing has been set to “industrial grade, RE”.

The environment has been set to “ground benign”, that is the condition of electronic equipment which is in a fixed position at ground level. Based on this information a failure rate of

0.48 frmh or 2×10^6 hours MTBF has been calculated. This result shows that the solution adopted has a predicted reliability similar to the one requested by ATLAS TDR.

Figure 4-25 shows the significant component failure rates of a hybrid. The transistor Q5 (the

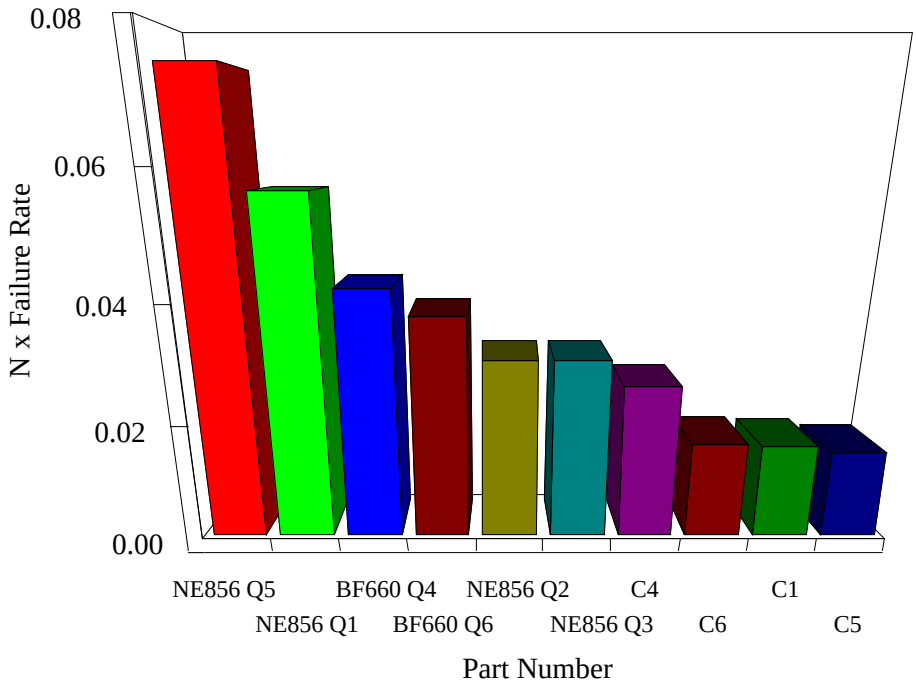


Figure 4-25. Failure rates of the most significant components.

NPN NE856 used in the white follower) is the single largest contributor to the hybrid failure rate because of its large V_{CE} which increases the "stress factor" of the devices.

The failure rate is also temperature dependent as shown in Table 4-8.

Table 4-8 Failure as a function of temperature

Temperature (^oC)	**frmh**
20	0.44
30	0.48
40	0.59
50	0.70
60	0.76
70	0.93

Highly Accelerated Life Tests

As an aid in testing the reliability and design limits of the preamplifier a Highly Accelerated Life Test (HALT) of a selected group of preamplifiers was performed at a Qualmark Corporation facility in Marlborough, Massachusetts. The purpose of these tests was to induce failures in a non-destructive way so as to expose weaknesses in design or manufacture. This information then can be used to improve the devices and to select the manufacturing processes used in producing the devices.

Twelve preamplifiers, six IO823 (50 Ω, 1 mA) and six IO824 (25 Ω, 5 mA), were mounted on a board with power and signal input/output lines so that the response could be monitored during the test. The board with the mounted preamplifiers was inserted in a computer controlled environmental chamber and tightened to a "platform" which can be vibrated by simultaneous triaxial shakers in a frequency range of 0 to 2 kHz.

The testing process was divided into 3 stages. The initial stage consisted of varying the temperature of the preamplifiers, first gradually and then in rapid temperature cycling (between - 100 ˚C and 100 ˚C). The second stage involved accelerating the preamplifiers at a fixed temperature (30 ˚C) starting at 5 Grms (Gravities root mean square) and increasing the acceleration in steps of 5 Grms up to a maximum of 50 Grms. In the final stage, both acceleration and rapid thermal cycling were combined.

The only preamplifier failure during the test was observed after many thermal cycles and at a vibration ~ 50 Grms, where all four channels of one hybrid became intermittent. The failure was caused by the failure of the + 3 V power pin. The edge pin solder joint broke due to the "fatigue" accumulated in the test.

At the conclusion of the test the pin was replaced and the hybrid was found working within specifications.

A visual inspection identified that some of the hybrid power pins (the four pins on the longest side of the hybrid) were not centred into the pad and they were soldered at an angle with respect of the ceramic substrate.

The pins, the last components to be assembled, were hand-soldered in place. The pin assembly is the least automated part of the manufacturing process. A more stringent inspection will be required for the final production.

Appendix A: Impedance on the Emitter of T_2

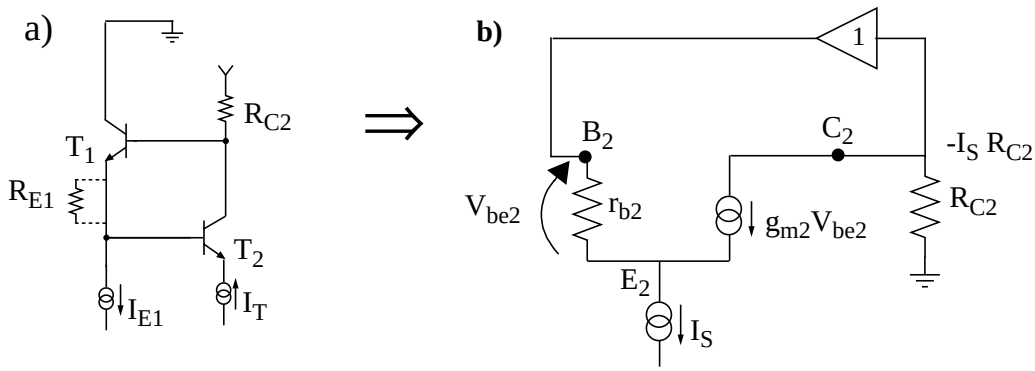


Figure 4-26. Equivalent circuit for the calculation of the impedance seen into the emitter of T_2 of the inner loop circuit. This impedance, approximately equal to R_{C2} ($\cong$ 200 Ω) is high with respect of the value of R_1 of the outer loop feedback network.

This appendix will show that the loading effect of the impedance seen into the emitter of T_2 on the feedback network of the outer loop (R_1, R_2 in Figure 4-2) can be disregarded in first approximation.

With reference to Figure 4-26 and disregarding R_{E1}, we can write:

$$\begin{aligned} V_{be2} &= V_{C2} - V_{E2} \\ V_{C2} &= -g_{m2}V_{be2}R_{C2} \end{aligned} \qquad \text{4-39}$$

Assuming $\beta 2 \rightarrow \infty$, so that the base current can be disregarded, we have:

$$I_S = g_{m2}(V_{C2} - V_{E2}) = -g_{m2}R_{C2}I_S - V_{E2}g_{m2} \qquad \text{4-40}$$

so that, by rearranging terms, we have:

$$Z_{E2} = -\frac{V_{E2}}{I_S} = \frac{1}{g_{m2}} + R_{C2} \cong R_{C2} \qquad \text{4-41}$$

The error due to the presence of the resistor R_{E1} is less than 1%.

This calculation shows that the emitter of T_2 is a high impedance point ($R_{C2} \cong 200$ Ω) with respect of the resistor $R_1 = 2.4$ Ω in the feedback voltage divider, so that its loading effect can be disregarded.

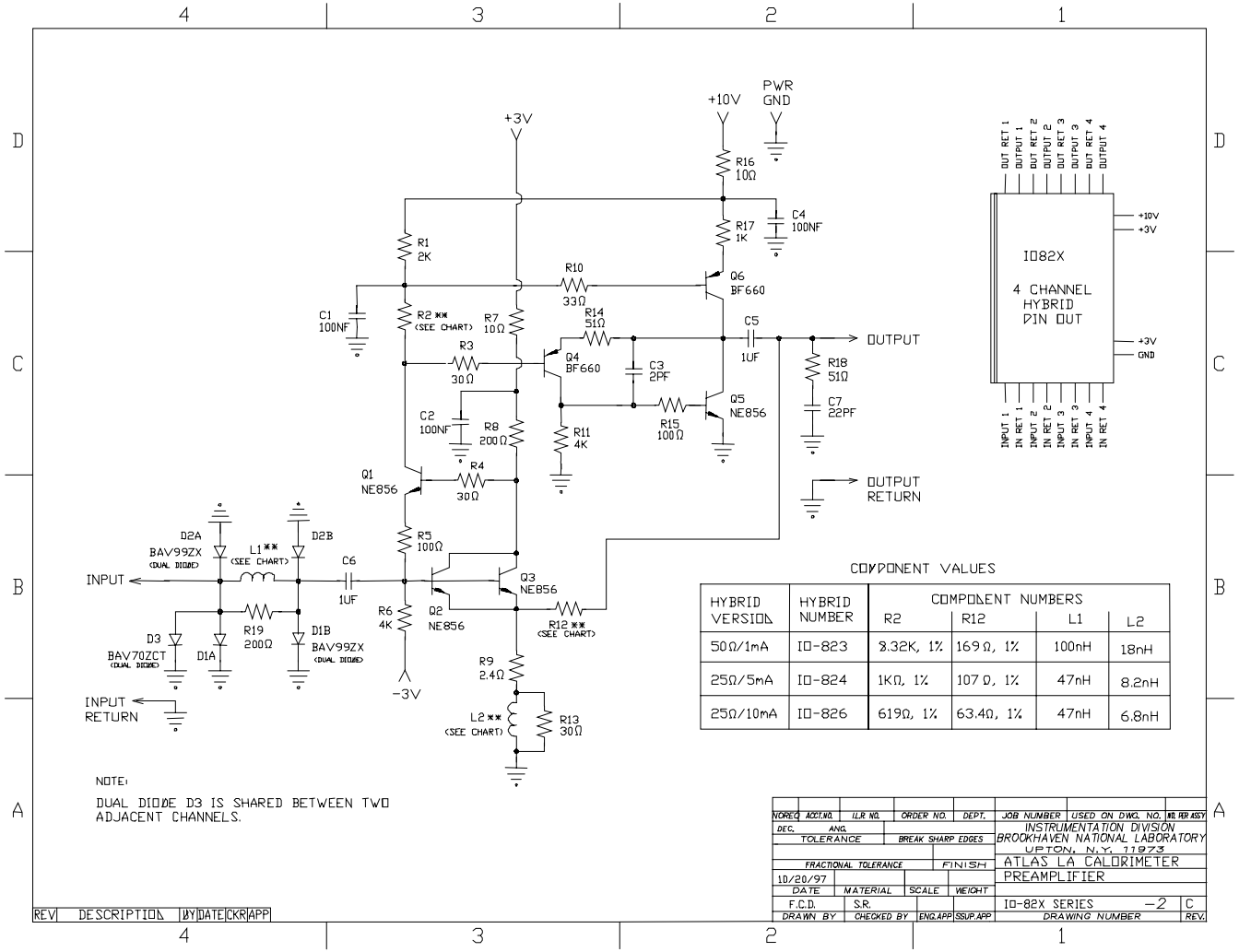


Figure 4-27. Circuit schematic of the IO82x series of preamplifiers.

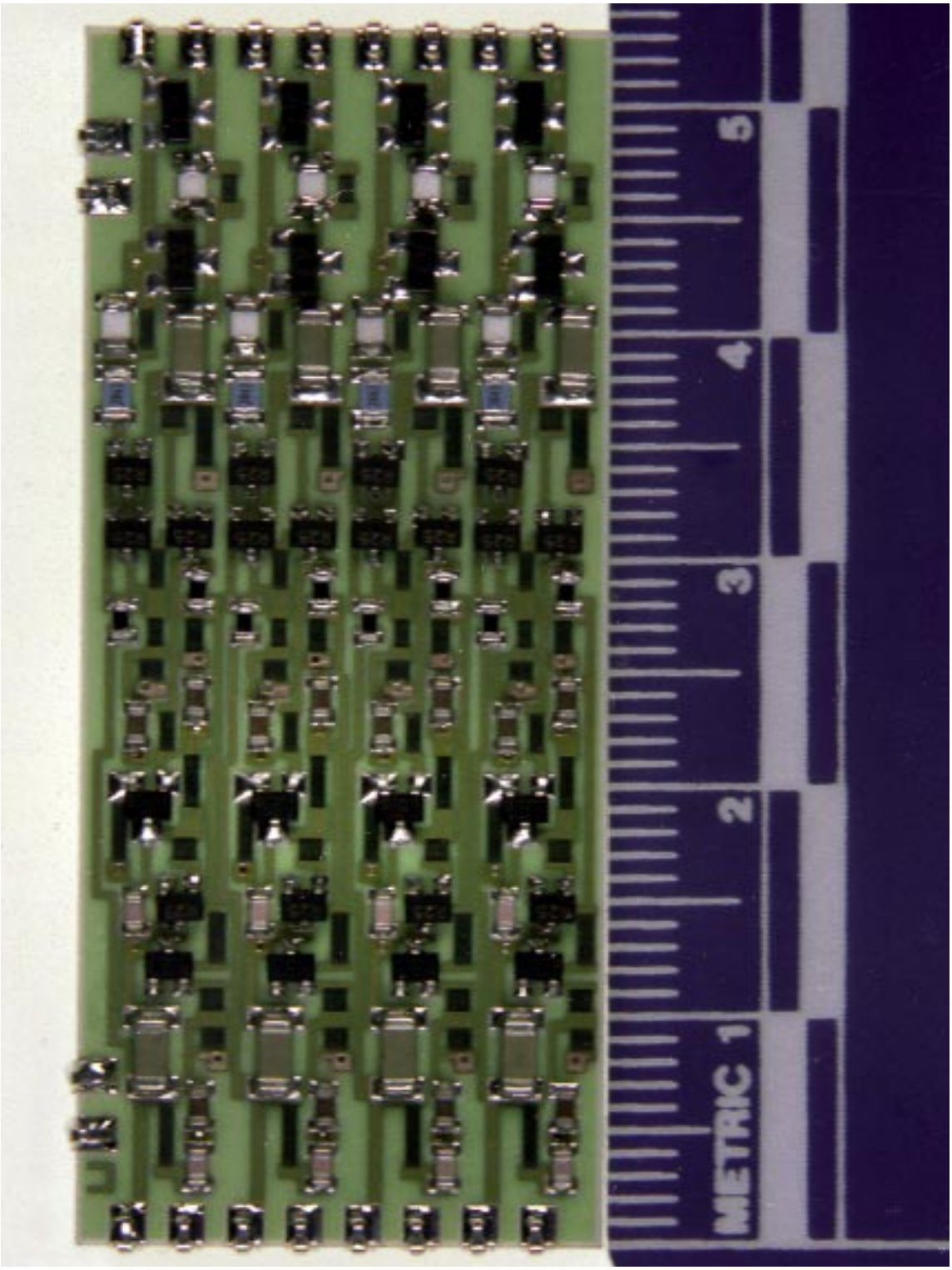


Figure 4-28. Photograph of the IO823 preamplifier.

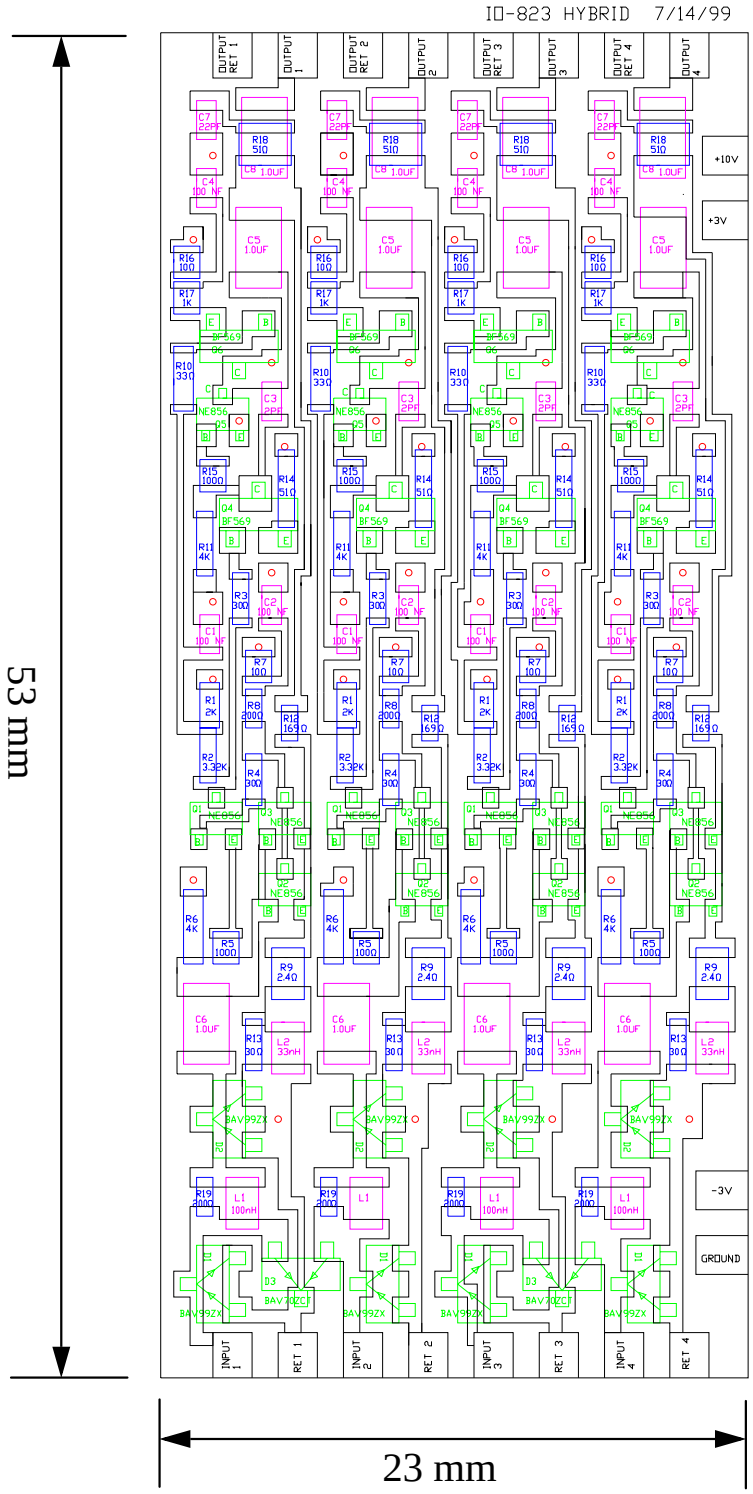


Figure 4-29. Layout of the IO82x series of ceramic hybrid modules. The one shown is the IO823. The other versions differ only for the component values.

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