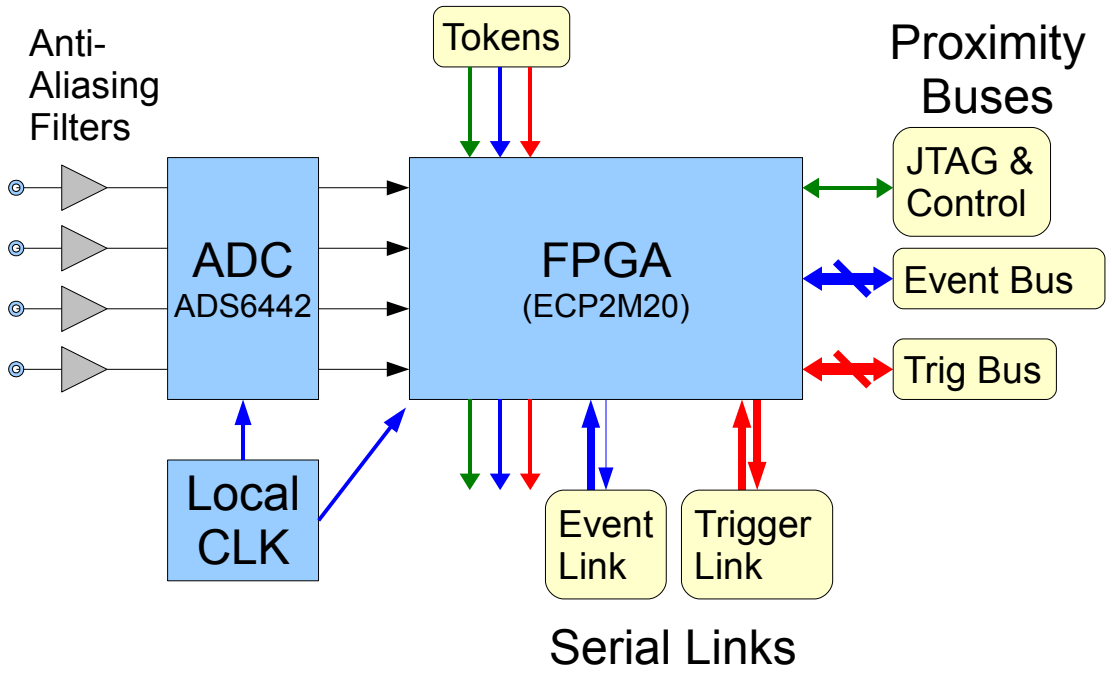
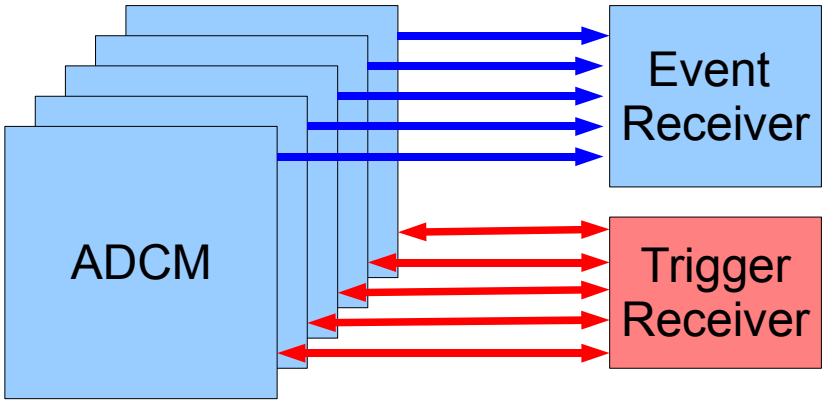
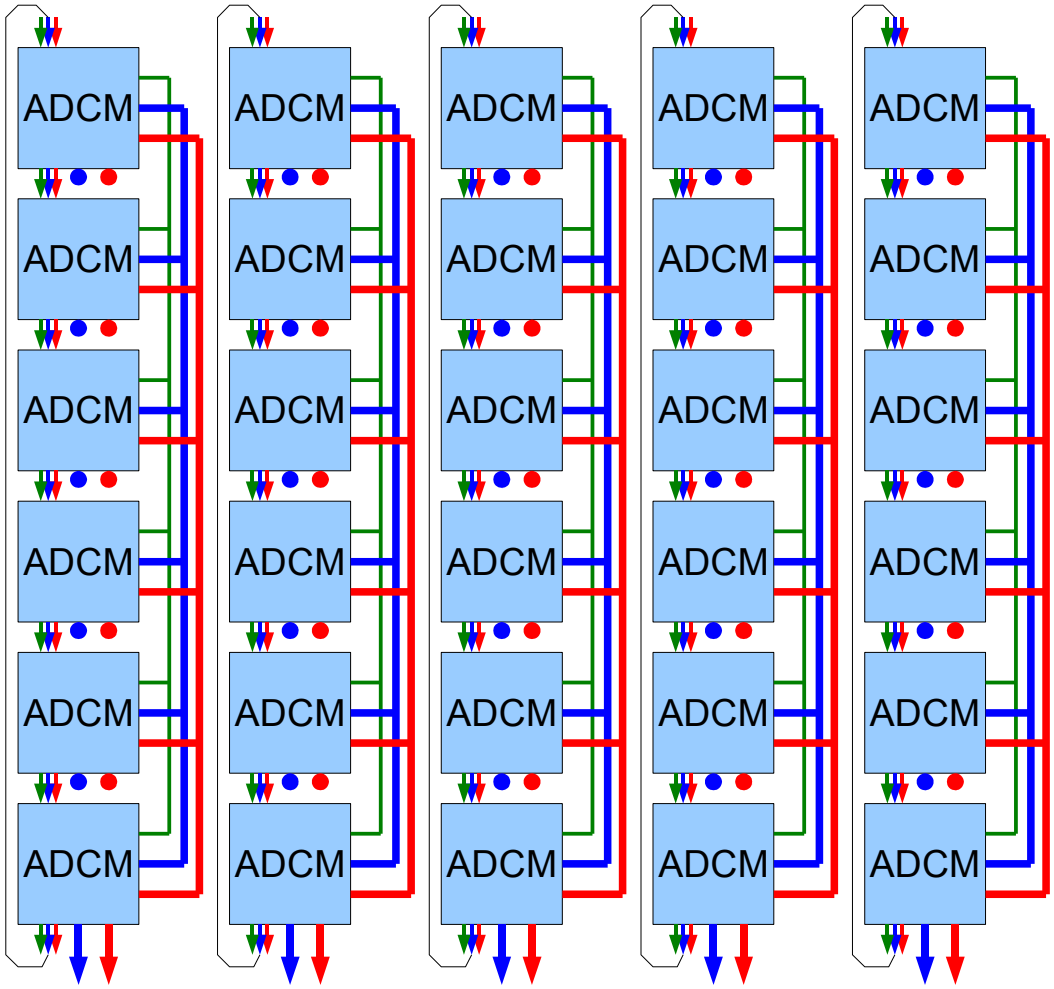
2x2 Module With Serial/Parallel Links




ADCM
Event
Receiver
Trigger
Receiver

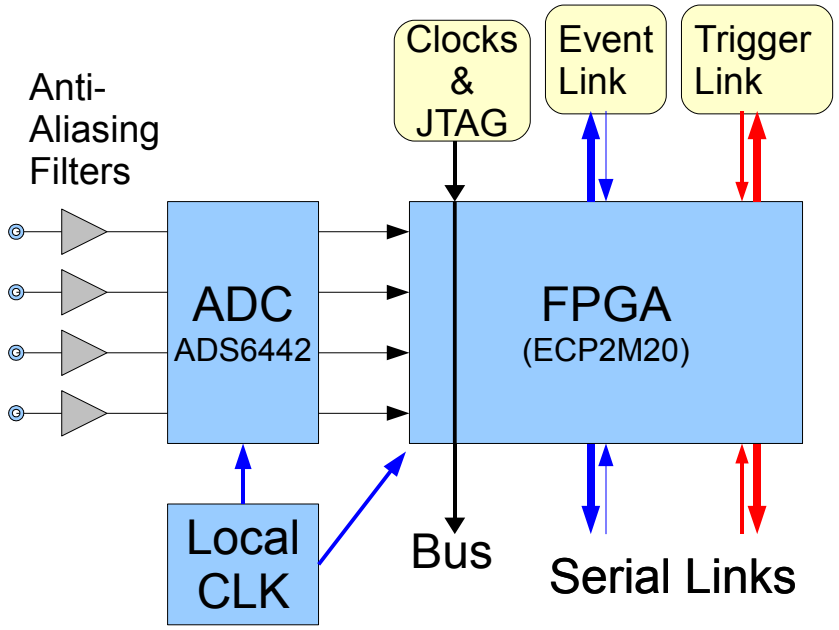
Supermodule with Parallel Interconnections

Trigger bus and event bus running through joined ADCMs, The combined bus width is ~20 pairs running DDR at 40 MHz.
Separate token passing ring (3lines) for daisy chaining trigger, event and JTAG.



Serial Links to Trigger and Event Receivers

2x2 Module With Serial Links



Supermodule with Serial Interconnections

Each ADCM has two input serial links (SERDES) and two output serial links, they are trigger (red) and data (blue). Each ADCM has two cable connections to its neighbors, 8 pairs for 2 SERDES links, 1 low speed pair for JTAG TDI/TDO and 5 pass-through pairs for clocks, and JTAG.

Serial Links to Trigger and Event Receivers

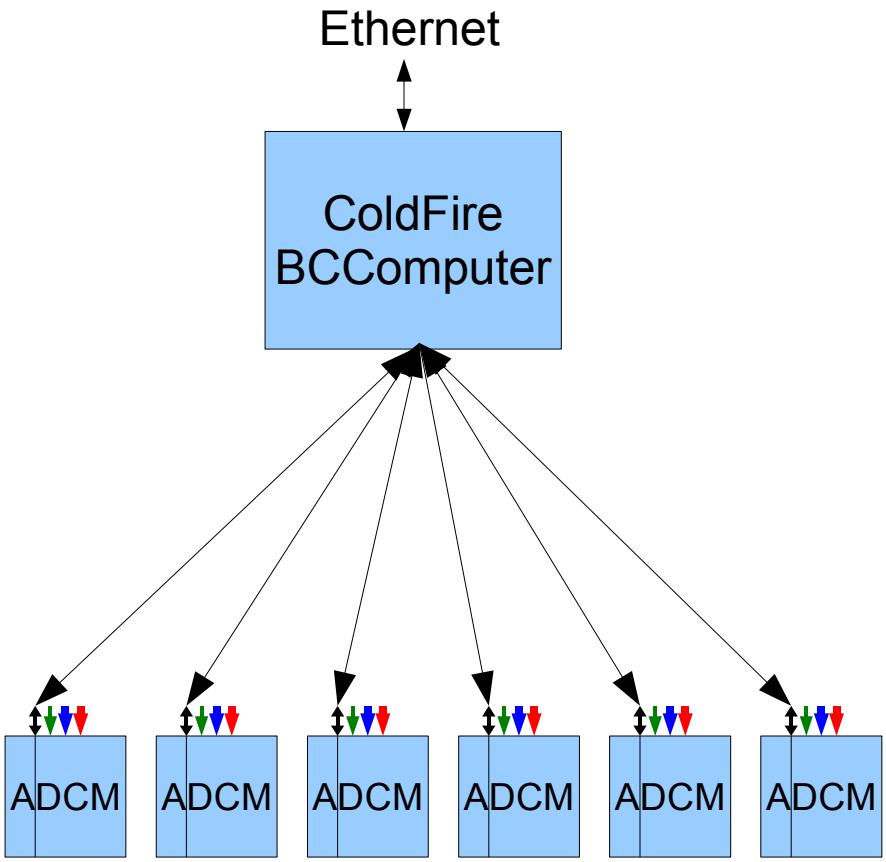
Rates

Data Transfer Rate	
ADC Sampling Rate, [MSPS]	50
Number of Channels	4
ADC Precision, bits	14
8b/10b Encoding, bits	17.5
Number of Samples	8
Data Collection Time [us]	20
Concentration Factor	6
Data Transfer Rate, Mbps	**168**

Buffer Size	
Buffering Time, [us]	4
Required Buffer Size [Kbits]	**11.2**

Trigger Transfer Rate	
Crossing Rate [MHz]	10
Number of Trigger Words	1
Bits per Word	8
8b/10b encoding	10
Concentration Factor	6
Trigger Transfer Rate, [Mbps	**600**

Lattice ECP2M20E-6F256C	
Embedded Memory [Kbits]	1217
sysDSP Blocks	6
18x18 Mutipliers	24
SERDES 250 to 3125 Mbps	4

JTAG-based Control and Testing

The JTAG and control is done using N3C system, developed for NCC
It provides JTAG configuration, online monitoring and test data taking (200KBytes/s).