Test of SRCV40_6

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Sensors are not connected.
SVX4 installed U1 and U4.

Initial power consumption: 5.0V, 0.395A

```
<< upload s jtag/spxfem_v23_tested.stapl
>> File replaced.
<< splay s xRUN_XILINX_PROC
>> JTAG playing file.
Successful File Execution.
success
JAM player returned 00000000 line 0000 code 00000000
>> JTAG finished playing file.
```

Power consumption after configuring FPGA: 5.0V, 0.570A

```
<< upload v jtag/ped.fem
>> File replaced.
<< jsvx v
<< jsvx v
Triggers could be generated using 'jusr t' command
loaded 769c8(180)
1000000100000001000000010000000100000001000000010000000100000001
0000000100000001000000010000000100000001000000010000000100000001
0000010001010101100000000000111101100000000111111111000000001000
0000000100000001000000010000000100000001000000010000000100000001
0000000100000001000000010000000100000001000000010000000100000001
0100000001010101100000000000111111110010001100000001100000001000
```

Generation of 1024 test events

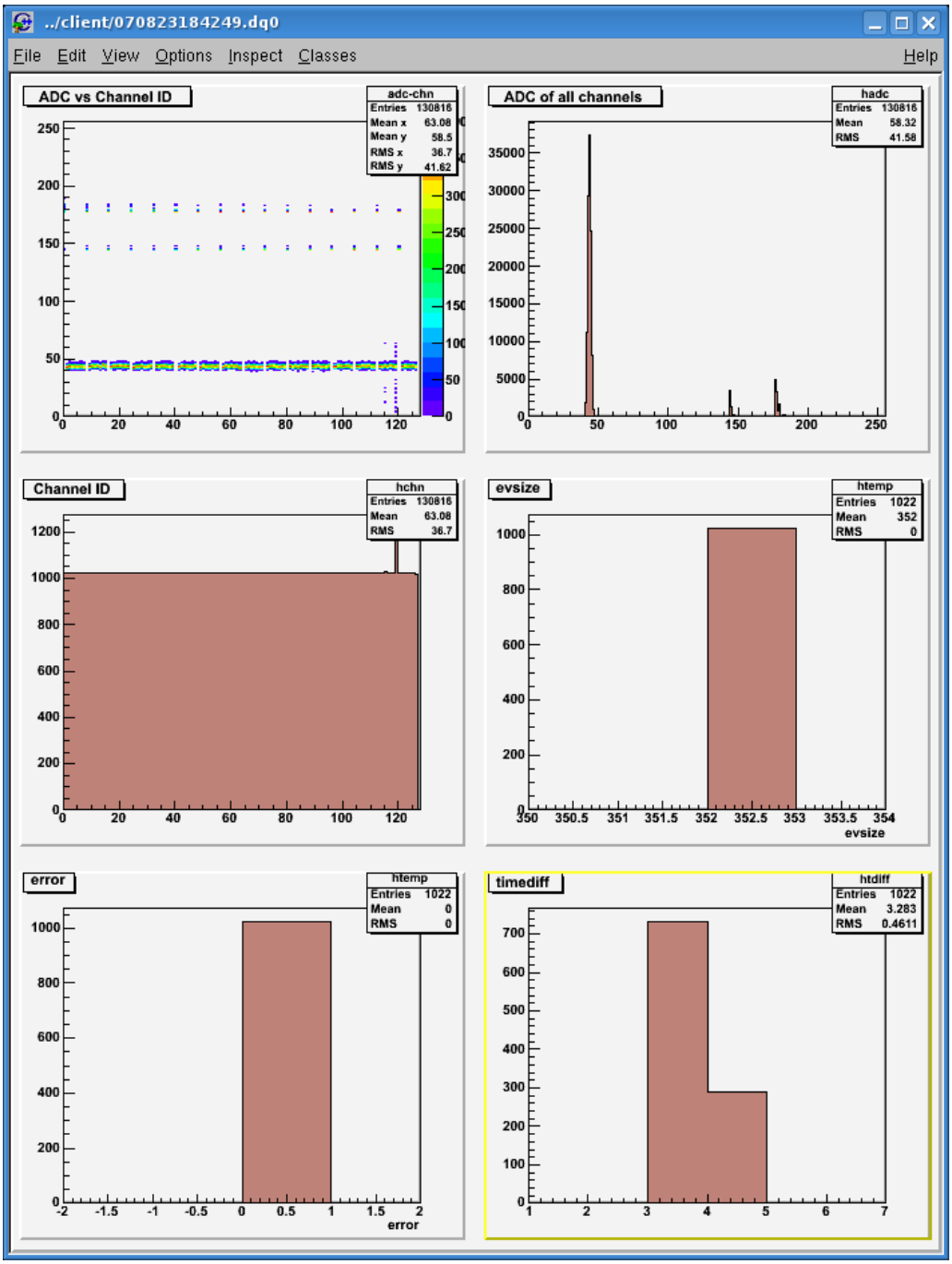
```
<< jusr i
<< jusr u
<< dsht 192.168.0.1 31337
>> DATASINKING host is set.
<< dsst
>> DATASINKING has started.
<< jusr t 10
<< dssp
>> DATASINKING has been stopped.

daqcapture:
Start Run 070823184249.dq0
Lost events 0x2406 @ ev0x2406
Lost events 0x2 @ ev0x2660
Stop Run. Downloaded 360096 bytes. 1024 packets @ 17.0645 KBytes/s
**Errors detected: 2
** Events lost: 9224
```

Analysis

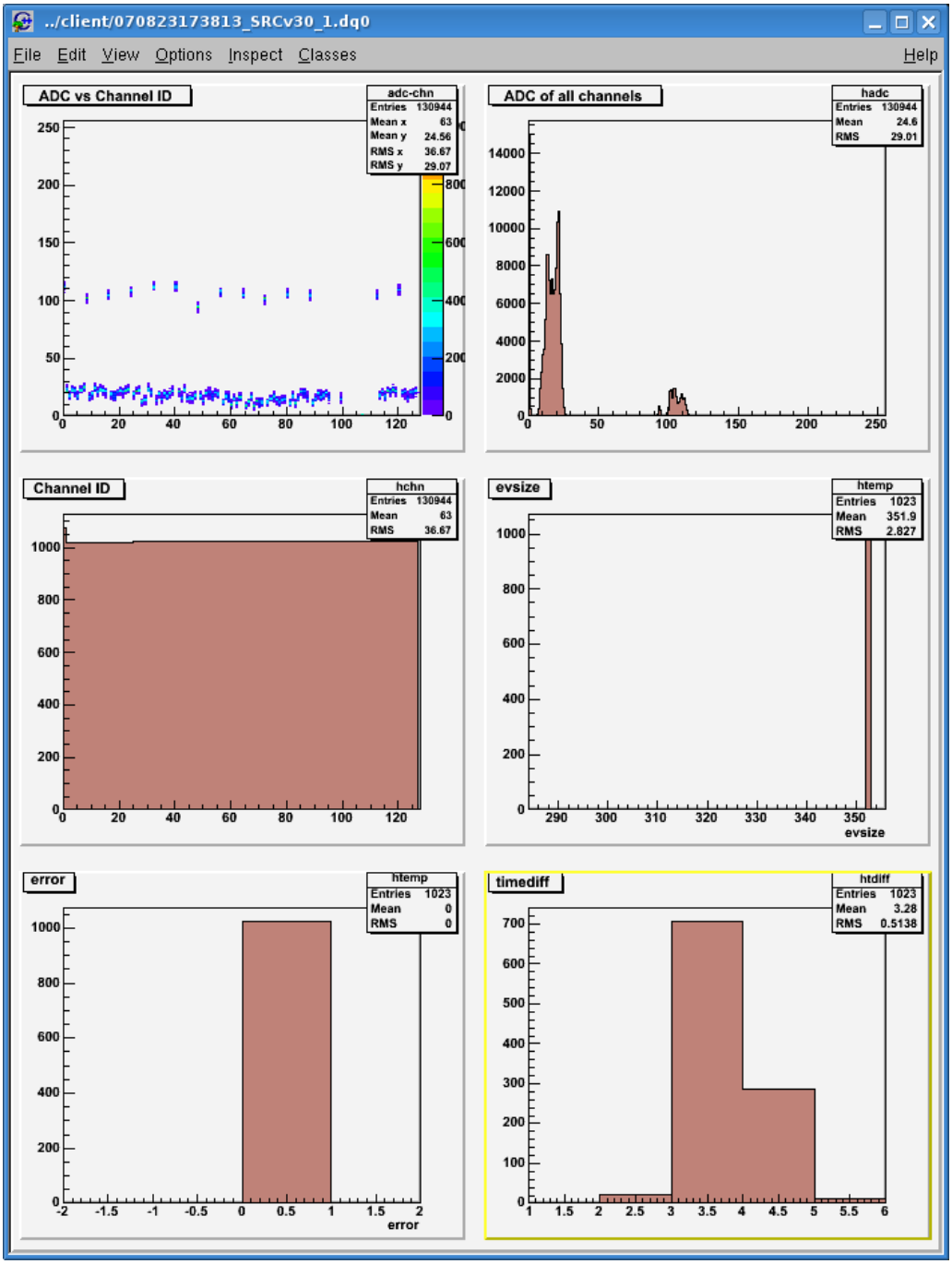
```
analysis$ root
root [1] .x go.C("../client/070823184249.dq0")
Macro for processing n3c files
Tn3c n(../client/070823184249.dq0) > Opening ../client/070823184249.dq0
File opened ../client/070823184249.dq0
filesize = 360096
Output file ../client/070823184249.root
TTree *t=n3c->MakeTree(); > ID 0004, ev# 00000000 at 00000160: 0400 1800 0000 0624
nch = a0, ch: 8303 93 12c 22e 32b
Size: 0x0160, Header: 00.04.00.18 00002406 900dc0de 00000000 0166e417 nch=160
ID 0004, ev# 00000001 at 000002c0: 0400 1800 0000 0724
nch = a0, ch: 8307 90 12a 229 32b
Size: 0x0160, Header: 00.04.00.18 00002407 900dc0de 00000000 0166e419 nch=160
ID 0004, ev# 00000002 at 00000420: 0400 1800 0000 0824
nch = a0, ch: 8304 b0 12a 22b 329
Size: 0x0160, Header: 00.04.00.18 00002408 900dc0de 00000000 0166e41c nch=160
ID 0004, ev# 00000003 at 00000580: 0400 1800 0000 0924
nch = a0, ch: 830f b3 12b 22b 329
Size: 0x0160, Header: 00.04.00.18 00002409 900dc0de 00000000 0166e41f nch=160
(Int_t)1022
```

Histograms, Board SRCV40_6

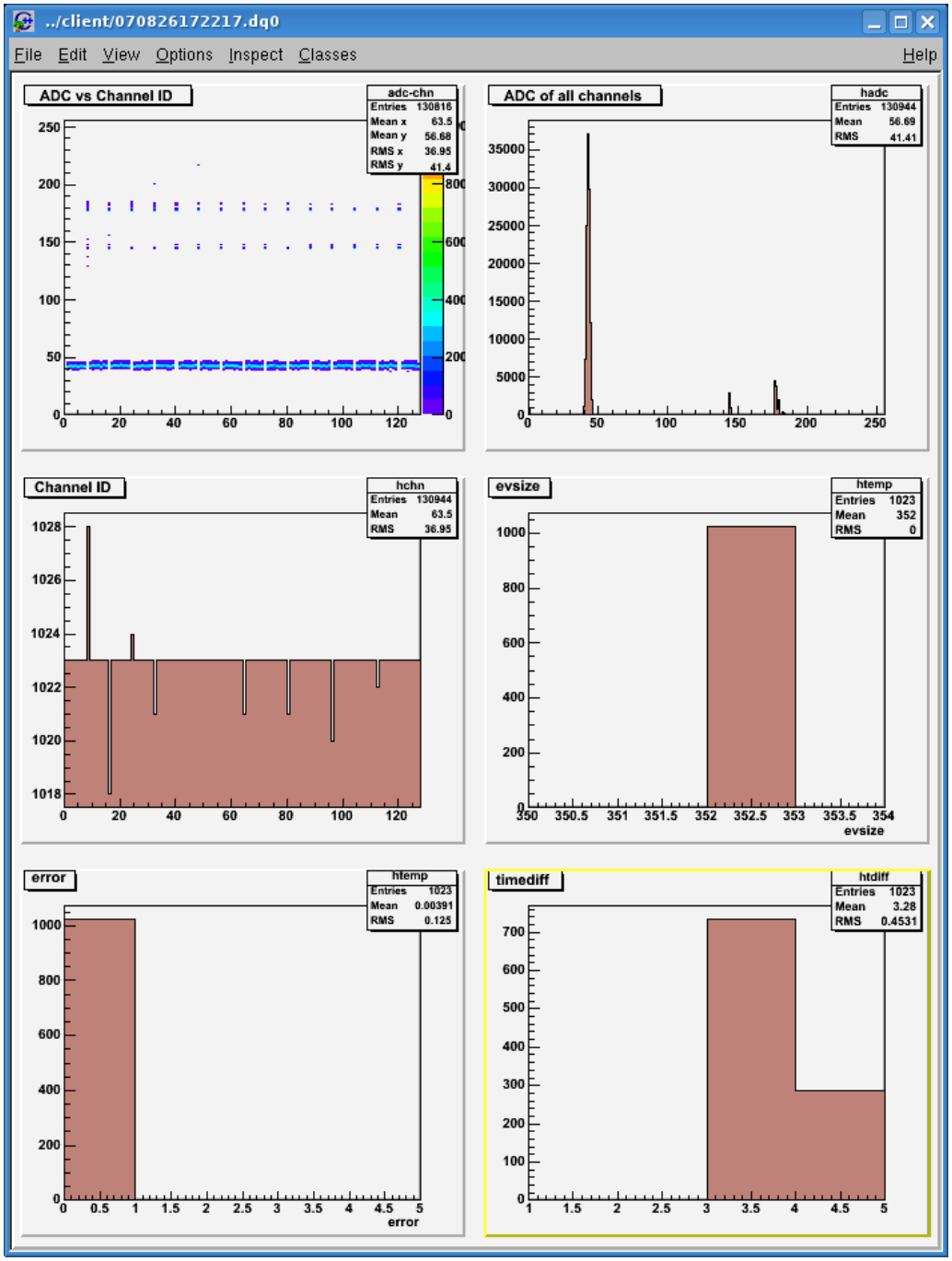


Power consumption 5.0V, 0.520A

For Comparison, Board SRCv30_0 (Old version)

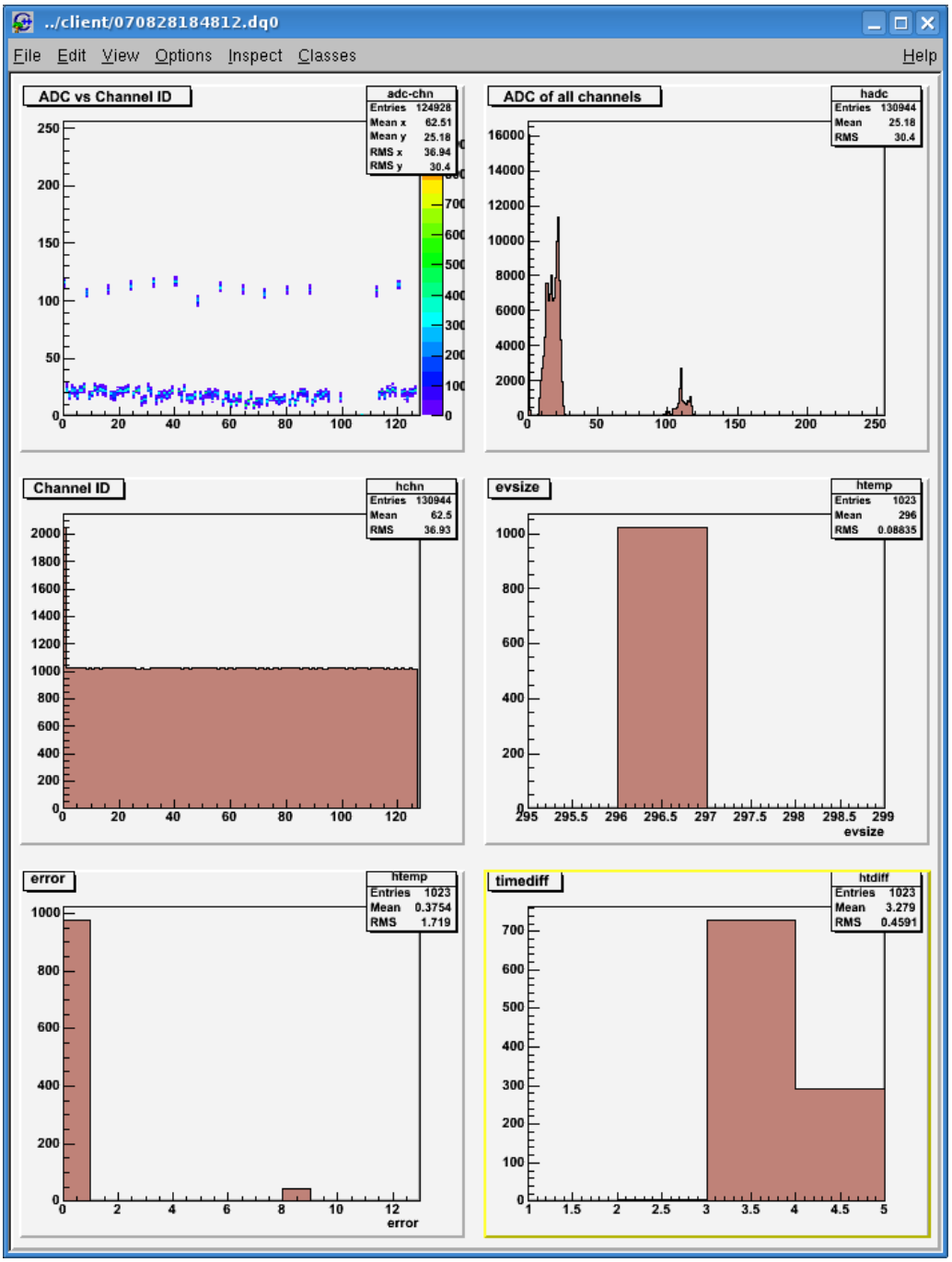


Board SRCV40_6 fpga: spxfem_v26_tested.stapl



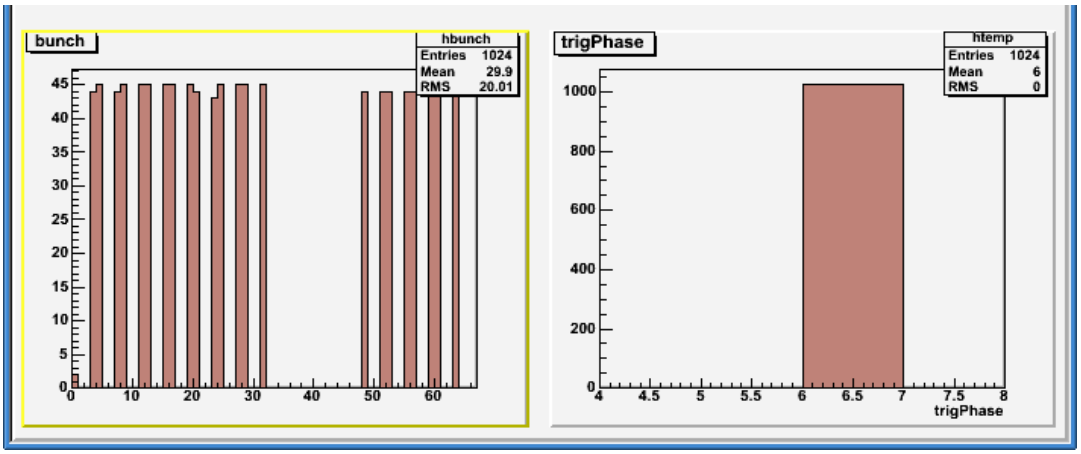
The pedestal line is much better on new board but test pulse line is split in two stripes. In general it works but some channel numbers are screwed up. In version 23 there were lots of errors Error ID 7733, ev# 000003f5 at 00057240 but channel numbers are OK.

Board SRCv30_0, femV2d, software revision past 533

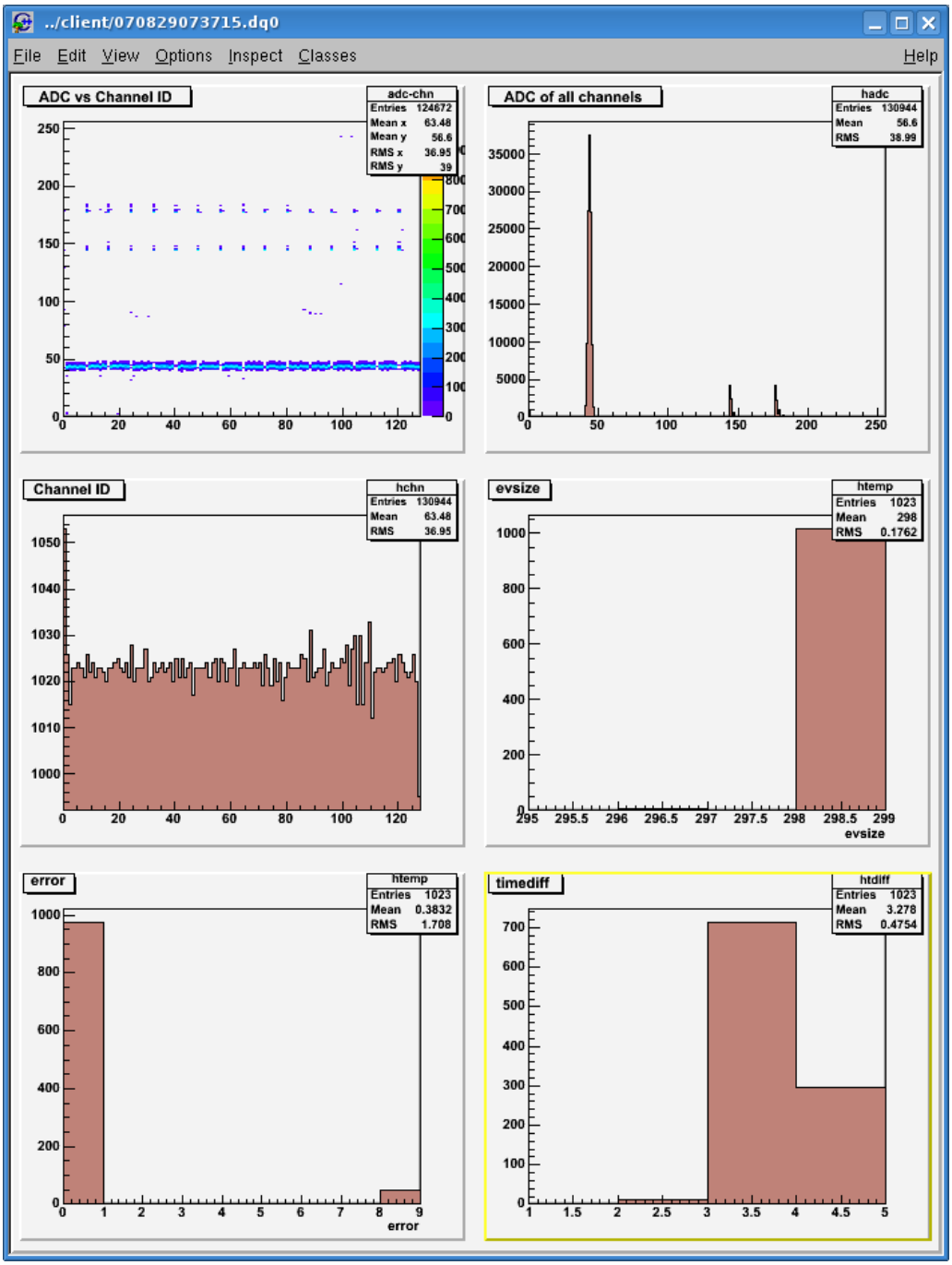


The same as on page 6.

Bunch number and TrigPhase.



Board SRCV40_6, fpga: spxfem_v2d_tested.stapl



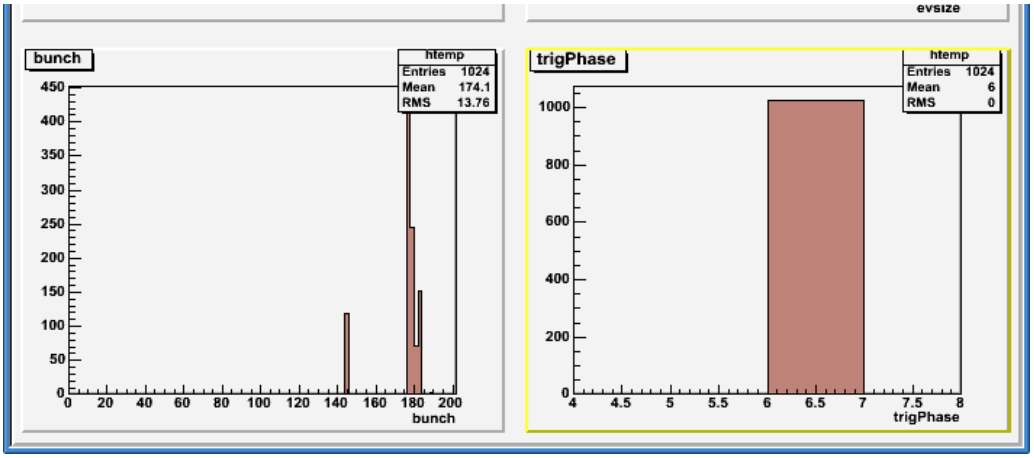
Errors:

```
Error CHn 01!=00, ev#00000002 @ 0000037e
ID 83b6, ev# 00000003 at 000004a8: 0400 1c00 0000 0400
nch = 83, ch: 83b6 12d 22d 32a 42c
Ev00000004[012a] hdr:00.04.00.1c 900dc0de 071c5c51 ch[83]:83b6 012d 022d 032a
Error CHn 01!=00, ev#00000003 @ 000004a8
Error CHn 01!=00, ev#00000004 @ 000005d2
```

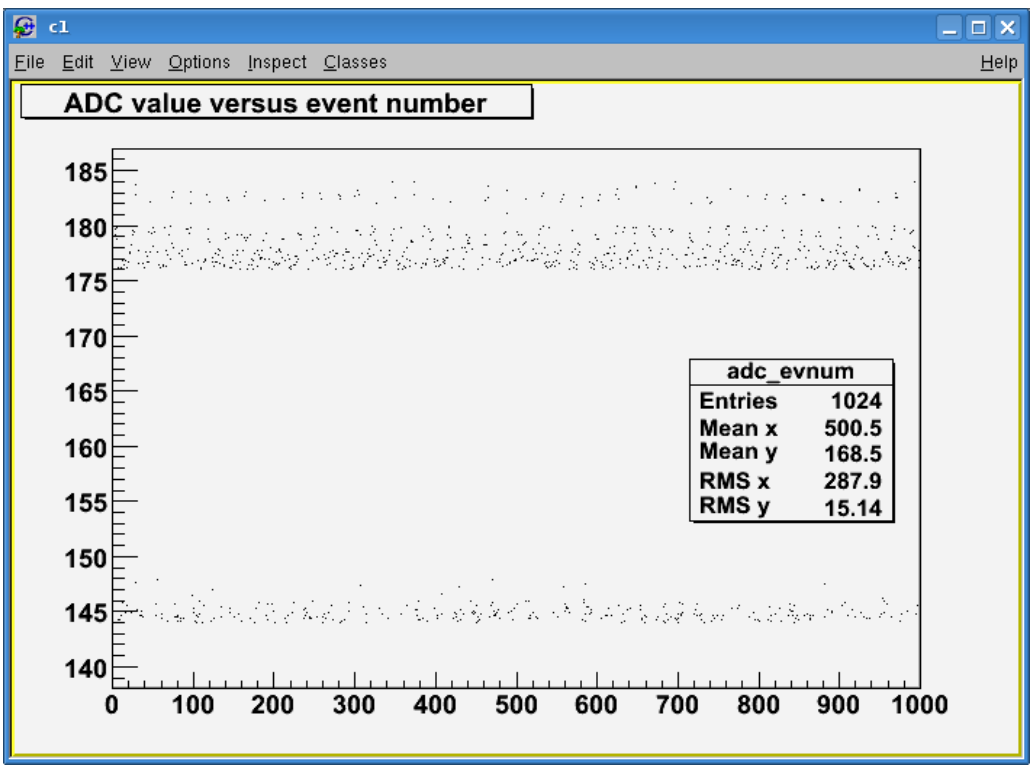
Channel ID histogram does not look good.

Looks like instead of bunch number we have channel 0 which was reported missing.

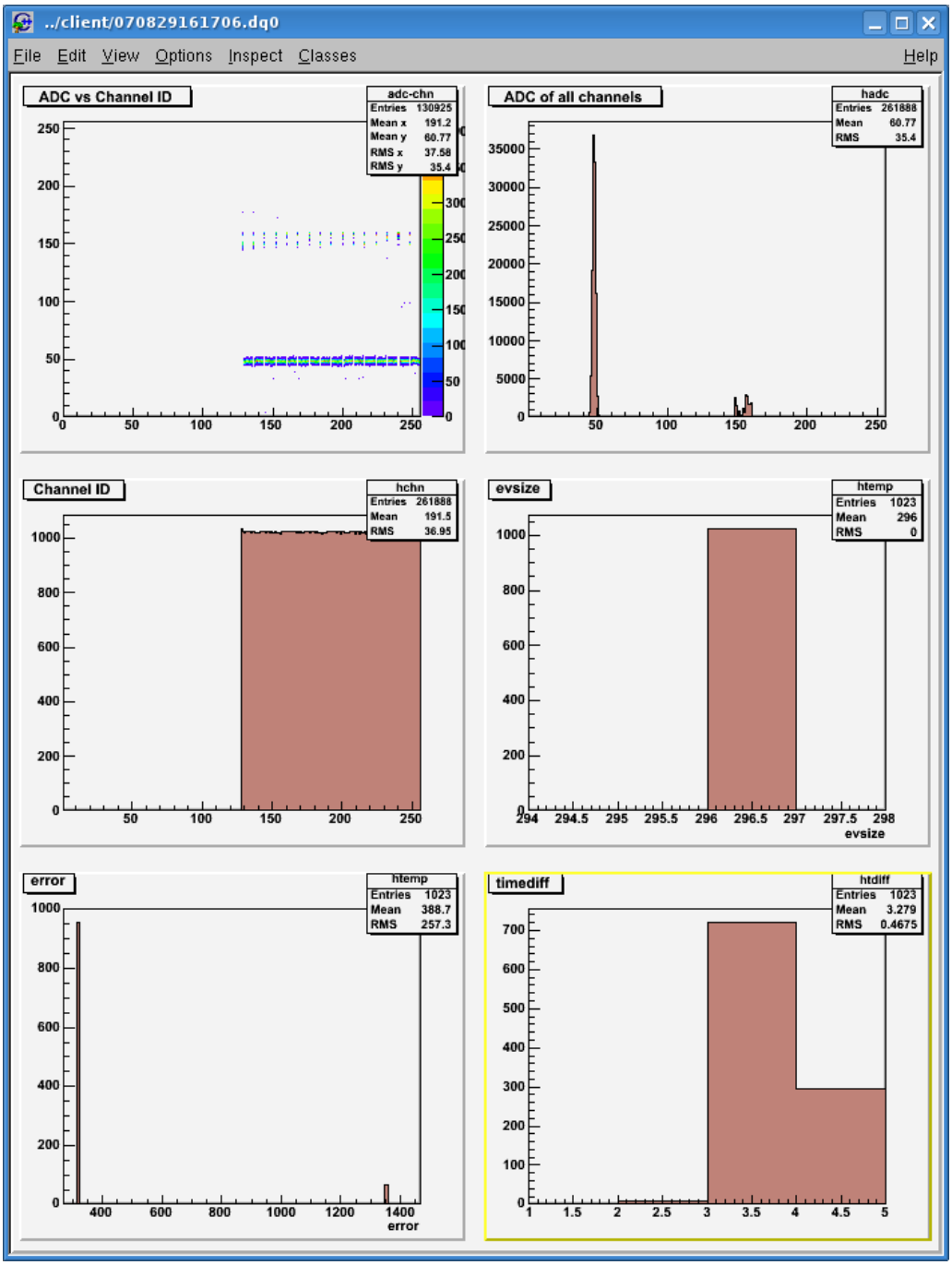
The trigPhase is OK, that means the timing is OK.



ADC versus event number. Could be that bit 5 randomly missing?

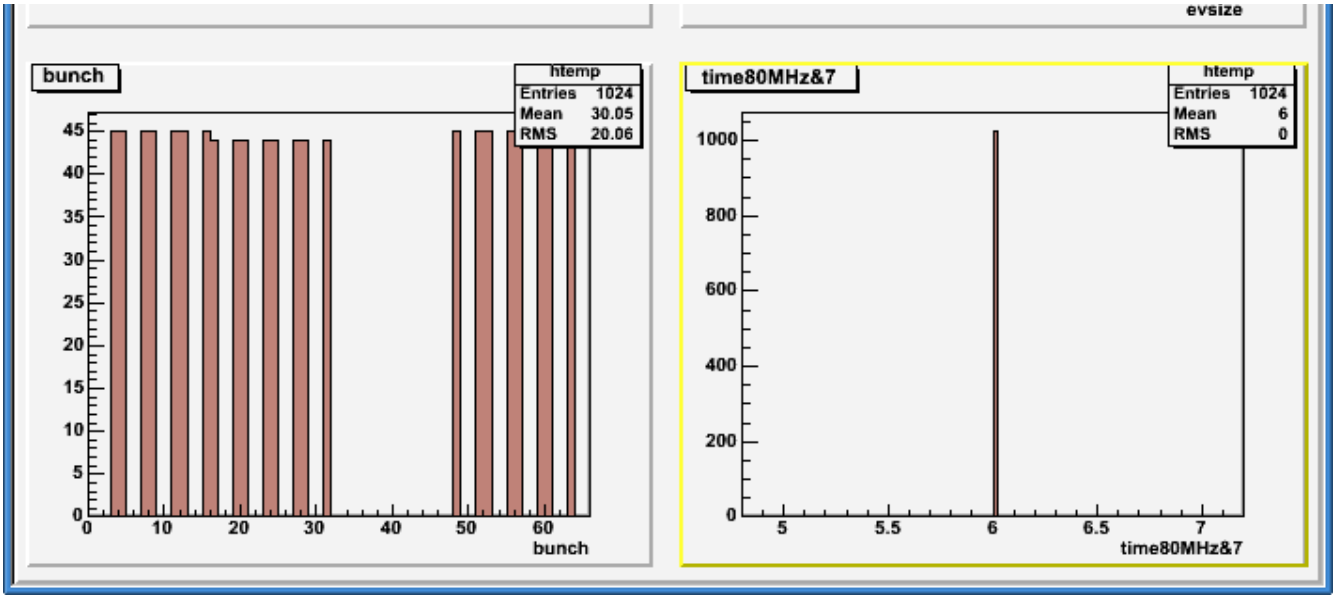


Board SRCV40_6, spxfem_v2d_tested.stapl, jtag/ped_2nd.fem



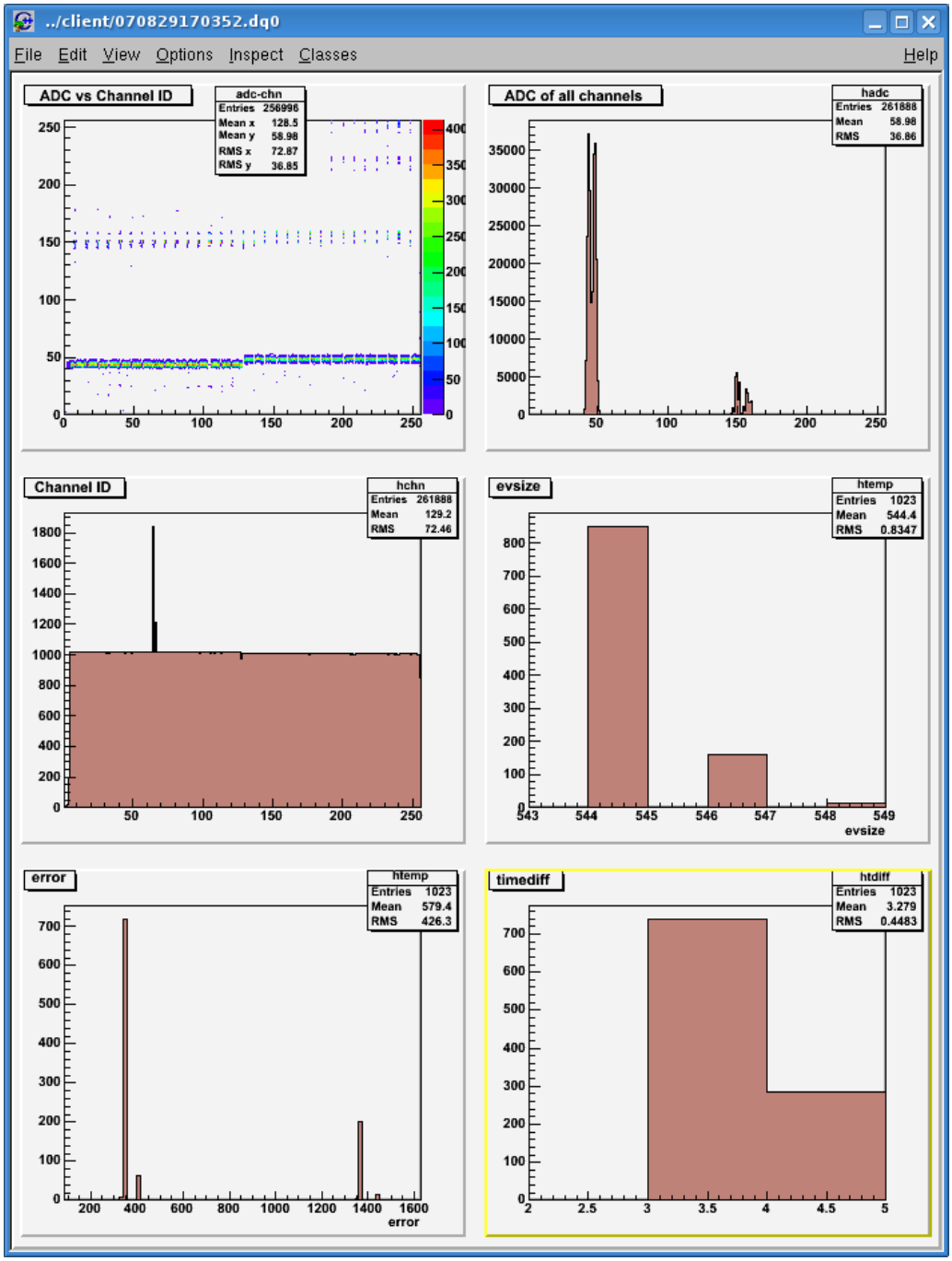
Finally it looks similar to first chip.

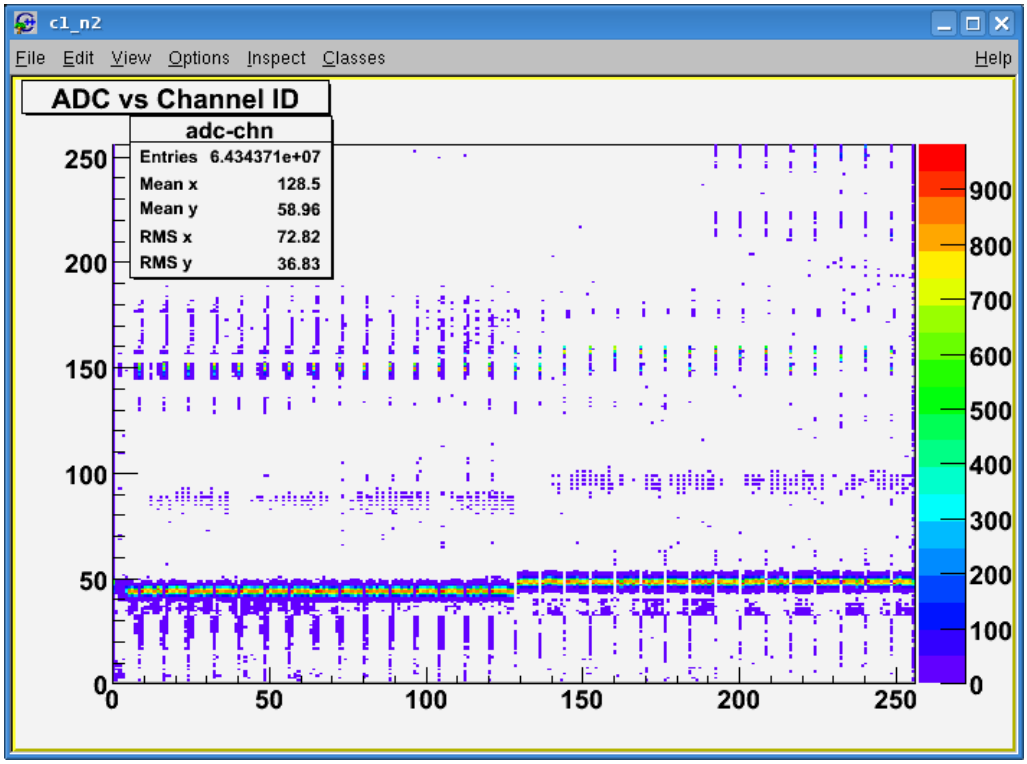
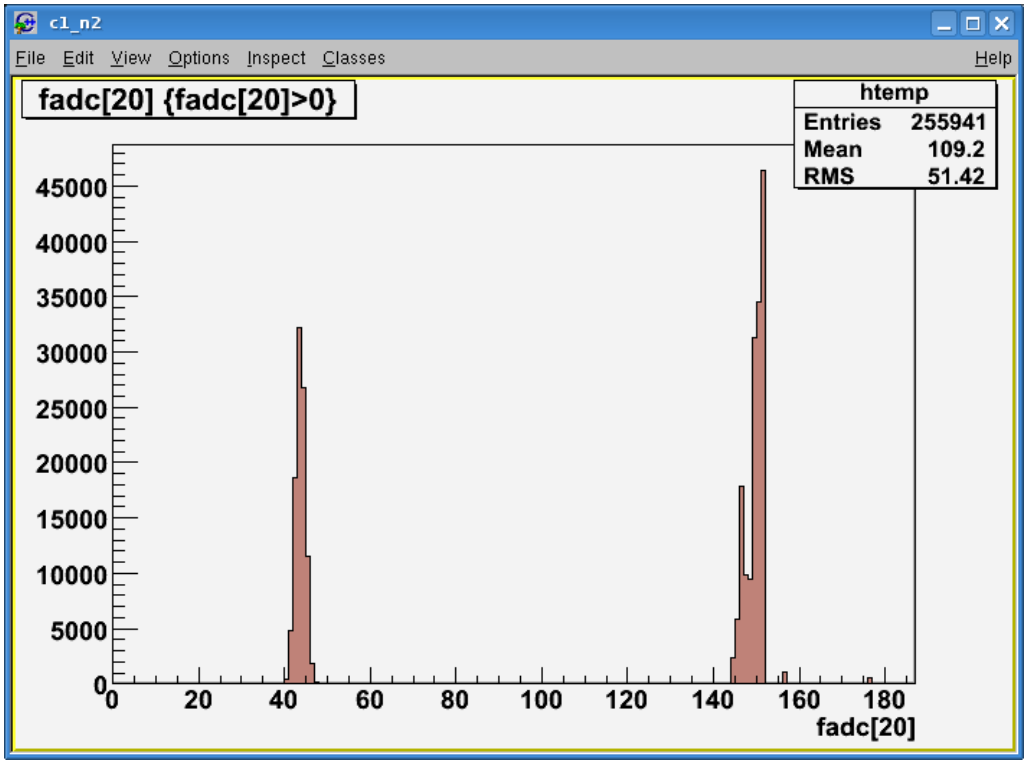
The bunch number is similar to board SRCV30.



Board SRCV40_6, Both Chips Enabled

spxfem_v2d_tested.stapl, ped_2chips.fem, svn 534.



The gap in the calibration stripe is much smaller. The higher amplitudes in scip2 (channels above 150) somehow related to chip1.

More statistics