Data Collection Module
Final Design Review

- **SCHEDULE**
  - **DCM System Overview**
  - **DCM-FEM Relationship**
  - **DCM Board**
  - **DCM/VME/ONCS (Jamie Nagle)**
  - **DCM Test Results (part 1)**
  - **DCM Test Result (part 2) (Jamie Nagle)**
  - **Summary and Future Schedule**

DCM Team

- **Cheng-Yi Chi**
- **Jamie Nagle**
- **Bill Sippach (Lead Engineer)**
- **Herb Cunitz (Engineer)**
- **Li Zhang (Engineer)**

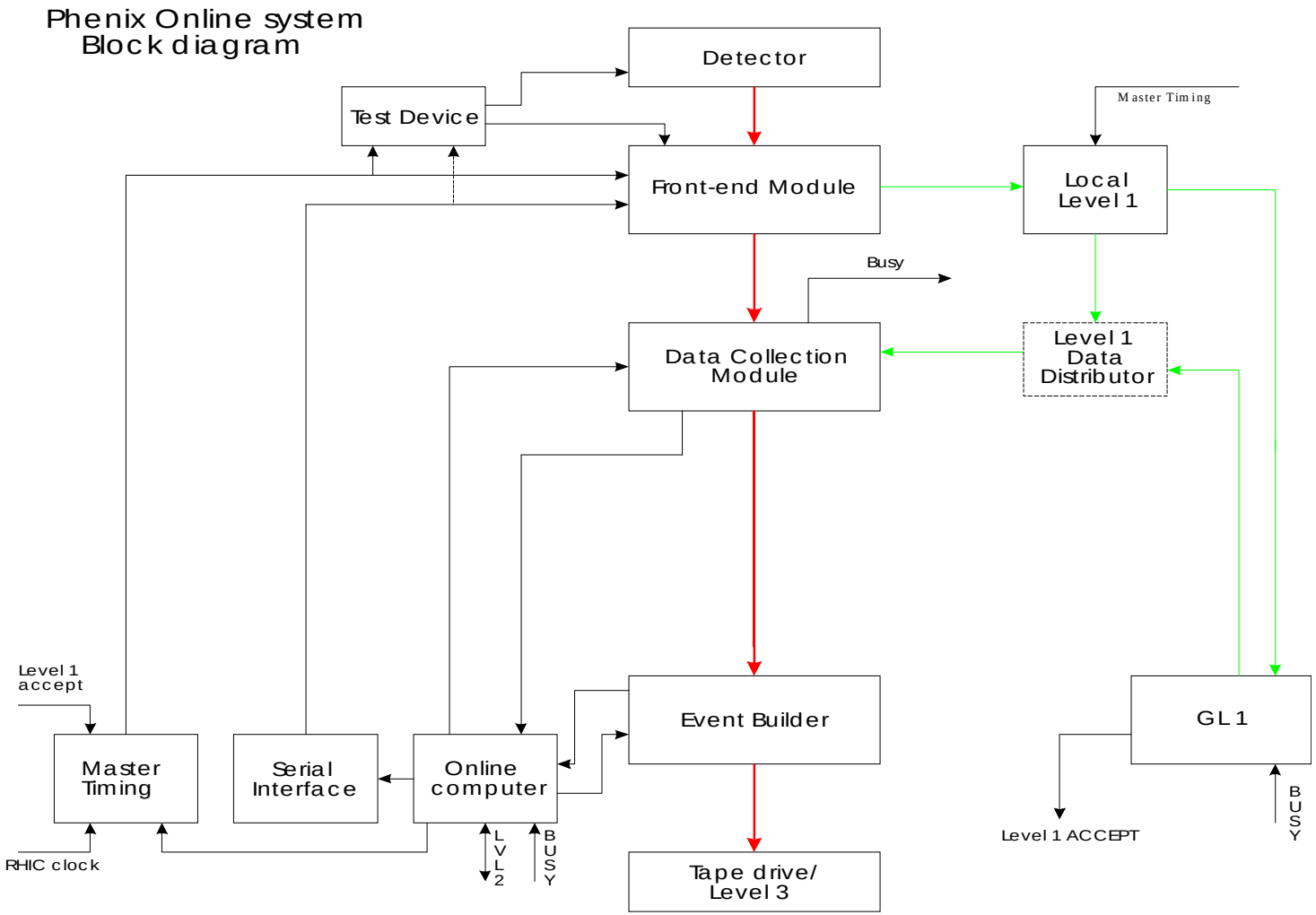
Review Purpose

- Obtain permission to purchase DCM and compressor board components
- Reasons:
  - Limited resources in Nevis Electronics shop
  - Long lead time for the components
  - Reasonable amount of testing has to be done for this stage of request

PHENIX Online System

- Approximately 300K detector channels
- Front end electronics close to or on the detectors
- Beam Crossing clock = 106 ns
- Level-1 trigger latency = 40 beam crossing clocks
- Maximum average Level-1 trigger rate = 25 kHz
- Fully pipelined, simultaneous Read / Write
- Detector occupancy ranges from
  - p + p (a few tracks) to Au +Au (2.5 - 10%)

PHENIX Online Overview



What is the function of the DCM

(really)

- Receive data from FEM's
- Reformat and send data to the Event Builder
- Send **BUSY** when there is no more space to take anymore data

(It could be simple, but foolishly we want to run in a dead-timeless DAQ system for all detectors in PHENIX)

DCM Function

- Zero suppressing FEM data
- Receiving Level-1 trigger primitives
- Applying calibration constants
- Error and alignment checking/handling
- First stage of the event building
- Reformatting data to send to the Event Builder
- Data Monitoring/Histogramming/Calibration
- Generating higher level trigger primitives
- Providing FEM data buffer

FEM in PHENIX

- Buffer detector signals either in AMU, FADC or 1-bit Y/N memory.
- Simultaneously R/W system
  - continuously record data, digitized accepted Level-1 events, buffer data and send to DCM's
- Capable of buffering five (5) Level-1 triggers.
- Fully controlled by Scheduler through Mode bits

FEM Data Transfer Rule

- FEM sends data to DCM over optical cable.
  - (through HP 101(2)2/101(2)4 (de)serializer)
    - (“GLINK” chip)
- Event Packet is framed by header and trailer.
  - First and last words are marked by GLINK **CAV** signal
  - Data are mark by GLINK **DAV** signal
- FEM should only transmit data after receiving ENDAT through Scheduler.
  - (regulates data flow to DCM)

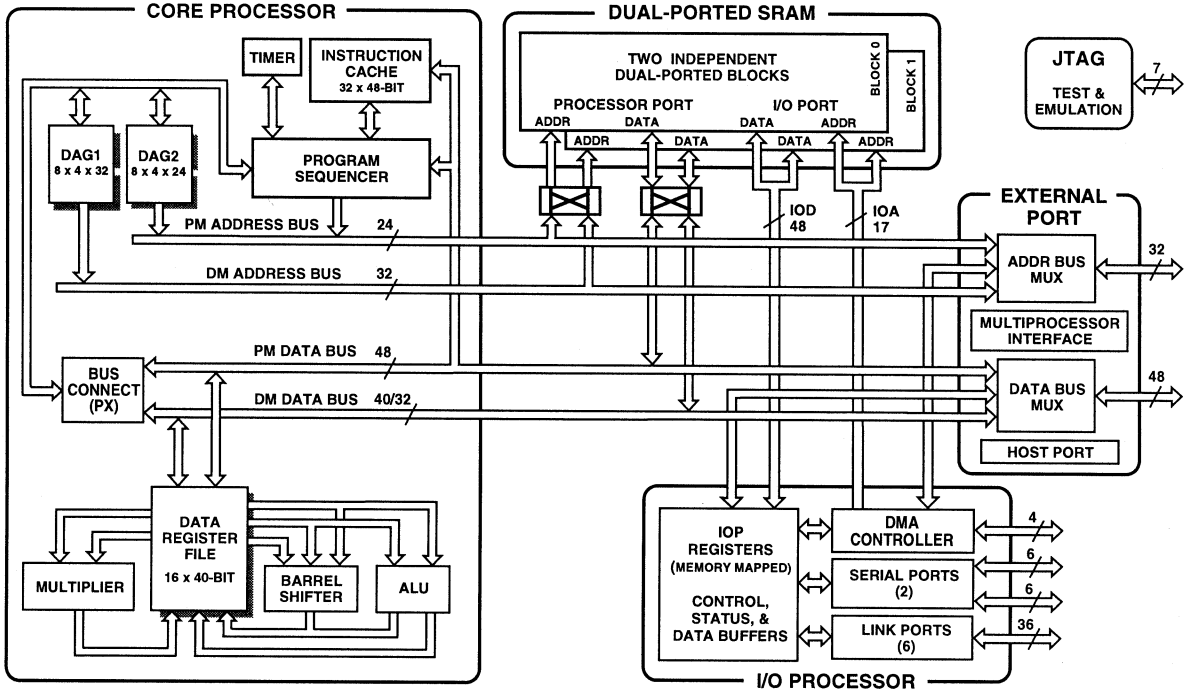
FEM Data Transfer Rule (cont.)

- Data is transferred to the DCM either in 2X or 4 X beam crossing rate (~ 20 or 40 MHz)
- No handshaking between DCM and FEM.
  - (regulation of data flow to DCM is done by shutting off Level-1 trigger)
- DCM has to provide **5** Level-1 accepted events buffer space for FEM after trigger is turned off
- FEM can have primary or alternative data format (for EMCal and MVD)
- FEM can pass zero suppression enable/disable bits

DCM Design Philosophy

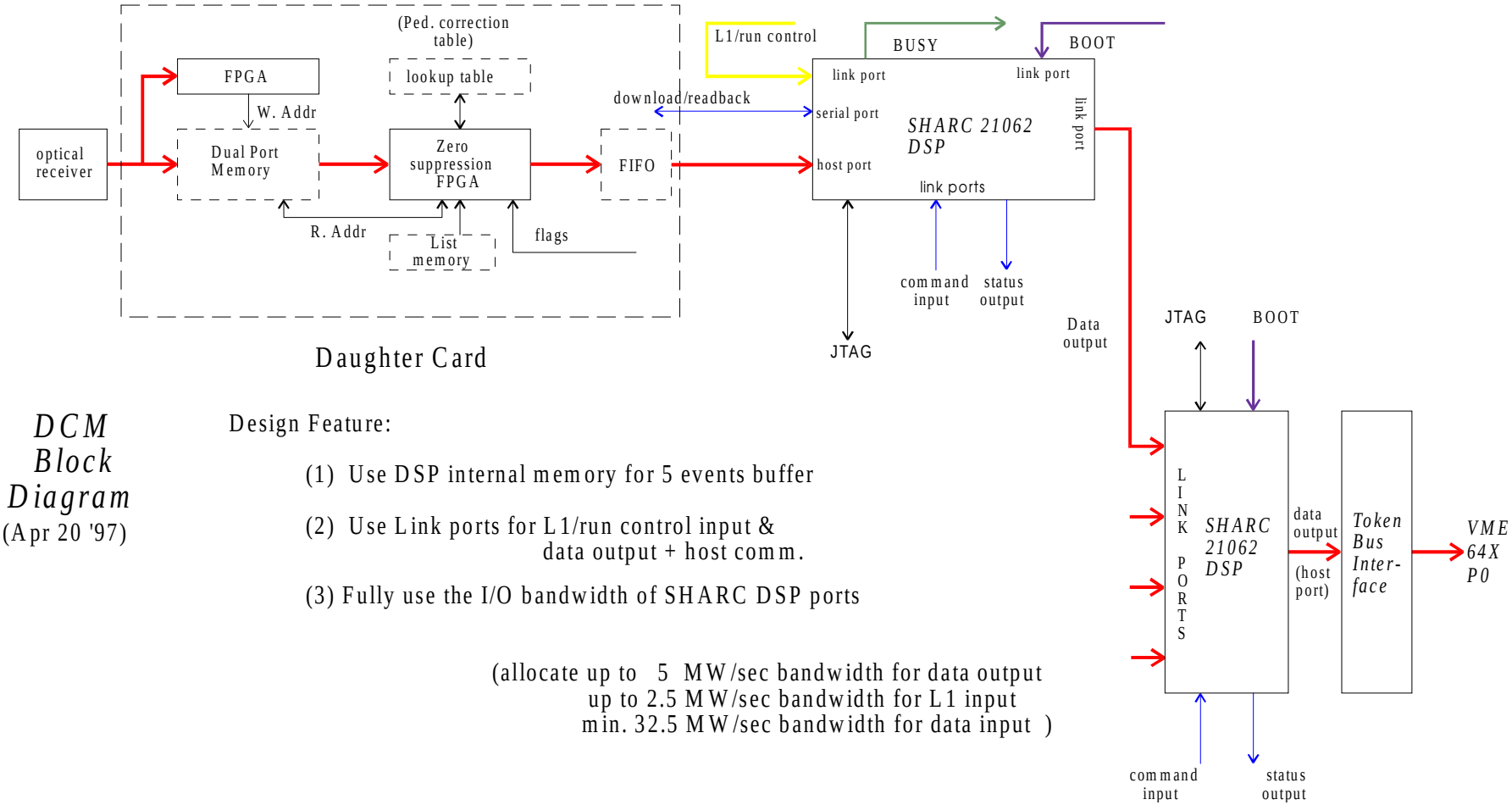
- Use FPGA for zero suppression of data
- After zero suppression, DSP's have more flexibility to do other jobs
- Contain the detector specific parts on a fixed portion of the DCM (daughter card)
- Use VME as download / slow(secondary) readout path

Analog Devices SHARC DSP



- **40 MHz clock**
- **2 Mbits dual port memory**
  - **(ADSP21062)**
- **I/O and computing units are independent**
- **40 Mwords per second I/O bandwidth**
- **1 host**
- **6 link ports (4 bits wide)**
- **2 serial ports**

DCM Block Diagram(1)



DCM Block Diagram
(Apr 20 '97)

Design Feature:

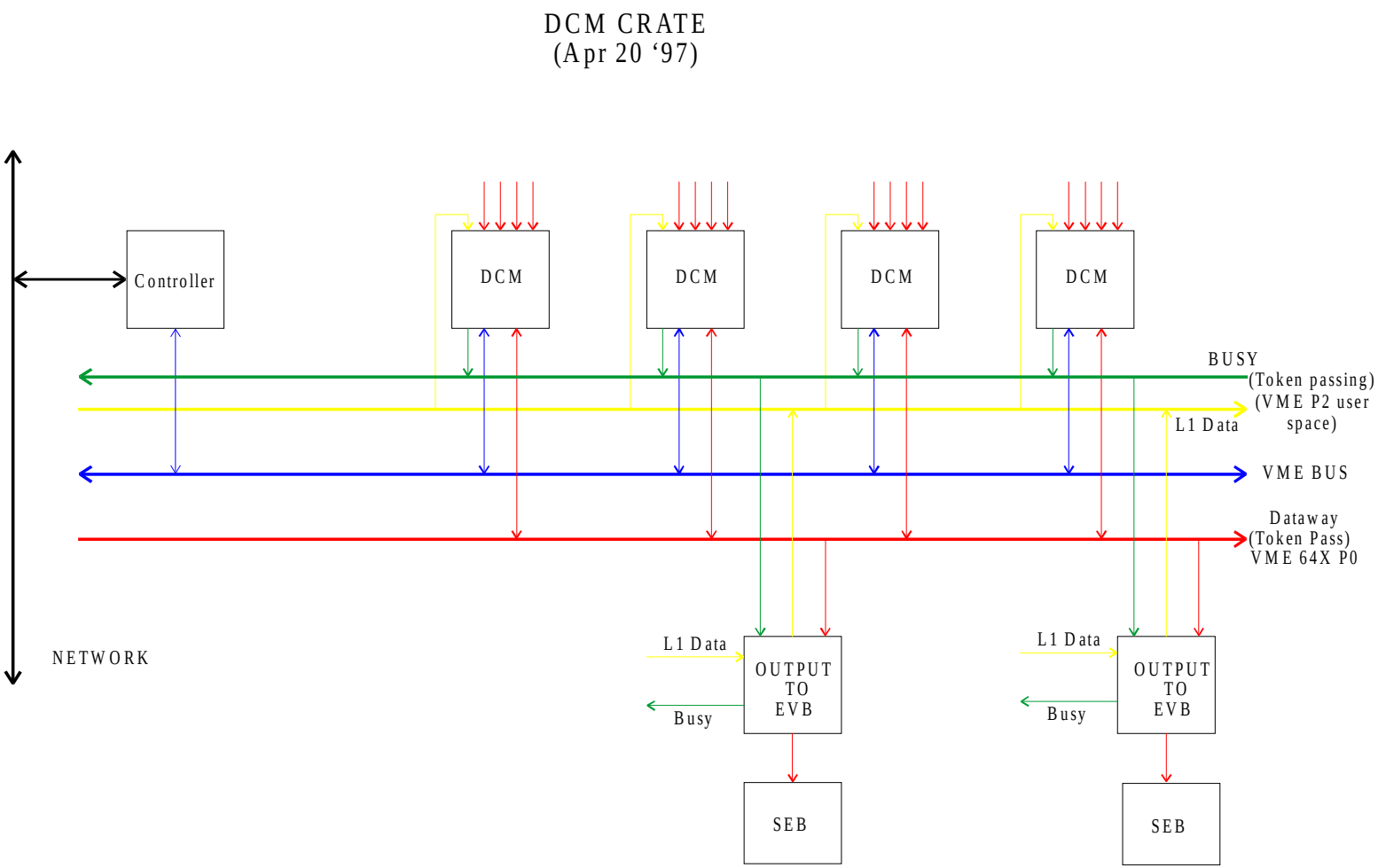
(1) Use DSP internal memory for 5 events buffer

(2) Use Link ports for L1/run control input &
data output + host comm.

(3) Fully use the I/O bandwidth of SHARC DSP ports

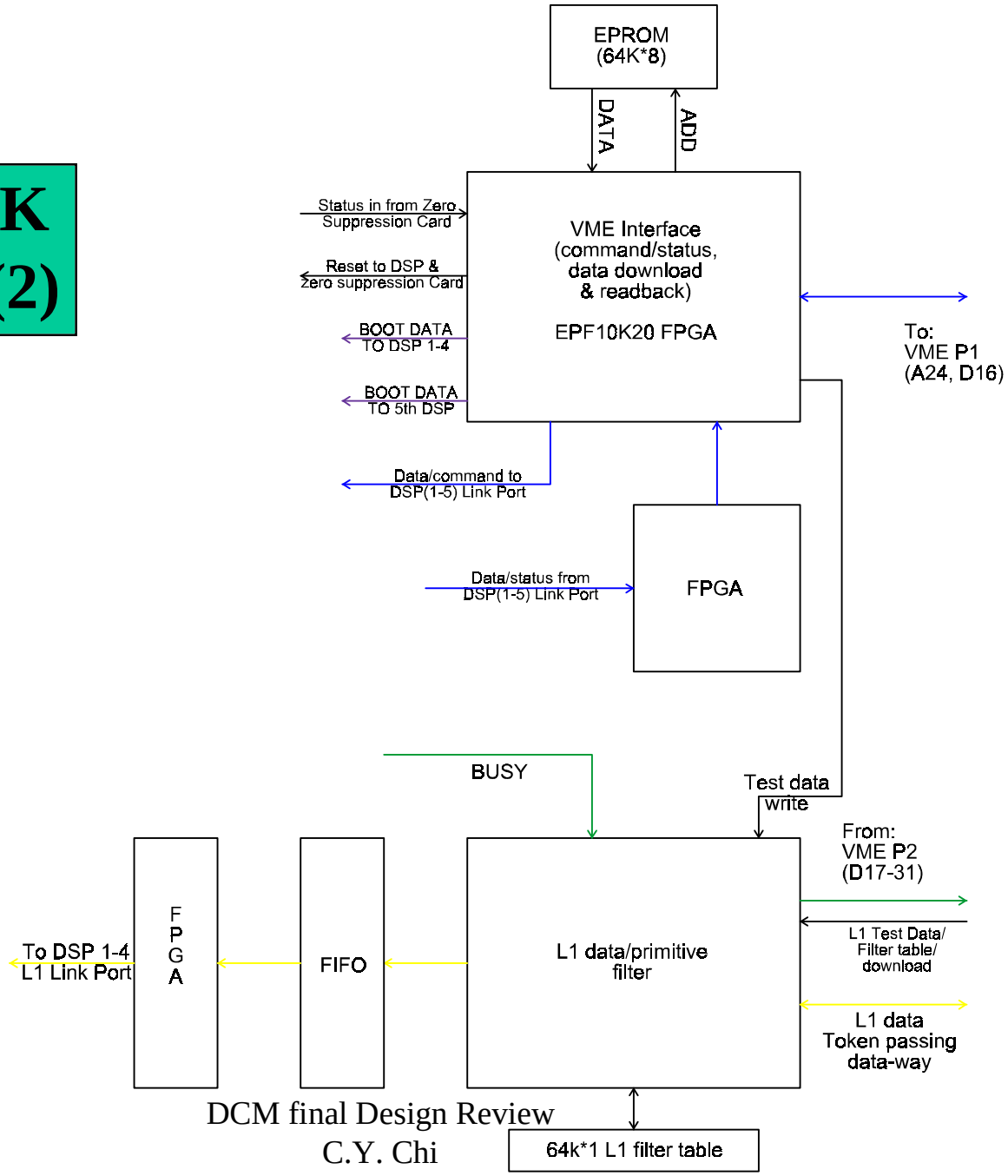
(allocate up to 5 MW/sec bandwidth for data output
up to 2.5 MW/sec bandwidth for L1 input
min. 32.5 MW/sec bandwidth for data input)

DCM Crate

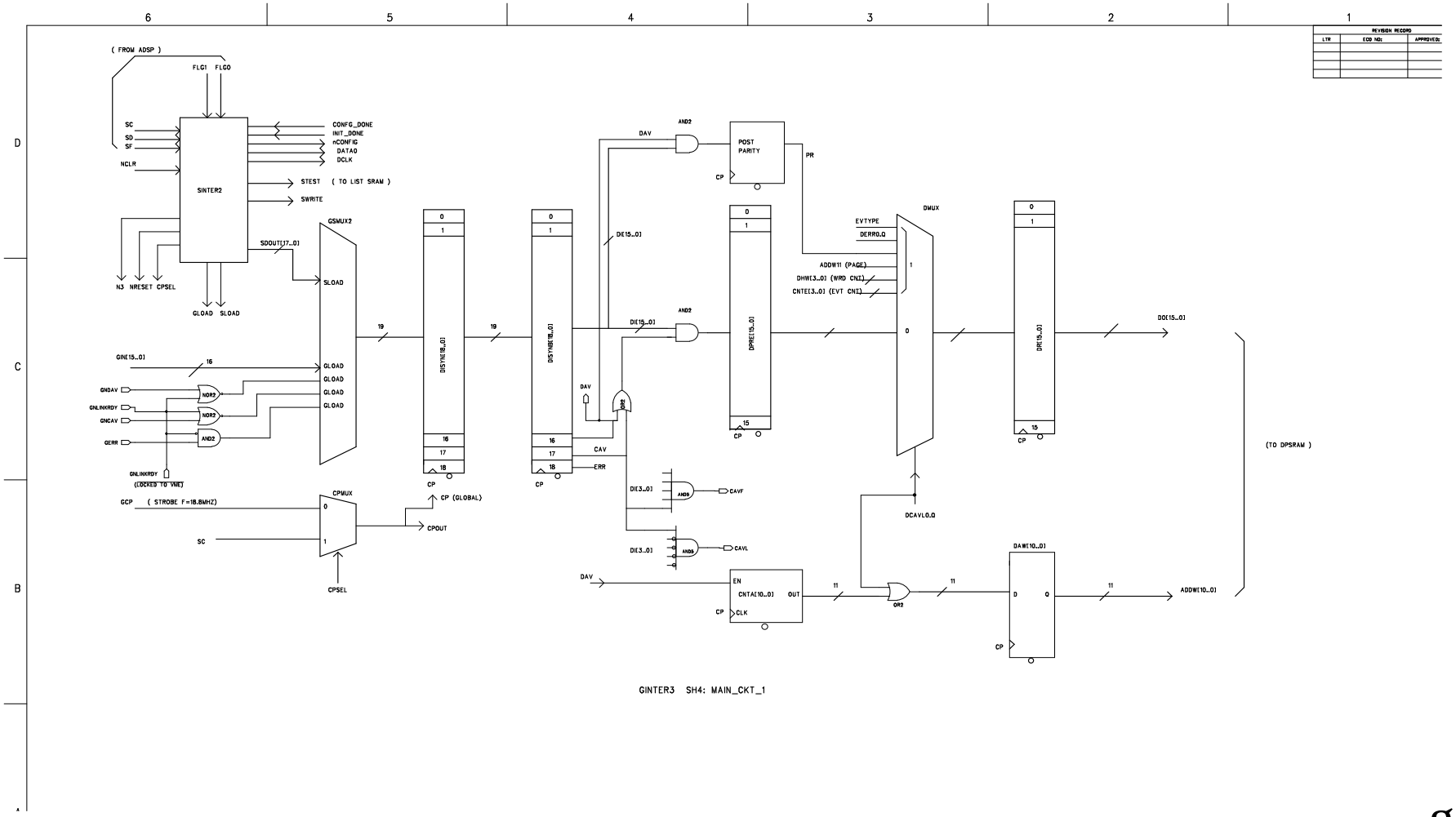

DCM CRATE
(Apr 20 '97)
Controller
DCM
DCM
DCM
DCM
BUSY
(Token passing)
(VME P2 user space)
L1 Data
VME BUS
Dataway
(Token Pass)
VME 64X P0
NETWORK
L1 Data
Busy
OUTPUT TO EVB
L1 Data
Busy
OUTPUT TO EVB
SEB
SEB

DCM
VME/L1 Interface
(Apr 20 '97)

DCM BLOCK DIAGRAM (2)



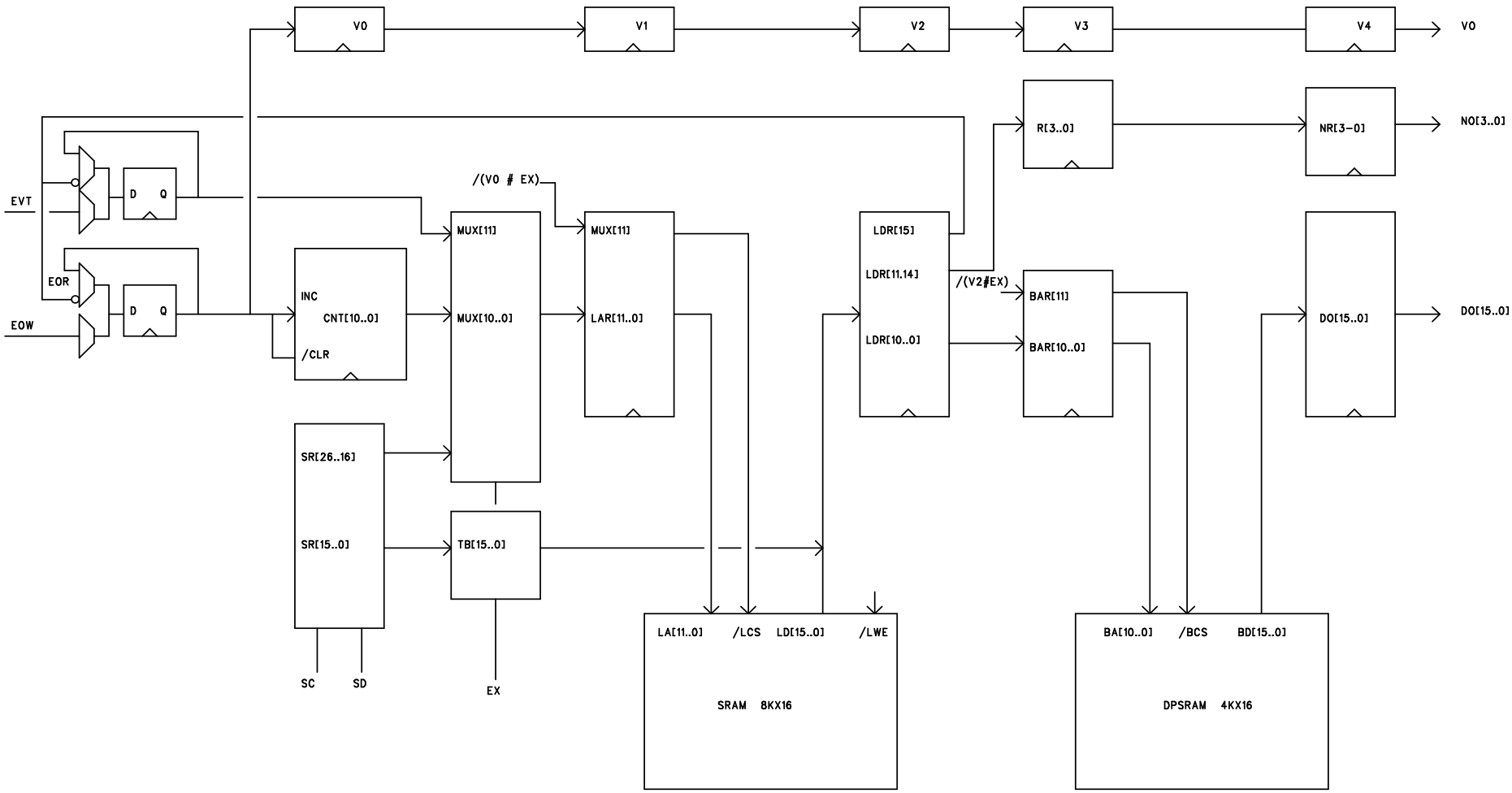
GLINK INTERFACE BLOCK DIAGRAM



gIn

ZERO SUPPRESSION (RE-ORDER DATA)

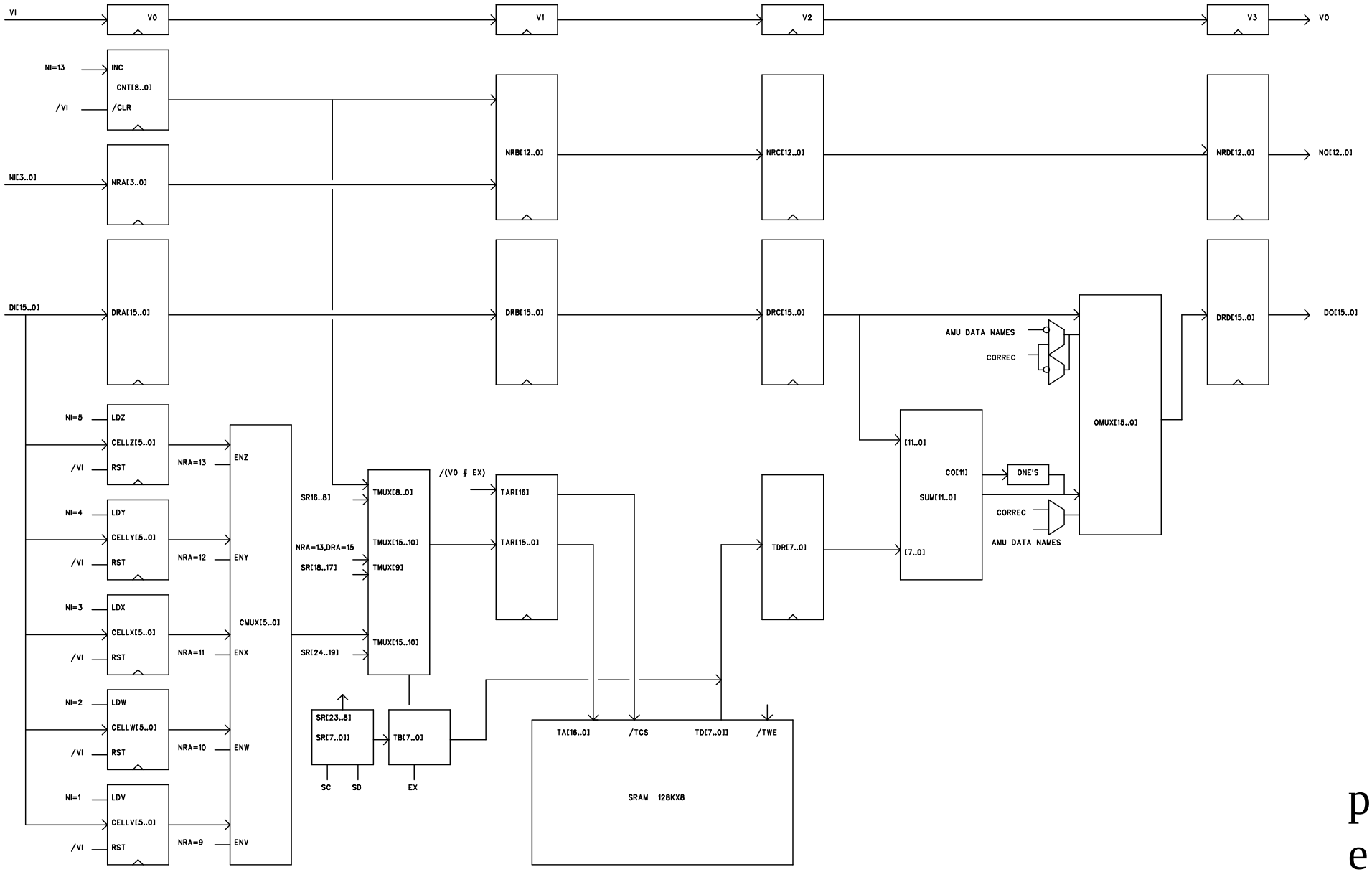
SK-ORD ORDERS AND LABELS DATA WRITTEN TO DPSRAM FROM FE MODULES



ord

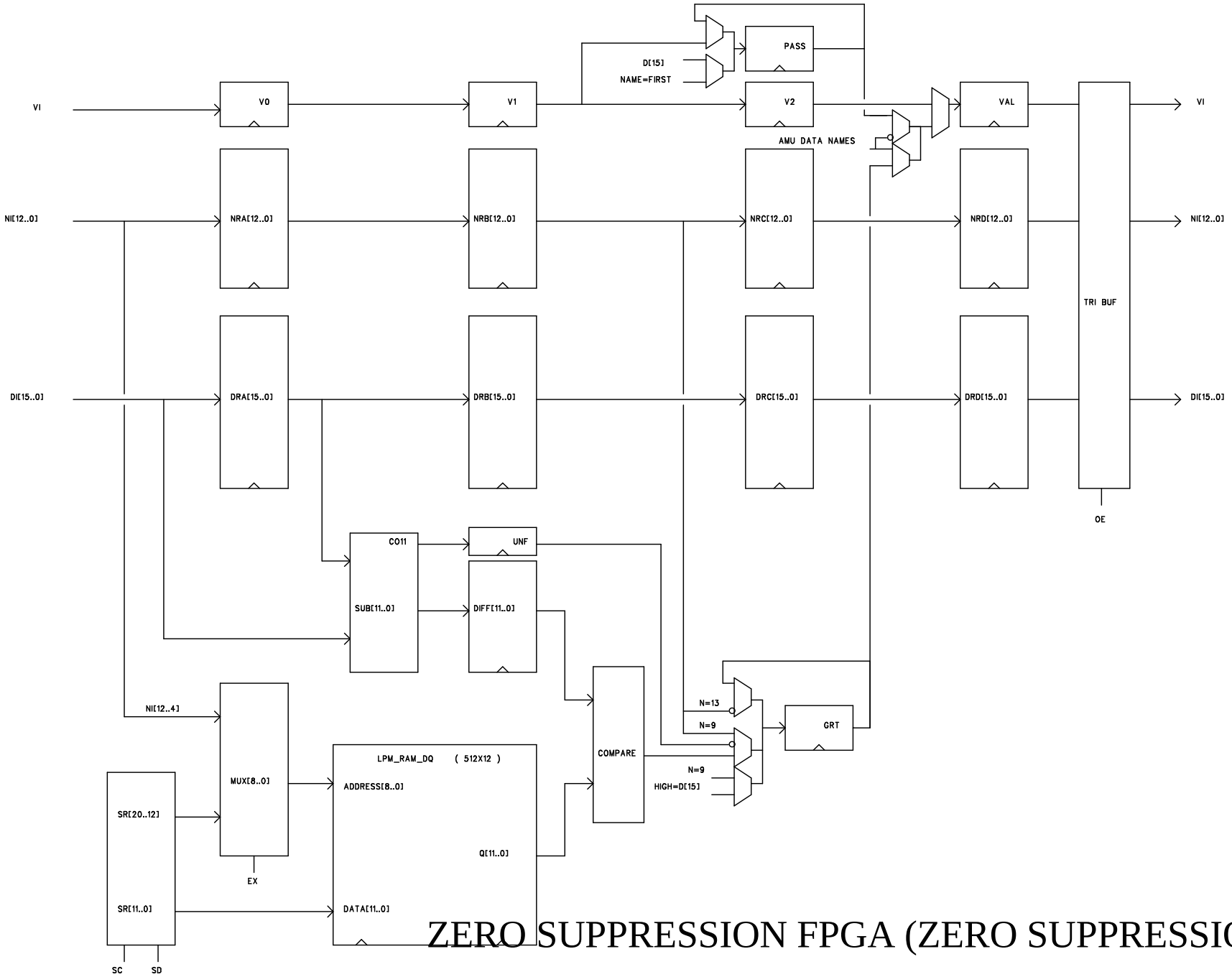
ZERO SUPPRESSION (PED. SUBTRACTION)

SK-PED CORRECTS AMU PEDESTALS AS FUNCTION OF CELL #,SIG#,SIG TYPE



ped

SK-ZER TESTS (SAMPLE2 - SAMPLE 1) VS THRESHOLD TO ZERO SUPPRESS.



ZERO SUPPRESSION FPGA (ZERO SUPPRESSION)

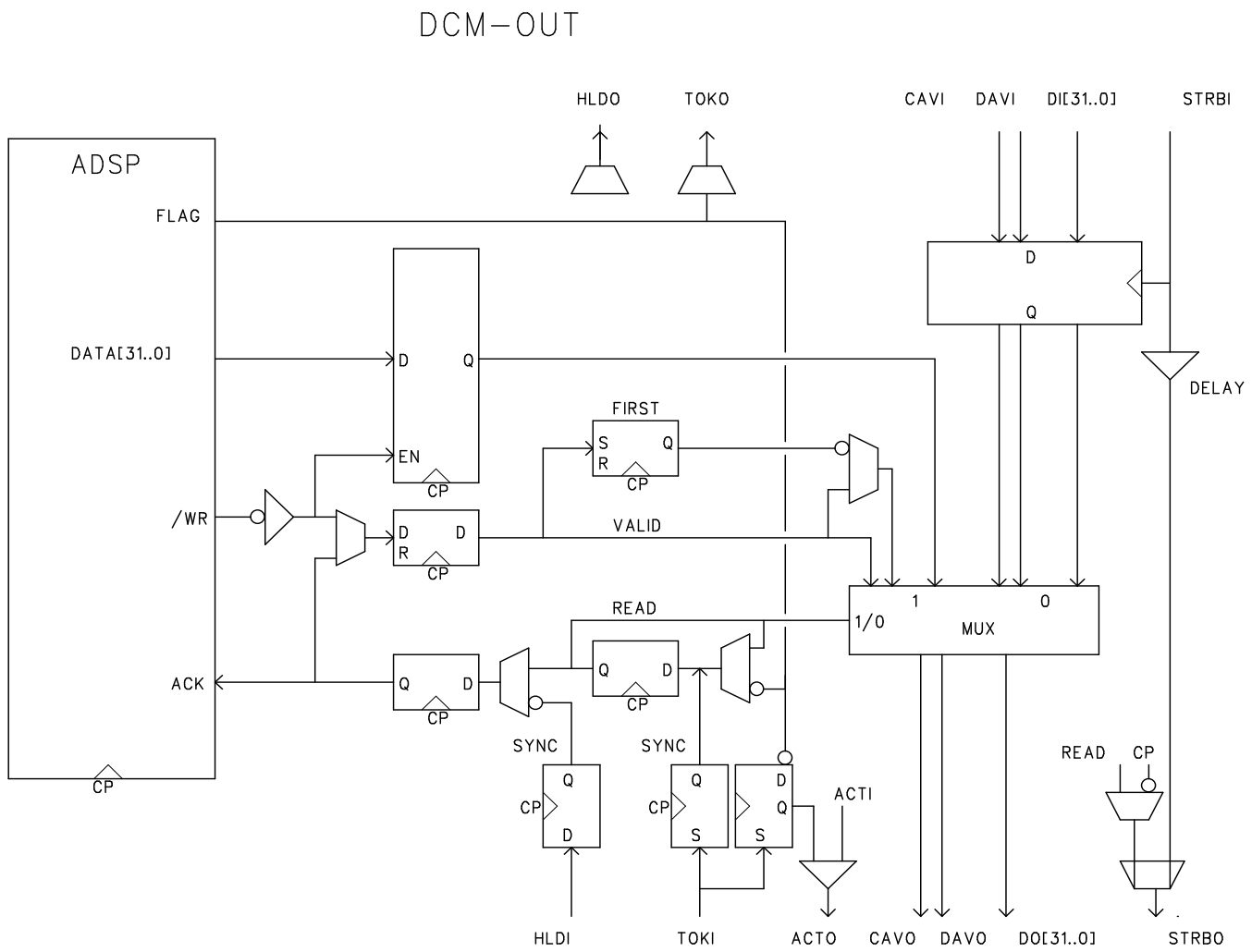
Compressor Board A (**AMU**) Memory Size

- Max. pedestal memory = **128K*8** bits
  - 2 *144 ch (2**8)* 3 AMU/Ch (2**2)* 64(2**6) (EMCAL)
- Max. threshold memory = **512*12** bits
  - 2 * 144ch (2**8) (MVD, EMCAL)
- Max.Dual port Memory = **4K *16** bits
  - 2 pages * (144 ch*5 words) (2**10) (EMCAL, MVD)
- Max. List Memory = **4K*16** bits
  - 4 pages * (144ch*5 words) (2**10)

Compressor Board T,D,P Memory Size

- Threshold table for TEC = 256*4 bits
  - 4 * 64 channel * 4 bits threshold
- FIFO size
  - 2K * 32 bits for TEC = 64 channel * 20 words/channel + X
- Channel sum table
  - 64 * 9 bits = 64 channel * 9 bits FADC sum

DCM DATA OUTPUT FPGA BLOCK DIAGRAM



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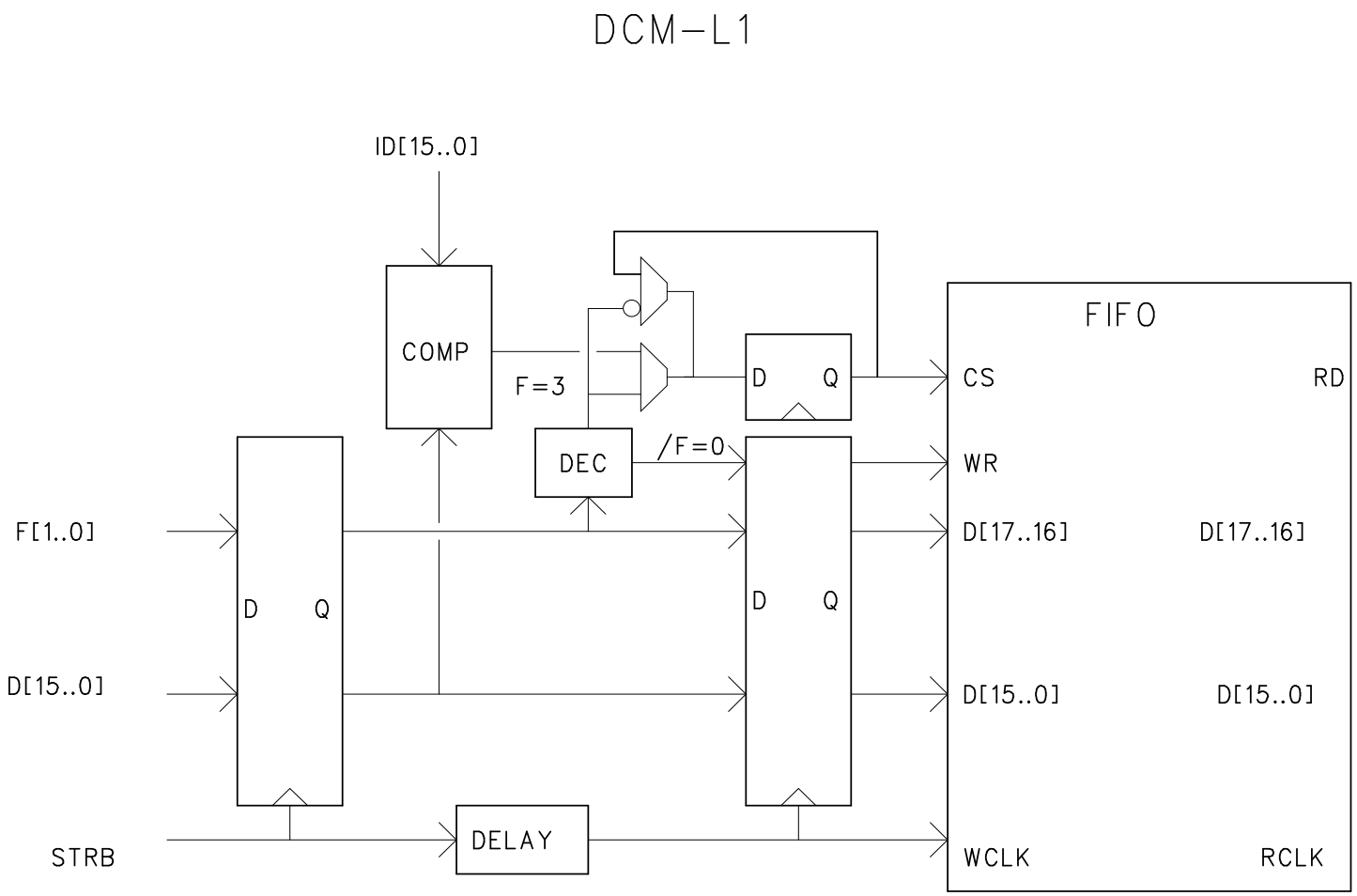
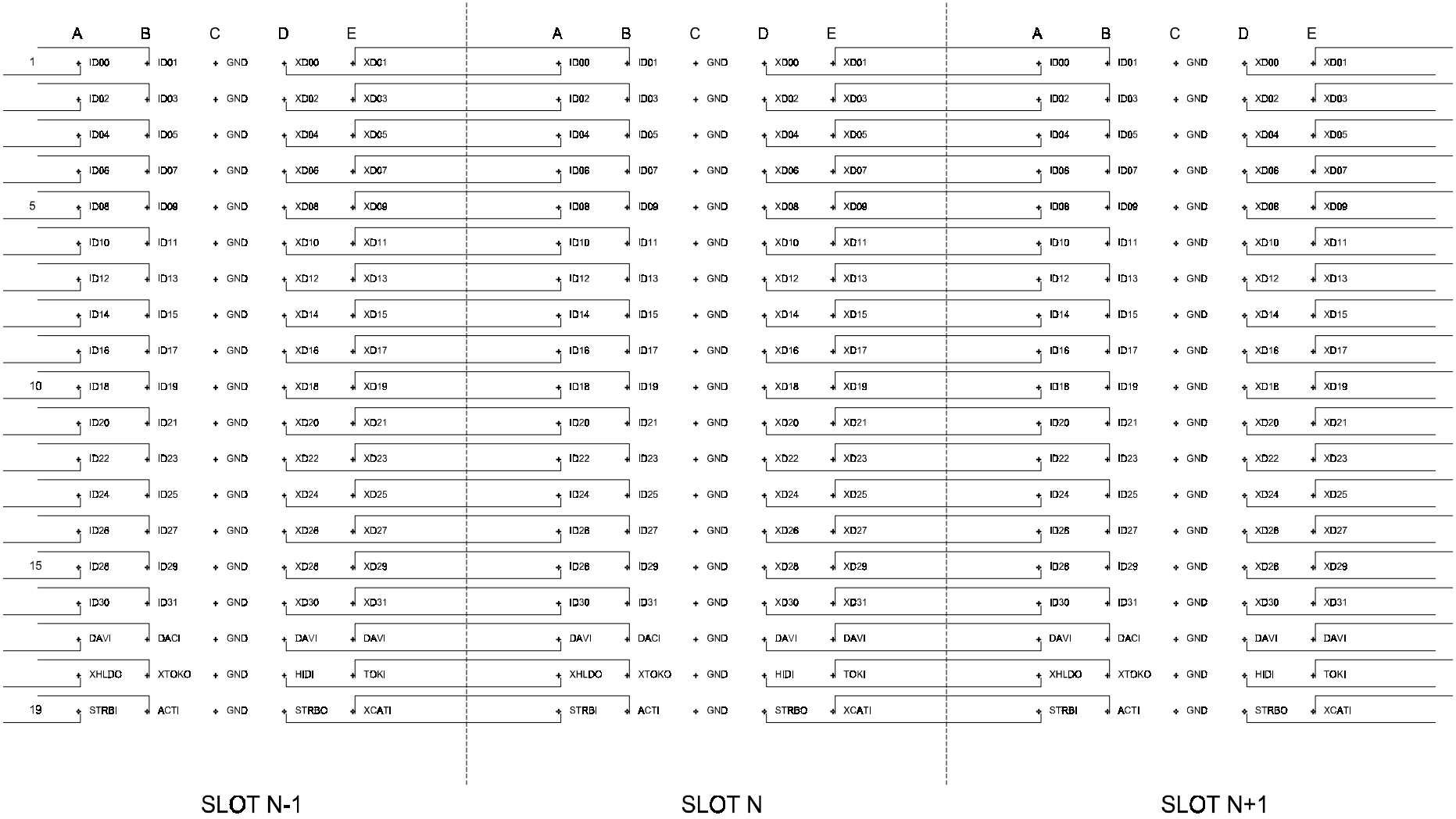
L1 FPGA BLOCK DIAGRAM





VME 64X P0 (FRONT VIEW)

DCM Final Design Review

C.Y. Chi

What VME can see from DCM during Data Taking

- Sample data/status through link ports
- 2 status words can be read by the controller. (without going through DSP link ports)
  - (i.e. compressor error, optical ready, FPGA booted, , “busy”, “token”, Level-1 FIFO full etc.)
- DCM raise flag, if it want to send information to Controller.
  - (flag state is reflected in VME status words)

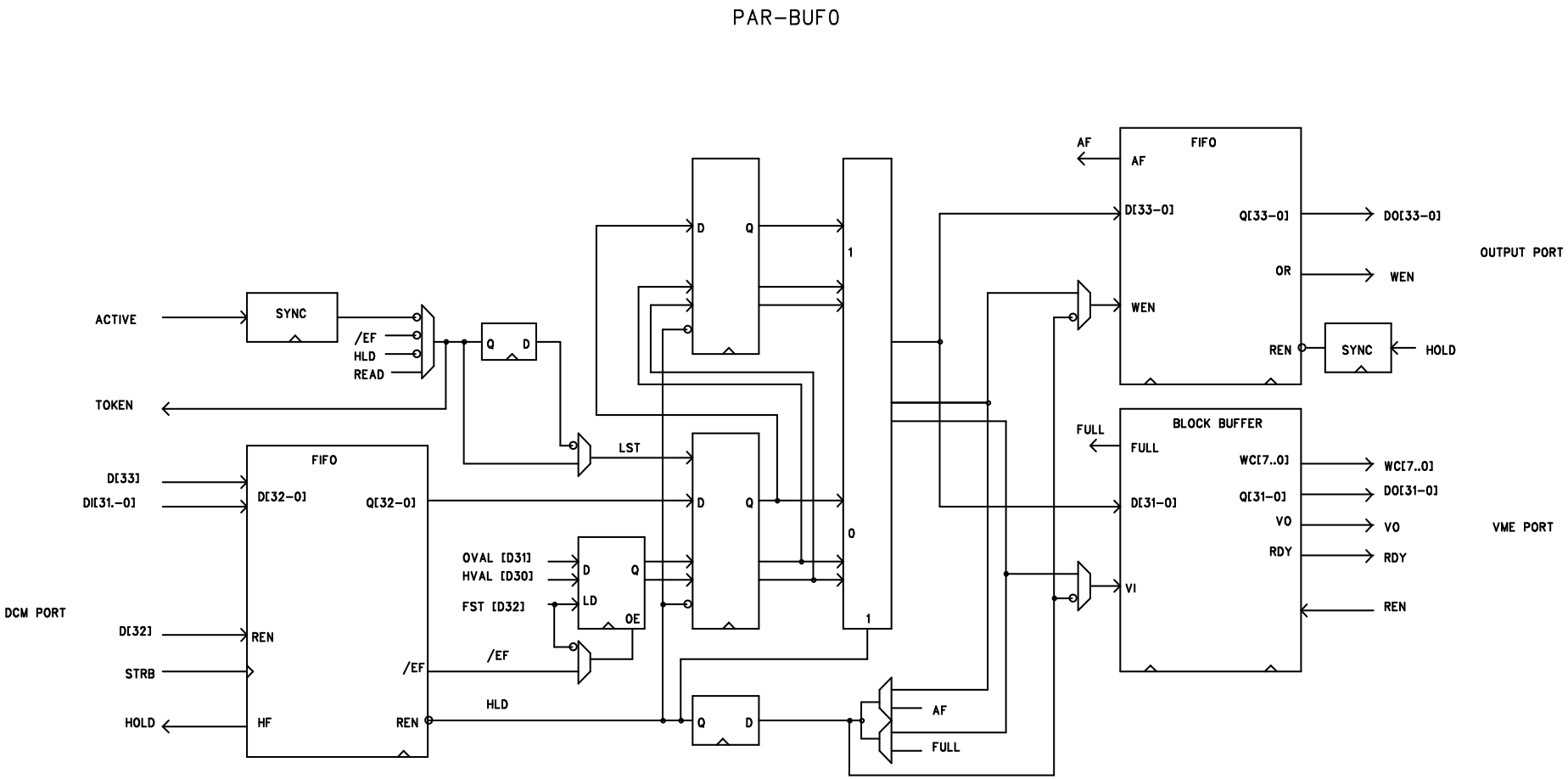
DCM Checking List

- GLINK error bits
- Reformat and check parity word included
- 4-bit word count and 4-bit event count in GLINK interface summary word
- Level-1 accept Event Number/Time Stamp comparison between Level-1 input and FEM data packet input
- DCM will report possible error to VME and keep going till...

Partition Module

- Collect data from DCM's
- Receive Level-1 Information.
  - 16 bits data, 1 strobe, 1 add. tag (20 MHz)
- Output to Sub-Event Buffer (SEB)
  - 32 bits data, hold, valid, last, nready
  - 40, 20, 10 MHz word rate
- BUSY to Timing System
- Data could be output to SEB and VME
- VME read via block mode with two page buffer

PARTITION MODULE BUFFER BLOCK DIAGRAM



par

DCM Test Result (part 1)

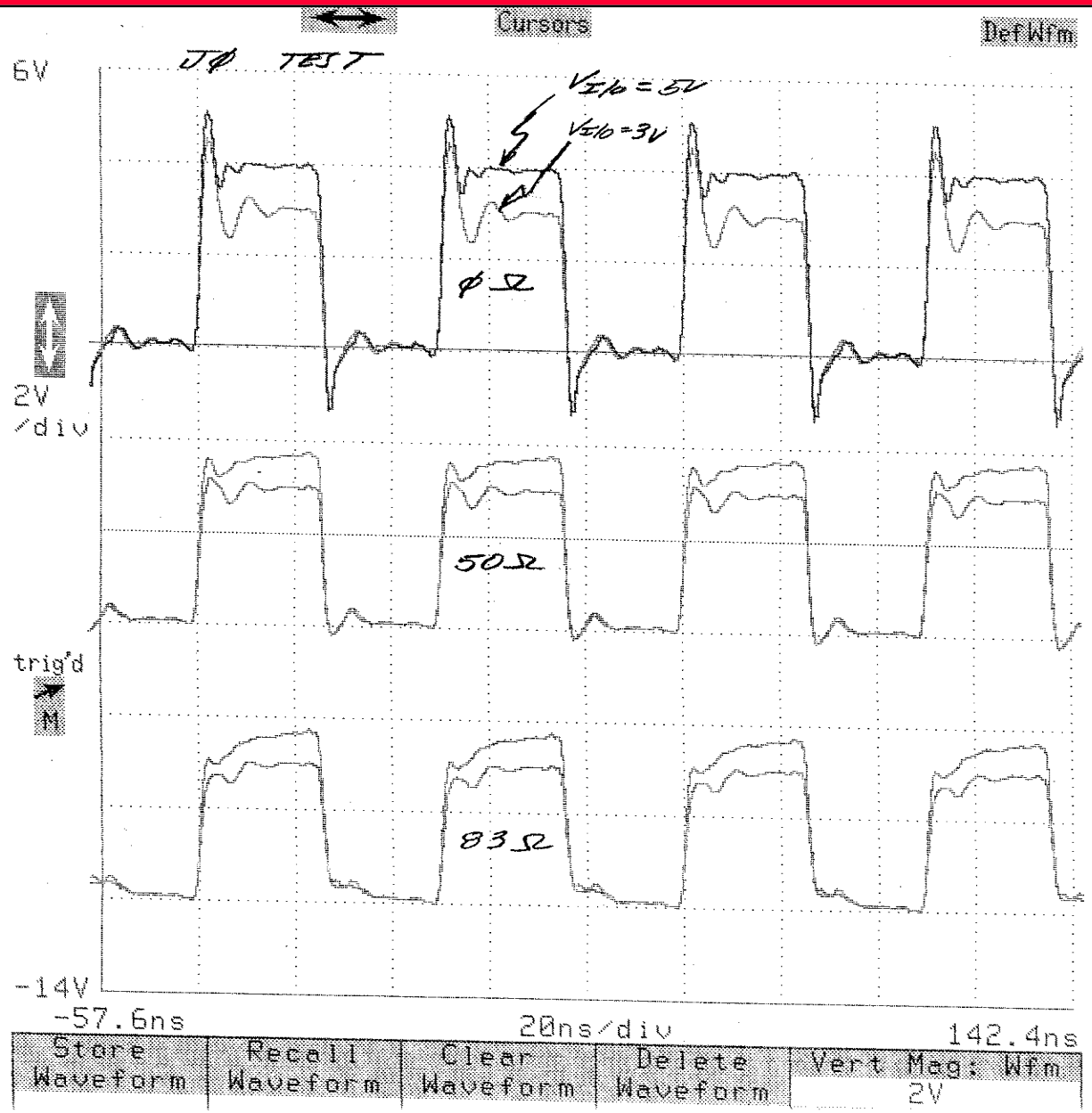
Early prototype results

Prototype Summary

Early Design Prototype

- DSP Test Board
  - Study DCM I/O bus sharing
    - (between host port, link ports)
  - DSP booting and programming
- J0 Bus Test Board
  - Study whether we can run data output port at 40 MHz

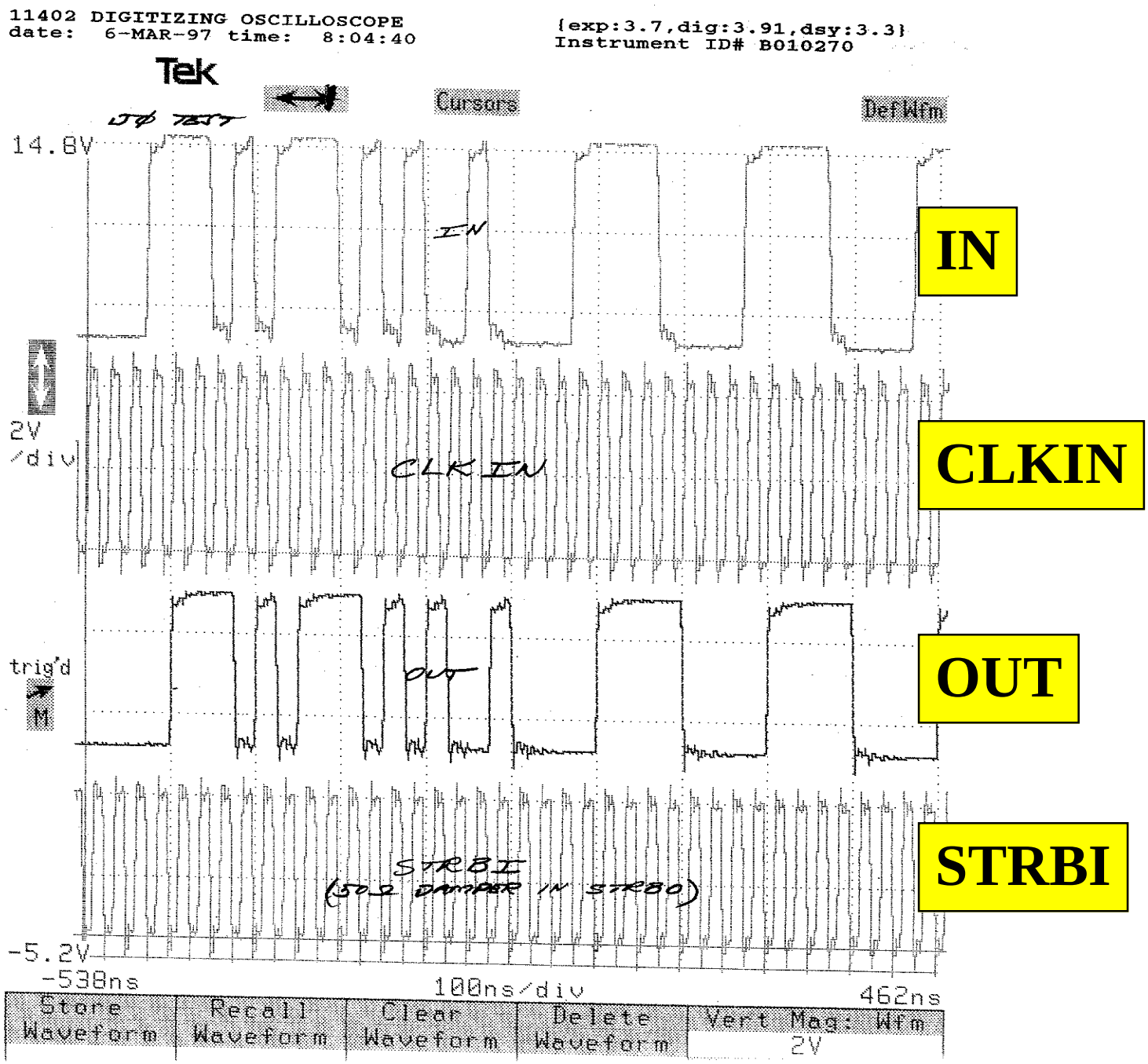
Clock line with different serial termination

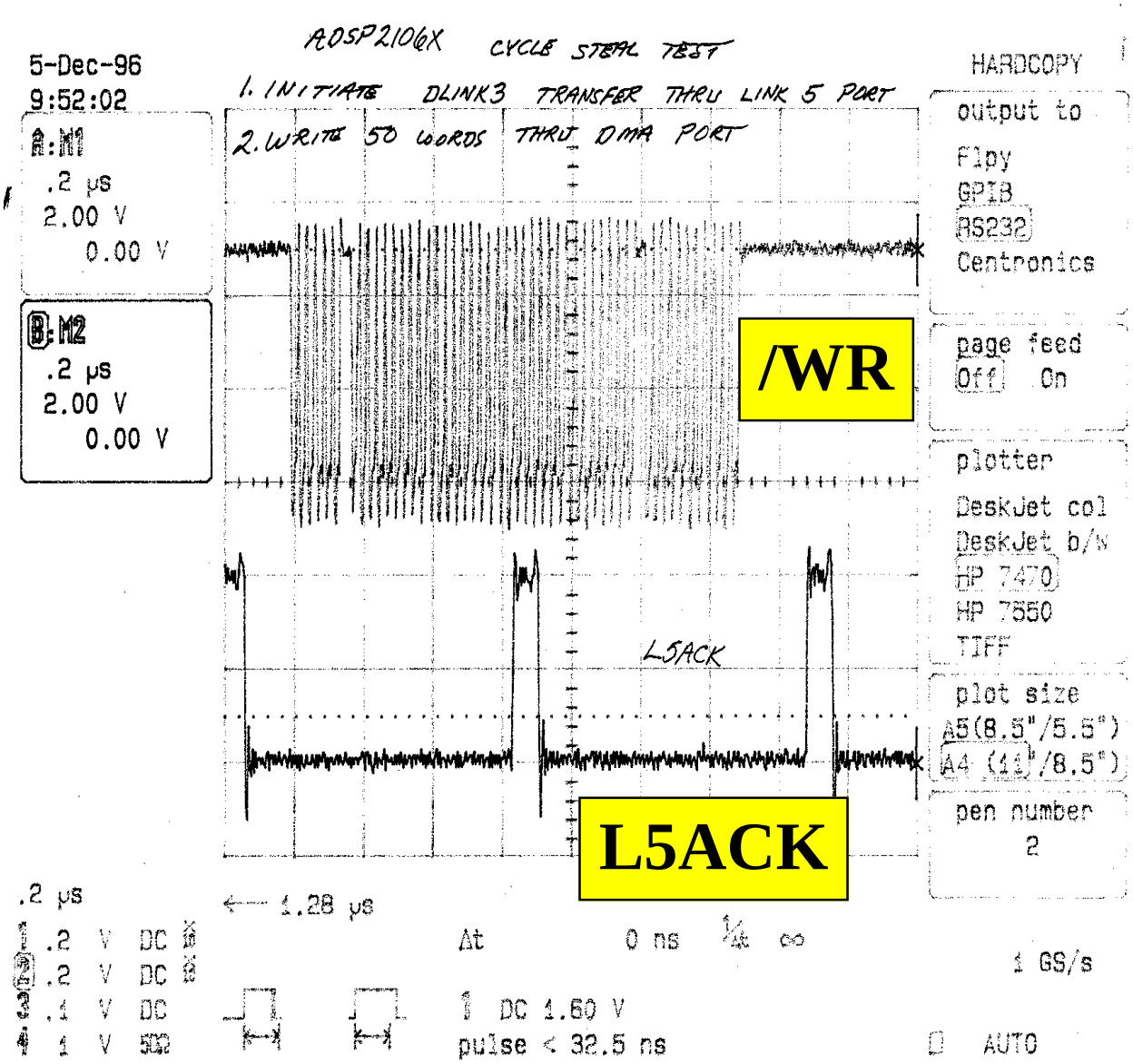


0 Ohms

50 Ohms

83 Ohms


11402 DIGITIZING OSCILLOSCOPE
date: 6-MAR-97 time: 8:04:40
{exp:3.7,dig:3.91,dsy:3.3}
Instrument ID# B010270
Tek
Cursors
DefWfm
14.8V
IN
IN
2V
/div
CLK IN
CLKIN
trig'd
M
OUT
OUT
STRBI
(50Ω DAMPER IN STRBO)
STRBI
-5.2V
-538ns
100ns/div
462ns
Store Waveform
Recall Waveform
Clear Waveform
Delete Waveform
Vert Mag: Wfm
2V


ADSP2106X CYCLE STEAL TEST
1. INITIATE DLINK3 TRANSFER THRU LINK 5 PORT
2. WRITE 50 WORDS THRU DMA PORT
5-Dec-96
9:52:02
A: M1
.2 µs
2.00 V
0.00 V
B: M2
.2 µs
2.00 V
0.00 V
/WR
L5ACK
L5ACK
HARDCOPY
output to
Flpy
GPIB
RS232
Centronics
page feed
Off On
plotter
DeskJet col
DeskJet b/w
HP 7470
HP 7550
TIFF
plot size
A5(8.5"/5.5")
A4 (11"/8.5")
pen number
2
.2 µs
← 1.28 µs
1 .2 V DC
2 .2 V DC
3 .1 V DC
4 1 V 500
Δt 0 ns
1 GS/s
DC 1.60 V
pulse < 32.5 ns
AUTO

Prototype Built

- 10 DCM mother boards
  - (3 populated at different levels for testing purpose)
- 10 AMU type compressor daughter cards
  - (2 fully populated)
- 10 T & D type compressor daughter cards
  - (1 populated, in testing stage)
- 2 semi-custom VME64X backplane ordered
- 1 VME64X crate
- 2 VME64X standard backplane

Prototype boards size & layers

- DCM board is 8 layers 6U by 280 mm
- Compressor boards are 4 layers

  5.6 in by 2.05 in

FPGA Usage Summary

Function	Type	Total LC	% LC used	Unused Pins
DCM-VME	EPF10K10208-3	465	80%	5
DCM-OUT	EPM7192SQC160	119	61%	3
Comp. A	EPF10K20QC208-3	684	59%	13
Glink-Inter	EPF8452AQC160-3	288	67%	Lots
Comp. B	EPM10K20TC144-3	542	47%	Lots
L1 Input	EPM7128SQC160-7	120	93%	1

SUMMARY/COST

Summary I

- DCM mother boards in very good shape. We have been using the boards for several months with two different people
- DCM main board has only two mistakes, (address lines swapped and missing one power pin on FPGA)
- Level-1 input port has been exercised including VME downloading

Summary II

- Compressor board A: All aspects of serial downloading works. We can download fake data, G-link data. It all works. Although zero suppression inside FPGA has not been tested yet, we do not foresee any problems.
- Although there is no difference in sending data from FEM or pattern generator (HP82000), we would still like to see TOF interface talk to DCM. It should not be viewed as a problem to approve purchasing the components.

Cost

- DCM board cost $**3.8K** under assumptions:
  - optical transceiver ($150)
  - DSP cost ($250)
  - this cost assumed purchase of 500 boards
- VME64X Backplane
  - **$2.6K** each for quantity of 10 backplanes
- Partition Module
  - **~$2K** each

Leo's DCM(B) Counts

Subsystem	# of DCMs	# of DCBs Day N	** Day 1	*** Eng Run
BB	2	1	1	1
MVD	136	34	17	17
DC	160	40	20	10
PC	96	24	12	6
TEC	496	124	62	16
PbSc	112	28	14	5
PbGl	68	17	9	9
RICH	32	8	4	2
TOF	16	4	2	2
MuTr	450	113	57	27
Muid	4	1	1	1

How many DCM to build?

- We have a plan with DC/PM with agreement on how many DCM boards to build.
- We will take a first cut on that soon, hopefully with help from John and Glenn.
- When DC/PM looks over these numbers, we should start buying parts, pending the blessing of this committee.

Future Test Plan

- Link with TOF crate interface (almost done)
- Finish up Compressor Board T testing.
- Test Backplane and Partition Module.
- ONCS should have a DCM around Feb. PHENIX collaboration meeting….
- Finish population of existing boards? (6)