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Nuclear Physics A661 (1999) 665c–668c

NUCLEAR PHYSICS A

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The pixel readout system for the PHENIX pad chambers

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A new concept for two-dimensional position readout of wire chambers is described. The basic idea is to use a cathode segmented into small pixels that are read out in specific groups (pads). The electronics is mounted on the outer face of the chamber with a chip-on-board technique, pushing the material thickness to a minimum. The system described here, containing 210 000 readout channels, will be used to read out the pad chambers in the PHENIX experiment at the Relativistic Heavy Ion Collider (RHIC).

1. Introduction

The difficulties of charged particle tracking increase with increasing multiplicity. In central Au+Au collisions at RHIC one expects to have a very high particle density which requires tracking detectors with good two-track separation capability, from which three-dimensional position information can be obtained. This can be achieved with a series of wire chambers equipped with the electronic readout scheme described below.

2. The pad chambers

The three layers of pad chambers in the PHENIX experiment provide three-dimensional coordinates along the charged particle trajectories in the field free region. The total area of the pad chambers in the central tracking arms exceeds 100m^2. Their main function

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PII S0375-9474(99)00545-X

is to ensure reliable pattern recognition in the high-multiplicity heavy ion collisions at RHIC.

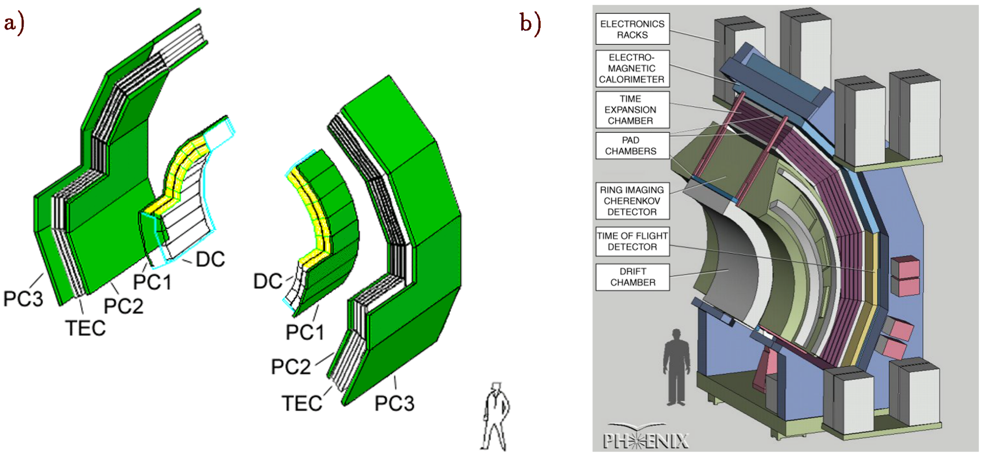

Figure 1. a) A cut view of the pad-, drift- and time expansion chambers in the PHENIX experiment. b) A central arm with all chambers shown.

The first layer, called PC1, has 8 chambers in each arm of multi-wire proportional chambers (MWPC:s, fig. 1). PC1 is placed immediately behind the drift chamber (DC) and in front of the ring imaging Cherenkov detector (RICH). PC2 and PC3 are placed behind the RICH, on both sides of the time expansion chamber (TEC). PC2/TEC/PC3 form the outer tracking unit which links track segments from particles found in the inner tracking unit (DC/PC1), that traverse the RICH and extend to the electromagnetic calorimeter (EMCal) and the time-of-flight detector (TOF).

3. The pixel layout

A new pad geometry for a cathode readout of MWPC:s has been designed [1]. The basic component is a pad consisting of nine smaller connected copper electrodes, called pixels (fig. 2a). The entire pad is read out by one single preamplifier and discriminator. The pads are interleaved with each other in a repeated pattern (fig. 2b). The group of three adjacent pixels belonging to three different pads is called a cell. This arrangement saves a factor of three in the number of readout channels with marginal loss of performance as compared to readout of individual pixels.

The side pixels (next to the wire) are somewhat larger than the center pixels (over the wire), that are closer to the avalanche. Thus the side pixels and center pixels collect approximately equal fractions of the avalanche charge.

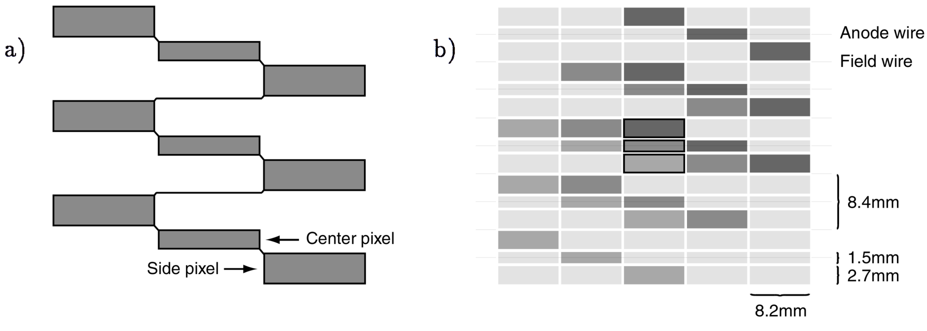

Figure 2. a) The nine connected pixels forming a pad. b) The three outlined pixels in the center, each belonging to a different but adjacent pad, constitute one cell. The dimensions are for PC1.

4. The pixel readout system

The pad chambers are read out by the induced signals sensed on the cathode pads. The demand that three neighboring channels have to fire to form a valid hit, makes the system highly immune to noise even at low thresholds. The digitizing concept is to analyze each channel against a discriminator threshold resulting in a one bit output. A system using a readout on a yes/no basis gives a position resolution similar to the cell size.

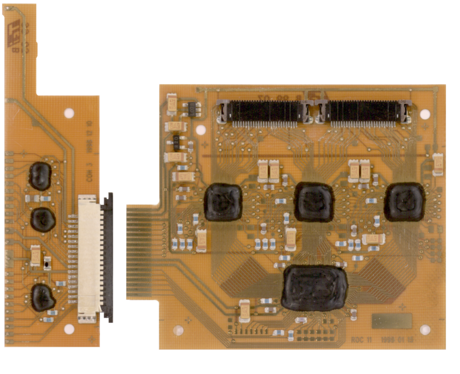

Figure 3. The readout card (right) along with its connector card (left). The connector card is soldered onto the motherboard, i.e. the upper layer of the sandwich on the backplane of the chamber.

The small pixel size gives rise to a high density of channels. The full system has approximately 210 000 readout channels which requires the electronics to be mounted directly on the detector. This is accomplished by mounting the readout cards (ROC:s), containing preamplifier-discriminator and digital memory chips, on the backplane of the chamber (fig. 3). Particles will pass through these cards, so a minimal mass of the ROC is a primary requirement of the design.

Two new integrated circuits were developed for the front-end electronics (FEE), one analog and one digital. The analog chip (TGL) has 16 channels of charge sensitive amplifiers followed by a leading edge discriminator. The charge gain is 10mV/fC with a noise performance given by $590e^- + 32e^-/pF$. This corresponds to 800-900e^- on PC1. The total power consumption is 6mW per channel and the discriminator is adjustable down to 1.5fC. Individual channels can be turned on/off, and each channel can be internally pulsed with variable amplitude. The test pulse generator is located on the chip and all functions of the chip are digitally controlled via a serial control interface.

The current driven discriminator output is received by a digital memory unit (DMU), that stores all data during the latency of the first level trigger (ca 40 beam crossings) and provides local storage of five events, pending readout.

Three TGL:s and one DMU, placed on each ROC, handle 48 channels. The circuit board material is 100 microns thick polyimid with the chips mounted as naked dice, bonded directly to the circuit board with the chip-on-board technique. The total weight of each ROC is 4g and the size is 5x6cm^2. The average thickness of the ROC is 0.2% of a radiation length.

The pads are connected to the amplifier inputs via short kapton cables that run through the honeycomb structure of the chamber. Nine readout cards are connected to a common bus. The communication between the readout cards and the front-end modules (FEM) placed at each end of the chamber is done by differential RS485 signals. The signals are translated into CMOS signals in three receiver chips on the connector card which is soldered onto the chamber. Each FEM provides power and control signals and collects data from 5x9 ROC:s. It also checks parity and event number consistency. The data is formatted into 20 bit words with a total of 108 words per FEM. The output data block is a direct map of the pads in the chamber, and is sent with a 1Gbit/s fiber optical link to the main data acquisition.

A full scale system was successfully tested at a discriminator threshold setting of 2fC.

5. Acknowledgments

We thank the technical staffs of the participating institutions for their vital contributions. The detector construction project is supported by the Department of Energy (USA), NFR and the Knut and Alice Wallenberg Foundation (Sweden), MIST and NSERC (Canada), and by a Grant No. 97-00088 from the United States-Israel Binational Science Foundation (BSF), Jerusalem, Israel and by a Research Grant from the Fusfeld Research Fund (Israel).

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