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A HIGH SPEED FASTBUS INTERFACE TO VME
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Abstract

A FASTBUS crate segment master has been developed to acquire data from front end FASTBUS slave modules into a Silicon Graphics 4D/320 [1] UNIX computer system. Data are transmitted via Branch Bus [2] to modified commercial VME modules which are used for single word and block transfers to the computer's memory. A kernel level device driver has been developed to allow DMA transfers to the machines memory. A maximum transfer speed of about 17 Mbyte/sec has been observed for long block transfers.

I. Introduction

A new interface emphasizing high speed block transfers has been built from FASTBUS and VME to VME-based computers. A FASTBUS master was designed for Brookhaven AGS Experiment 787, and is also used by AGS Experiment 852. A device driver and high level software running on Silicon Graphics 4D servers and workstations has been developed and used in these experiments.

II. Computer Interface

Three VME slots are needed in the computer for the interface modules, which are modified interface modules developed by the FERMILAB ACP project, [2] and purchased from Omnibyte Corporation, [3] which produced them commercially. The first is the VBBC, which is the controller for non-DMA transfers, and is used to perform the initialization for DMA transfers. The second is the VBVI, which is the controller and VME master for DMA transfers. The daughter-boards which provide the electrical interface to Branch Bus have been modified slightly in order to make possible faster DMA transfers. A hardware switch on the VBBC daughter-board is provided for selecting DMA or non-DMA transfers. The third is a Branch Bus terminator module, which uses the VME backplane only for power.

We have also operated this interface using a VME bus extender, with some performance degradation, but this has allowed us to use the interface from a workstation with a single VME slot, and to more easily debug the modifications to the VME modules.

Figure 1 shows how the interface modules are connected to the Silicon Graphics 4D/320S system which is being used to acquire data. Outside the computer, the BBFC developed here is used to provide a connection to FASTBUS, and the commercially available (and unmodified) external VBVI provides a connection to remote VME.

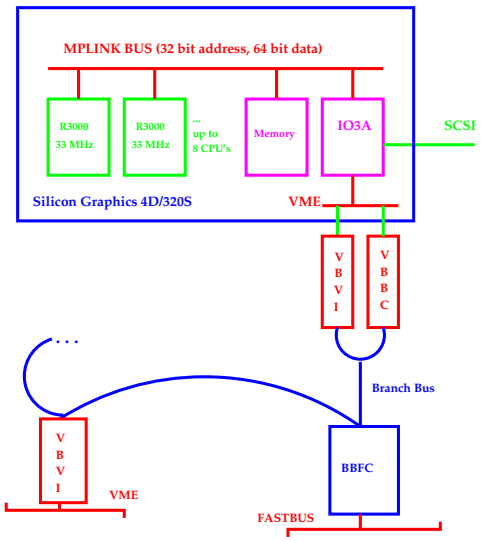

Fig. 1. This block diagram shows how the FASTBUS interface (BBFC) is connected to a Silicon Graphics acquisition computer.

III. FASTBUS Master

The FASTBUS module which we developed to interface to FASTBUS is called the BBFC (for Branch Bus to FASTBUS Controller). This module is FASTBUS master, and a Branch Bus slave. Since the Branch Bus standard has a crate number, many BBFC's can be connected to a single computer, which can then communicate with any of them directly.

To transfer data in non-DMA mode, the VBBC simply carries out a conventional Branch Bus cycle, and the BBFC responds as a conventional Branch Bus slave to transfer data through the VBBC to the VME destination address.

To transfer data in DMA mode, the VBBC initiates the transfer by loading the destination VME address and word count into the VBVI, then loads the origin FASTBUS secondary address and word count into the BBFC. The VBVI

then initiates the transfer by pushing data as fast as possible into the VME memory (which is mapped by a software driver to the main memory, in the case of the Silicon Graphics 4D/320 system).

Transfer errors were signaled using the Branch Bus error line. Since there is a wide variety of FASTBUS errors, a register in the BBFC was accessible (using spare control bits) to completely decode the FASTBUS error. Another control bit allowed reading the value of the Service Request line, so that polling the SR could be used to synchronize activity in the FASTBUS crate with the acquisition program.

Physically, this board is a single width FASTBUS module, fabricated with 8 layers (2 signal layers) using TTL F series logic.

IV. Software

A kernel level device driver was developed from one written by M. Iseley at FERMILAB for a similar application. This driver supports both DMA and non-DMA transfers.

A library of diagnostic routines developed with the use of this module in data acquisition which used a user level library of a restricted set of IEEE FASTBUS Standard Routines (IEEE Std 1177-1989). These routines provided single word and block transfers from control and data space, which were found to be the only operations specifically required for the experiment's data acquisition architecture.

A library of higher level routines using the SLAC designed SSP [4] to emulate the Segment Interconnect in software, which had been developed for a VAX/VMS system, was ported with minimal difficulty.

V. Performance

We measured the transfer speed of the interface by observing the data strobes during a transfer. On non-DMA transfers, we observed a 1.8 Mbyte/sec speed on Input Block Transfers (reading data into the computer), and 2.0 Mbyte/sec on Output Block Transfers to SSP memory. On DMA transfers, we observed 17.6 Mbyte/sec on input, and 11.8 Mbyte/sec on output to an SSP. These speeds are consistent with Branch Bus speed and the FASTBUS slave response time. The system overhead is relatively low: timing 1000 0.5 Mbyte transfers gives an average input transfer speed of 14.2 Mbyte/sec.

VI. Acknowledgements

We wish to thank the FERMILAB ACP group for their help in understanding Branch Bus, and particularly Michael Iseley for giving us a similar device driver from which we could develop our own. We would also like to thank M. Van Lith and P. Bichoneau for their help in fabrication.

VII. References

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