A Large System of 500 MHz Transient Digitizers

M.S. Atiya, J.S. Haggerty, M.M. Ito, C. Ng
Brookhaven National Laboratory, Upton, NY, USA, 11973
F.W. Sippach
Nevis Laboratories, Columbia University, Irvington, NY, USA, 11530

ABSTRACT

We have constructed a system of 300 channels of 500 MHz, 8 bit solid-state transient digitizers for a rare kaon decay experiment at Brookhaven National Laboratory (AGS E787). The system has several features, which make it interesting for present and future high rate collider machines.

1 Introduction

The digitization of analog signals from standard high energy physics detector elements has often enriched our understanding of the devices generating the signals and frequently improved the performance of these systems through more thorough software analysis of the data. In a small class of experiments (ours included) such digitization is vital for extracting physics information unavailable through other readout means. In future high rate experiments at colliders such digitization will play a central role in pipelined systems necessary for high speed triggering and data acquisition. For example in the SSC with 16 nsec beam crossing time it will be necessary to store detector information in a pipe until the trigger and readout systems are ready to handle the data. The traditional means of storing the information in a long timing cable are not viable both because of the large number of elements and the desire to minimize the number of cables in the detector. Storing the analog, or digitized analog, information in a pipe is an efficient means of handling high-rate data in a parallel time-independent and event-independent fashion.

In this note we describe a system of 500 Msample/sec, 8-bits waveform digitizers (transient digitizers) used in Brookhaven National Laboratory (BNL) experiment E787 to observe the decay sequence $\pi \rightarrow \mu \rightarrow e$ in scintillator. The system is extendable to even larger number of channels and has several features judged vital to high rate experiments such as zero-suppression prior to write, deep memory, fast readout in a standard format (FastBus) as well as access to front-end high speed computing for data compaction and on-line trigger decisions.

2 Physics objectives

BNL experiment E787 is designed to study the decay $K^+ \rightarrow \pi^+\nu\overline{\nu}$ to the level of 2×10^{-10} in branching ratio. Figure 1 shows an outline of the detector. Low energy kaons (750 to 800 MeV/c) from a separated secondary beam are degraded by a Be degrader and stopped in a 2000 element (of 2 mm each) fiber target. The charged decay products are momentum analyzed in a cylindrical drift chamber (σ=2.5%) and stopped in a 15 layer, 24 azimuthal sectors, scintillator range stack. A high rejection photon veto (lead-scintillator) surrounds the detector in both the barrel and endcap regions. A 1 Tesla solenoidal coil surrounds the entire detector and a thick iron yoke barrel and endcaps provide excellent flux return.

While it is not the purpose of this note to provide a detailed description of the detector or the physics, it is useful to give a brief outline of background rejection mechanisms. Roughly speaking the major backgrounds are $K^+ \rightarrow \pi^+\pi^0$ and $K^+ \rightarrow \mu^+\nu$. The former is rejected by a combination of vetoing the photons of the π^0 (rejection factor of 3×10^{-6}) and by working with charged pions above the $K_{\pi 2}$ charged pion momentum of 205 MeV/c. The latter background's rejection depends on a combination of range/momentum/energy analysis and the observation of the decay sequence of the stopped charged track in the range stack. The primary pion

will decay into a mono-energetic muon and a neutrino, with the secondary muon in turn decaying into an electron and two neutrinos, while the primary muon will decay directly into an electron and two neutrinos. In order to observe the decay sequence in the scintillator one needs a device capable of digitizing the photomultiplier signals with sufficient performance. There are roughly 800 PMT channels and the summing of more than 4 PMT channels into one digitizer is undesirable from the point of view of random background rate and signal degradation. The parameters of the decay sequence set the performance scale of the digitizers:

- Since the typical signal is 30-40 nsec wide at the base and the pion lifetime is 26 nsec, one needs sampling rate of upward of 300 Msamples/sec to be able to detect early decays (less than 10 nsec). The detection of those decays is vital to having an overall large acceptance for pions.

- Since the muon lifetime is 2.2 μsec one needs a memory depth of at least 10 μsec to insure high efficiency for the detection of the muon decay.

- The energy of the stopping pion ranges from 1 to 30 MeV while the decay muon is always 4 MeV in energy. In order to observe the muon with sufficient resolution and still have a small number of pion overflows it is necessary to have a dynamic range of at least 7 bits.

- The experiment is designed as a high rate, high statistics experiment. In order not to compromise the basic design of the data acquisition system, one needs a suppression of the large number of zero points prior to writing. This also insures a fast readout of the overall system.

Our final design of the 500 Msample 8 bit system achieves all the above goals. Figure 2 shows a block diagram of the basic digitizing channel. It consists of four parts: the flash A/D converter, the custom data handling chip, fast ECL 256 x 4 memories and data acquisition/readout protocol electronics.

3 The Flash A/D

In choosing the basic digitizing technique flash A/D' s typically offer a somewhat lower dynamic range than charge coupled devices (CCD) or analog memory devices. However, they offer the distinct advantages of having the ability to subtract zeros prior to writing and of generally faster access to the data, as well as the possibility of a large depth of memory (or pipe). Our choice for the task was a Tektronix A/D converter hybrid TKAD508 consisting of a 500 Msample/sec Sample-and-Hold circuit and two interleaved 250 Msample/sec A/D converters. The hybrid with all 3 IC's comes in a standard 84 pin flat pack with 7 watt power consumption. Figure 3 shows a basic block diagram of the Sample-and-Hold system and the A/D. The Sample-and-Hold has two differential inputs, both with 50 Ω internal termination and 1 pF shunted

input capacitance. The clock is driven differentially at 500 MHz. The Sample-and-Hold drives the two 250 MHz A/D's and supplies the necessary clocking and buffering. Two references (V_+ and V_-) must be externally provided for each A/D. The output of the hybrid is a pair of interleaved bytes of data at a rate of 250 MHz. One byte is output on the rising edge of the clock, while the other is output on the falling edge of the clock. The device is capable of 7.2 effective bits performance at 100 MHz, at 6.8 effective bits at 250 MHz input frequency.

We use the two analog inputs in a non-standard fashion. Since our signals are all of one polarity (negative), we input the analog signal on one side and a DC level generated by the 12 bit Digital-to-Analog converter (DAC) on the other side. This allows a software settable threshold of .25 mV sensitivity while the digital threshold cut is at a fixed count of 7. This flexibility is necessary since standard PMT signals are transported on RG8X and RG58 cables and can acquire small voltage shifts. The shifts can be disastrous in the sense that they push all signals above the zero suppression cut and cause a huge increase in the amount of data generated by the device. DAC level corrections to the signals effectively eliminate this problem as well as provide an efficient means of on-line testing and calibration. This method of using the device provided a full scale voltage of 1 Volt.

The output rate of the flash A/D of 2 bytes at 250 MHz renders it difficult to deal with since no standard memory runs at such a fast rate. Also, as mentioned earlier, it is desirable to do zero suppression prior to writing in memory. We opted to design a semi-custom IC to handle both the speed of the data and zero suppression, as well as the various housekeeping and digital readout duties required in such a device. The IC (BNL787TD) is commonly called the Macro-Cell and is described in the next section.

4 The Data Handler(Macro-Cell)

The custom-designed IC BNL787TD is a time demultiplexer capable of handling input data rates of up to 400 MHz (it normally runs at 250 MHz) with power consumption of 12 watts. It is implemented in Signetics ACE2200 current mode logic technology and has roughly 2150 gate equivalent. Figure 4 shows a block diagram of the IC. In operation it has as input 2 bytes of data and a synchronizing clock (pair differential). The output is 4 bytes of data at half the input frequency. In addition the IC generates two identical sets of 8 bits of memory address for controlling the external ECL RAM. Furthermore, the IC has an internal 8-bit counter (the TIMER) running at half the input clock frequency. The output of the TIMER is used as a tag for data words to define their relative timing. This, of course, is necessary because of the zero-suppression feature of the system. The zero-suppression is achieved by incrementing the memory address AFTER fulfilling one of the following conditions:

- At least one of the input bytes has a value greater than 7. In effect values below 7 are overwritten by the subsequent data word.

- The previous or subsequent byte in time has a value greater than 7. This insures that we detect full rather than a truncated pulse.
- The TIMER counter overflows. This allows a longer memory depth than afforded by the 8 bit timer (2 μsec). In fact the total memory depth is dependant on the occupancy rate of the data.
- Every time an external input line ($R/\overline{W}$) changes state from ECL low (write) to ECL high (Read). This allows synchronization of the data with external detector signals. Furthermore, when the ($R/\overline{W}$) line is in high state the memory writing is disabled, as this line is directly in control of the memory $\overline{WRITE}$ strobe. This allows a simple way of controlling the triggerability and the operation of the system in a standard high energy physics experiment.
- If an external line $\overline{EnableSuppression}$ is held in an ECL high state. This is a useful feature for debugging and testing.

The extension of the Timer data to greater than 2 μsec and the rearrangement of the data is done subsequent to readout, in software, at the crate level.

5 The External Memory

The external RAM must be fast enough (125 MHz or 8 nsec) to handle the Macro-Cell output data. We chose the Hitachi HM10422-7 256 x 4 ECL memory with access time of 4 nsec. The data word width is 48 bits (32 bits of data, 8 bits of time and 8 bits of flags to disentangle the 4 PMT to one channel sum) and one needs 12 such memories per channel (total power consumption of 12 watts). We operated the memory in a fashion where we do not strobe the write enable line, but rather rely on the fact that the data and address lines arrive at exactly the same phase in order not to corrupt the memory by writing to the wrong location. The address lines from the Macro-Cell must be generated with less than 200 psec skew and the printed circuit board layout has to insure similar performance. To reduce the load on the address line we organized the memories into two banks of 6 memories each (hence the two identical address line sets generated by the Macro-Cell). The entire memory system is placed on a separate printed circuit board which is plugged into the mother board via a set of connectors. This makes for easier construction and debugging.

6 Overall Organization

The system is organized into six FastBus crates each supporting up to 32 channels (see Figure 5). Each basic board is a double width FastBus module with 4 channels. Each FastBus crate also contains a single board (TDMASTER) which houses the 32 DAC level generators and is used to readout the data. Because of the bandwidth limitation and expense of FastBus, the data is readout by the TDMASTER from the 32 channels

over a special bus on the auxiliary backplane and transferred to the crate controller on the main FastBus backplane. The crate of 8 TD boards and the TDMASTER then looks logically to any crate master as a single board at the geographical location of TDMASTER and containing 32 channels of secondary addresses. In addition each crate houses a SLAC Scanner Processor (SSP) as a crate master and two 500 MHz clock fanout boards. Total power consumption on the crate is 240 A on the -5 V, 70 A on the -2 V, and 40 A on the $+5$ Volt and 1 A each on the $+15$ and -15 Volt lines. Cooling is achieved by forced air through water-cooled heat exchanger. The typical local temperature is 25 °C near any of the devices. The overall readout time for the crate is 100 microsecond (with no software analysis).

7 Crate-level Intelligence

A major drawback of such a high speed pipelined sampling system is the possibility of saturating any data acquisition system with a large volume of data. On the other hand the quality and immediate availability of the data make the system ideal for making on-line trigger decisions of reasonable sophistication. Crate-level intelligence is necessary to allow sophisticated on-line triggers and reduce both the volume of data and the the number of triggers per second. In our system we have two types of Crate-level intelligence. The crate controller (SSP) is a special purpose integer arithmetic computer with roughly 1-2 Mips of computing power. We also developed a special Front-End processor to handle the basic channel data prior to reading out by the SSP. This module, known as the Transient Digitizers Smart Controller or TDSC, uses an AMD 29K pipeline RISC processor with separate data, address and I/O busses and a compatible floating point co-processor. The TDSC with a processor running at 25-33 MHz basic clock rate is capable of 15-20 Mips of computing power. The TDSC uses standard C-language (or FORTRAN) software with a cross compiler available on both UNIX and DOS compatible systems.

8 System Performance

We operated 200 channels of the system between February and May of 1989. Roughly 20 million selected decays were recorded on tape. The transient digitizer system was used for both on-line trigger and off-line π/μ separation. Figure 6 shows a typical $K^+ \to \pi^+\pi^0$ event where the pion penetrated through several layers of counters, came to rest in one counter, decayed into a muon, and the muon subsequently decayed into an electron which, in turn, penetrated through several counters. The power of correlated time-pulse height measurements is clearly shown in such an event. On closer inspection on the pion pulse one can clearly distinguish the secondary muon pulse, measure its area and time. Figure 7 shows a trace of the data from a scintillation counter where decay pion has come to a stop. One can clearly see the primary pulse with the secondary muon decay. To separate pions from muons a fitting scheme is

used to test for how the data fits a single pulse or a two pulse hypothesis. Figure 8 shows a true pion pulse fitted to a pion and a muon hypothesis. From the fits one can extract the energy of the muon from the pion decay which has a unique energy of 4 MeV. Figure 9 shows the secondary muon pulse area. The curve shows a 15% energy resolution on the 4 Mev muon. This resolution is due to a combination of the basic resolution of the device and the software fitting scheme resolution. Reduction of random bakcgrounds is achieved by comparing the timing of the secondary and tertiary pulses relative to the primary pulse on both ends of the scintillation counter. Figures 10 and 11 show the timing distribution for standard $K^+ \to \pi^+\pi^0$ data for both the secondary pulse (muon) and tertiary pulse (electron). Figure 12 shows a distribution of the secondary pulse time relative to the primary pulse. The superimposed line represent the pion lifetime curve of 26.1 nsec. The dropoff in efficiency in very early times (8 nsec) costs only 25% in decay detection efficiency. The final π/μ rejection achieved using both the secondary and tertiary pulse detection was better than 10^{-4}.

9 Conclusions

We have constructed and successfully operated a large system of high performance transient digitizers in a demanding high-rate enviroment.

10 Acknowlegments

We thank members of E787 for their support and assistance. We also thank Mr M. Van Lith, Mr P. Bichoneau and Mr G. Munoz for their assistance in the design, construction and testing of the system. This research is supported in part by the U.S. Department of Energy under Contract No. DE-AC02-76CH00016.

List of Figures

Figure 1: The E787 $K^+ \to \pi^+ \nu \overline{\nu}$ detector

Figure 2: Block diagram of a single Transient digitizer channel. There are four channels to a double width FastBus board

Figure 3: Block diagram of the Tektronix TKAD508 Flash ADC

Figure 4: Block diagram of the data handling IC BNL787GS

Figure 5: Typical Transient Digitizer FastBus crate

Figure 6: A pion track stopping and decaying in the Range Stack

Figure 7: A trace showing $\pi \rightarrow \mu \rightarrow e$ decay

Figure 8: A fit to both muon and pion hypotheses for a stopping pion pulse

Figure 9: Pulse area spectrum for muons from pion decays

Figure 10: End-to-End timing for the muon from pion decay

Figure 11: End-to-End timing for the electron from secondary muon decay

Figure 12: Distribution of secondary pulse times showing the pion lifetime

Contents