

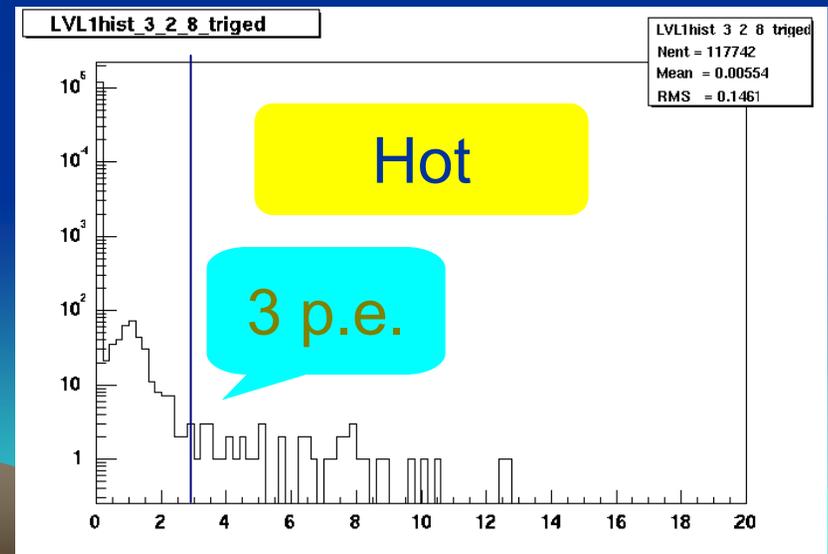
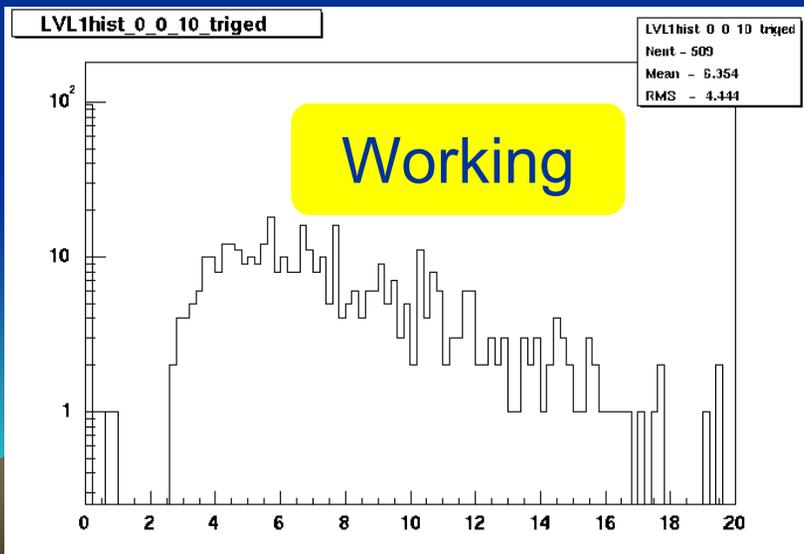
Status of RICH LVL-1 Working

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Problems in RUN 2

- In all 256 RICH LVL-1 tiles,
 - Working tile : 38 tiles (14.9%)
 - Noisy (Hot) tile : 74 tiles (28.9%)
→ Masked
 - No output (Dead) tile : 144 (56.3%)



What was done in Japan ?

- Debug of the problems.
 - Hot Modification of ECL bias for INT_R.
 - Dead Combination of 5 INT_R chips.
- New Selection of INT_R chips for RUN3.
 - Yield rate = 16.5 ± 0.552 % (more tight)
 - 1044 available chips (640 chips will be used).
- Spy board production.
 - For checking the Current mode sum signal.



Causes of hot & dead channel

- Hot channel
 - No trigger stop signal.(= The probable main cause)
 - Oscillation of base line by INT_R chips. (~ 1.0%)
- Dead channel
 - Differences of the bias voltage between 5 INT_R chips in some trigger tiles. (= The main cause)
 - RICH LVL-1 modules have some broken Op-amps. (~ 6.2%)



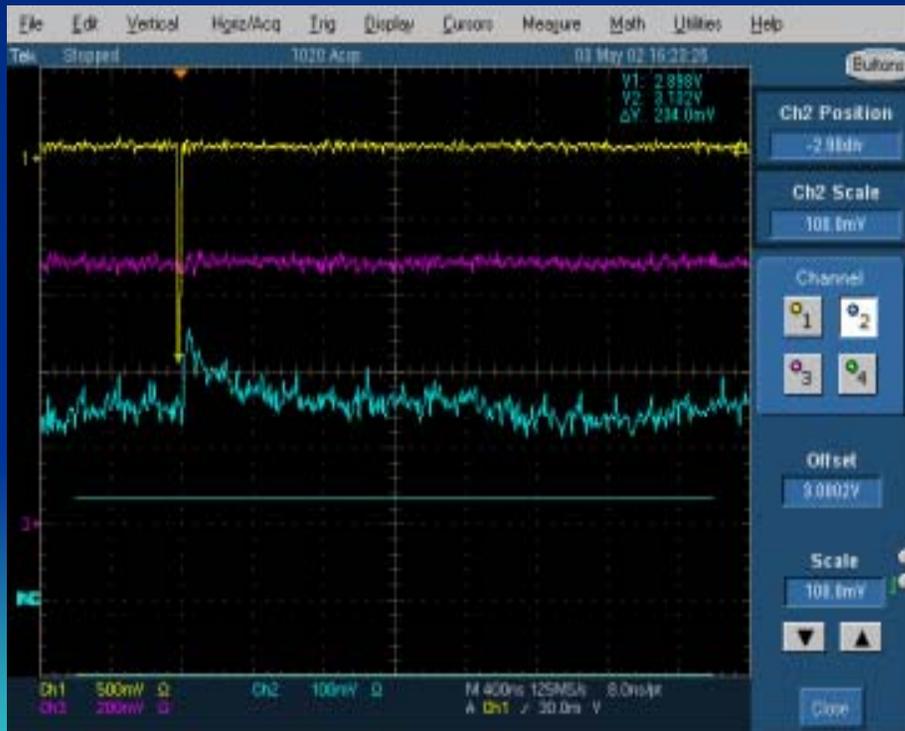
Status at BNL

- Present activities
 - 30/80 AMU/ADC modules have been modified.
 - New INT_R chips have been installed on modified AMU/ADC modules.
 - Analog current mode signals were confirmed in 312/340 PMT channels.
- Future plans
 - Checking digital outputs from RICH LVL-1 modules.
 - High voltage for PMT & Trigger ROC
 - Checking signal lines on back planes.
 - Checking Op-amps on RICH LVL-1 modules.

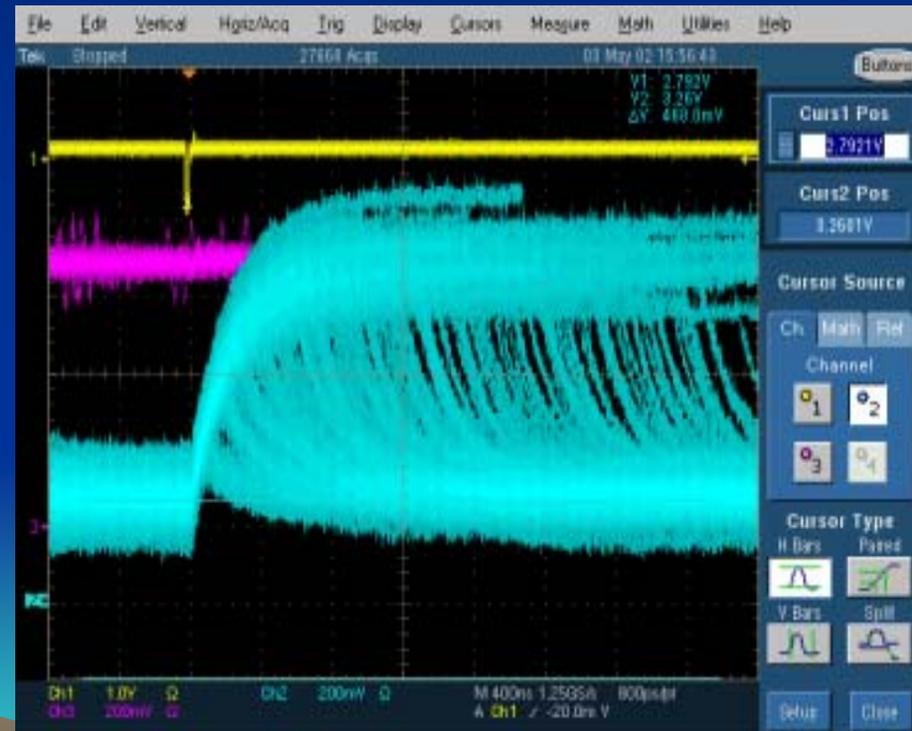


Signal on the Back Plane

Normal



Noisy



Oscillation of base line

In front of FADC

Base line
T ~ 200ns
A ~ 300mV

