EMC Trigger Summery from RunII and discussion for RunIII

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ERT Lvl-1 meeting

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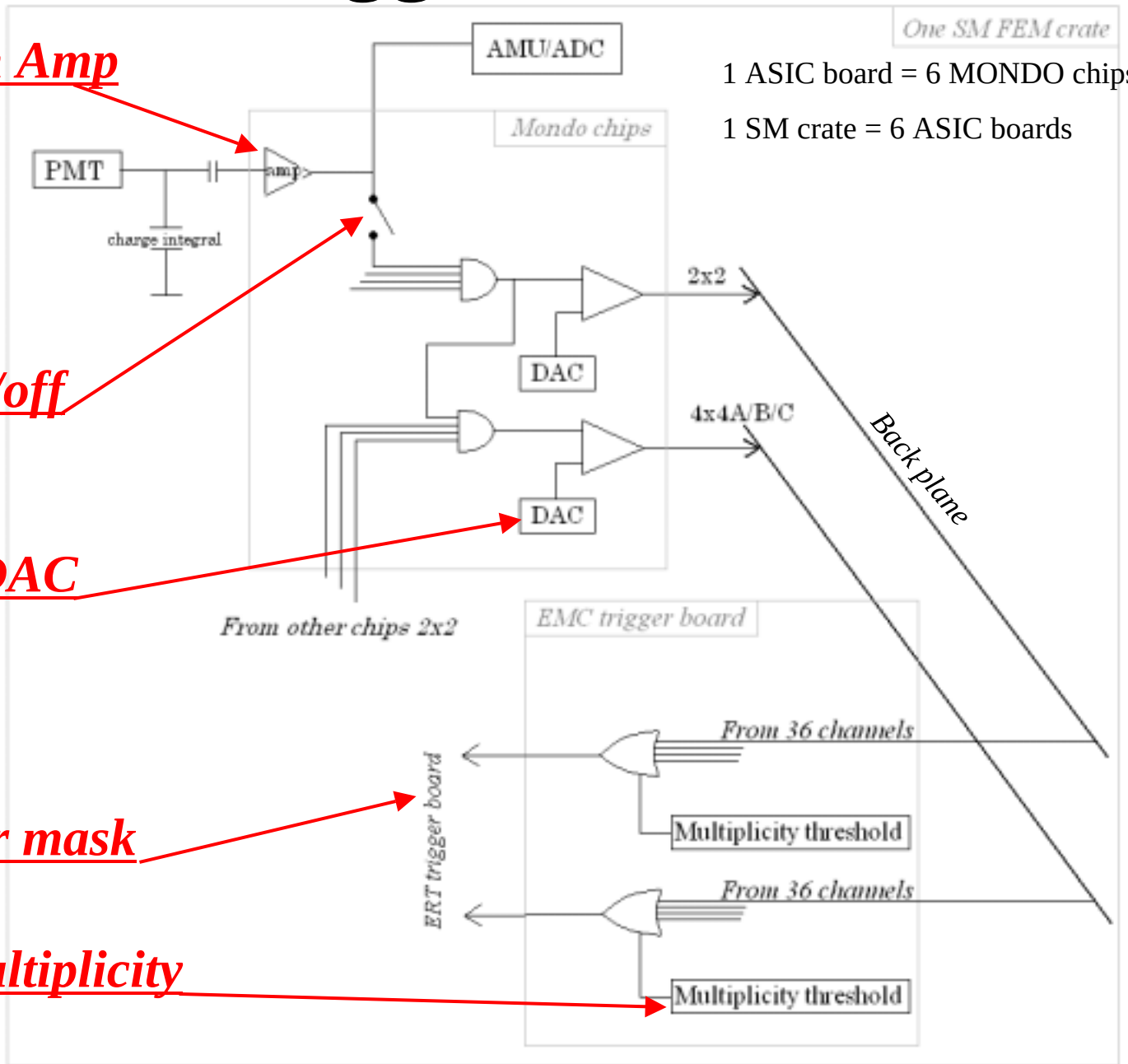
EMC Trigger Circuit



Variable Gain Amp

Switch on/off

Threshold DAC

ERT trigger mask

Multiplicity

1 ASIC board = 6 MONDO chips

1 SM crate = 6 ASIC boards

Trigger Board Prototype Test(2001/Jun)

- Test with 30 EMCal FEM boards + 2 EMCal trigger prototype boards
  - Those 30 boards had been rejected from installation, so the situation what I got through this test might be worse than what we have in PHENIX
- (0) Healthy offline readout.
  - Made 6 FEMs work correctly through ADC/TDC readout by tuning the several parameters. This needed some iterations, so it took an hour, kind of painful….
  - 2 channels were always fired , the trigger output looked always on through the oscilloscope → 8 multiplicity in 4x4 trigger
- (1) Noisy channel search
  - Set the multiplicity threshold of 9 and put the test signal into 36 inputs. If it's the noisy one, no trigger output would be seen.
  - (Fix) replace the boards
- (3) Trigger algorithm check (4x4 algorithm)
  - Put a test signal into 18 inputs (half of a SM) and find the minimum multiplicity threshold. 1 channel in the middle of SM had 2 or 3 multiplicity th.
  - (Fix) replace the boards
- (4) SM-to-SM connection check
  - Connected one cable between two SMs and put the test signal in the edge.
  - Could see a trigger output from next SM.

Summary of Prototype Test(2001/Jun)

- Some always-fired channels existed
  - Fixed by replacing the FEM boards.
- One channel showed wrong 4x4 algorithm
  - Fixed by replacing the FEM boards.
- Get a proof of the connection between two SMs
  - The 4x4 algorithm in the SM connection might be wrong.
  - The multiplicity threshold of 4 may results in strange behavior. Let’s set the multiplicity threshold 1.

Final Check before Installing EMCal Trigger Board(2001/Dec)

- Before installing all 172 trigger boards, we did a simple check of all the EMCal trigger boards
  - Put a test signal into one channels and check the output is there.
  - All the EMCal trigger boards passed the check.
- Observed some threshold behavior using installed EMCal trigger board

Threshold curve for c026 (W0, SM8)

	100ns for 10 sec	frecuency	107ns_ext frecuency	107_int frecuency	107ns_ext frecuency
15	14000000	1400000			
16	14000000	1400000			
17	14000000	1400000			
18	240000	24000	180000		
19	224	22.4	800	5	
20	80	8	2		4.5
21	60	6			
22	35	3.5			
23	25	2.5			
24	15	1.5			

During pp RunII : Switch off the Noisy Channels

- There were several noisy channels/SMs
- Make switch off for all 15525 channels
  - Took data in the force accept trigger.
  - The noisy channels looked to be remained still.
  - Didn't work to reduce the noisy SMs

→ The noise occurred after "switch on/off".
probably in the analog sum or the threshold circuit.

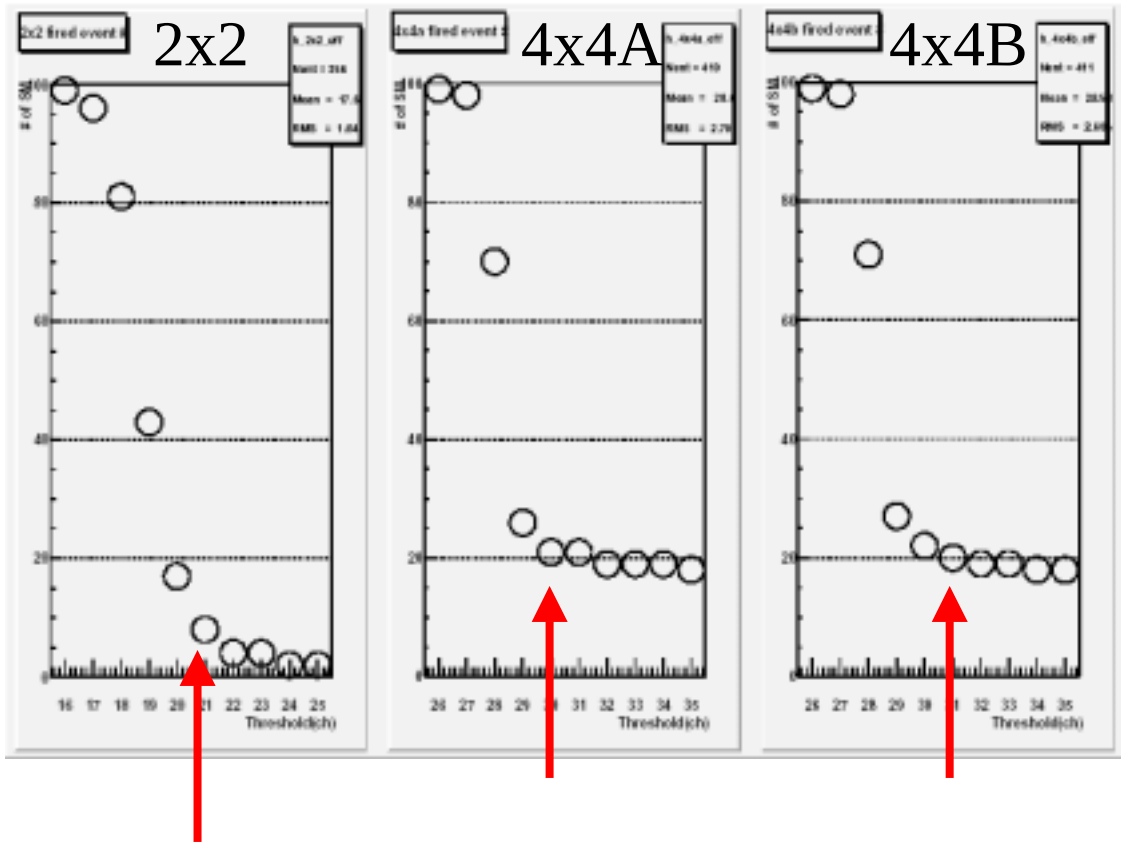
During pp RunII : Threshold Scan

- In January, before pp-run
  - To find a minimum threshold more than zero level.
    - The multiplicity threshold is 1 for all
  - 1000 events (10sec) with force accept mode. If at least one events had a trigger in a particular SM, we defined the SM as a ↯‘fired’↯ one.
    - The rigger is from 36 tiles(1 SM),
    - Count number of ↯‘fired’↯ SMs out of 172 SMs as a function of threshold
- The ↯‘fired’↯ is caused by
  - Noise
  - One tile with lowest threshold in the 36 tiles can be across the zero-level and

During pp RunII : Threshold Scan

- Final threshold value
  - 2x2 : 21 (0.15GeV)
  - 4x4A : 30 (2.1GeV)
  - 4x4B : 31 (2.6GeV)
- The ↯‘fired’↯ SMs at above threshold were masked off
  - 2x2 : 14 SMs
  - 4x4A : 37 SMs
  - 4x4B : 48 SMs
- The ↯‘fired’↯ SMs were remained in the higher threshold setting

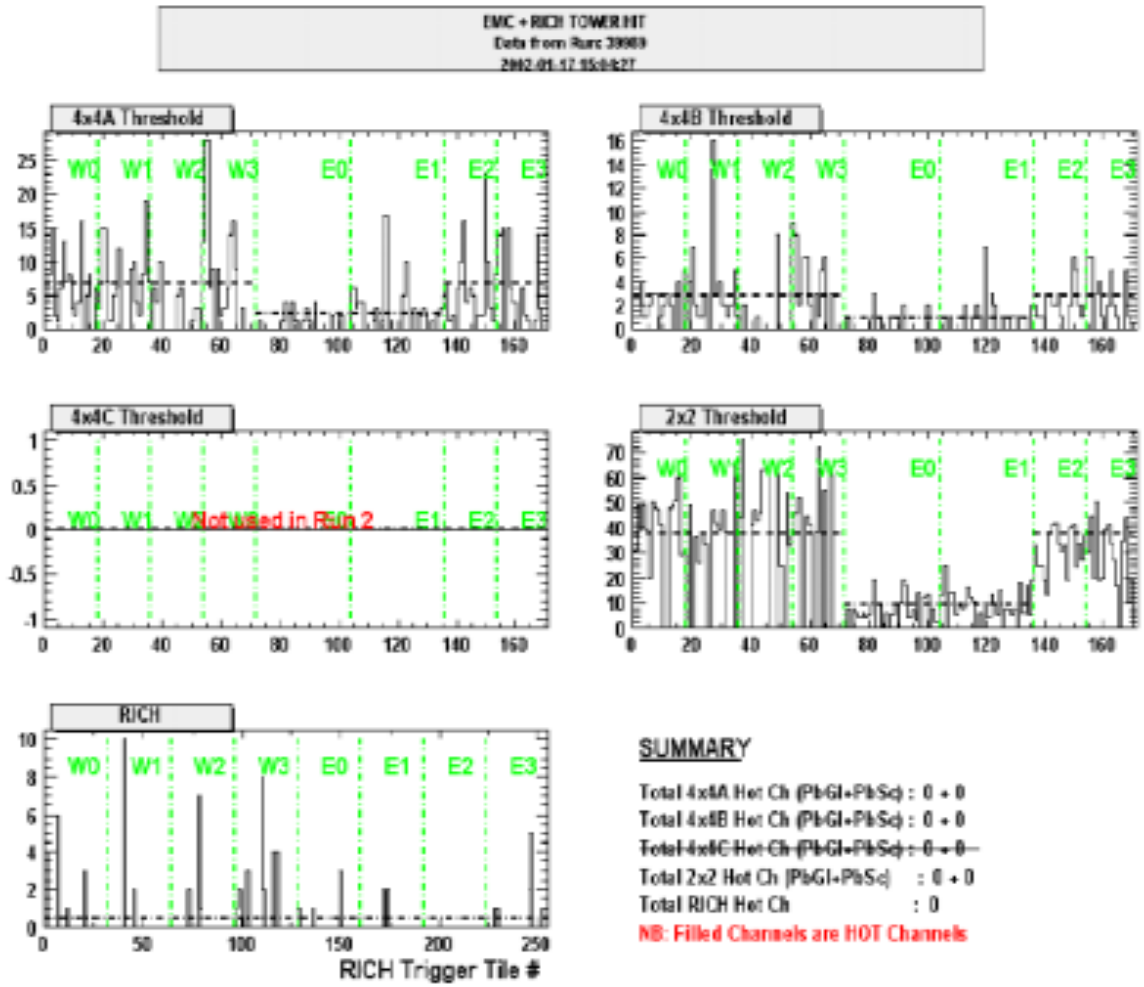
West 100 SMs



During pp RunII : Mask Scan

- In addition to the masked SMs at the threshold scan

- Using the online monitoring software, some additional masks were obtained in the beam condition. (Run 38730 & Run 38789)
  - 2x2: 13SMs
  - 4x4A: 3SMs
  - 4x4B: 2SMs
- The algorithm is to find hot and cold channels compared to the mean hit frequency.



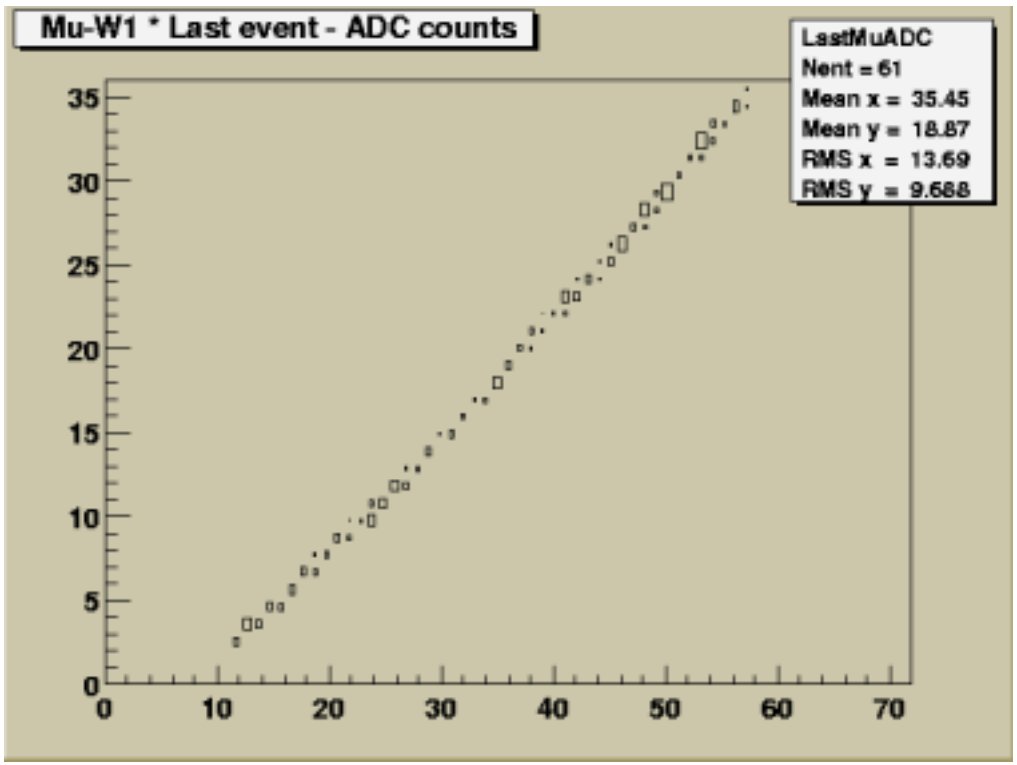
During pp RunII : Summary

- Mask
  - 1-version of mask after Run38823 (Jan/5)
    - 2x2 : 27 SMs
    - 4x4A : 40 SMs
    - 4x4B : 50 SMs (total 172SMs)
  - During run
    - The shifter did the online monitoring software to find the noisy SMs, and increased the number of mask.
    - The history of the mask have been recorded into Objectivity data base and was used in the offline analysis.
- Threshold
  - Run38844 - (Jan/6)
    - Threshold 21(0.15GeV)→24(0.3GeV) for 2x2 trigger
  - Run39785 – (Jan/15)
    - Threshold 24(0.3GeV)→34(0.8GeV) for 2x2 trigger

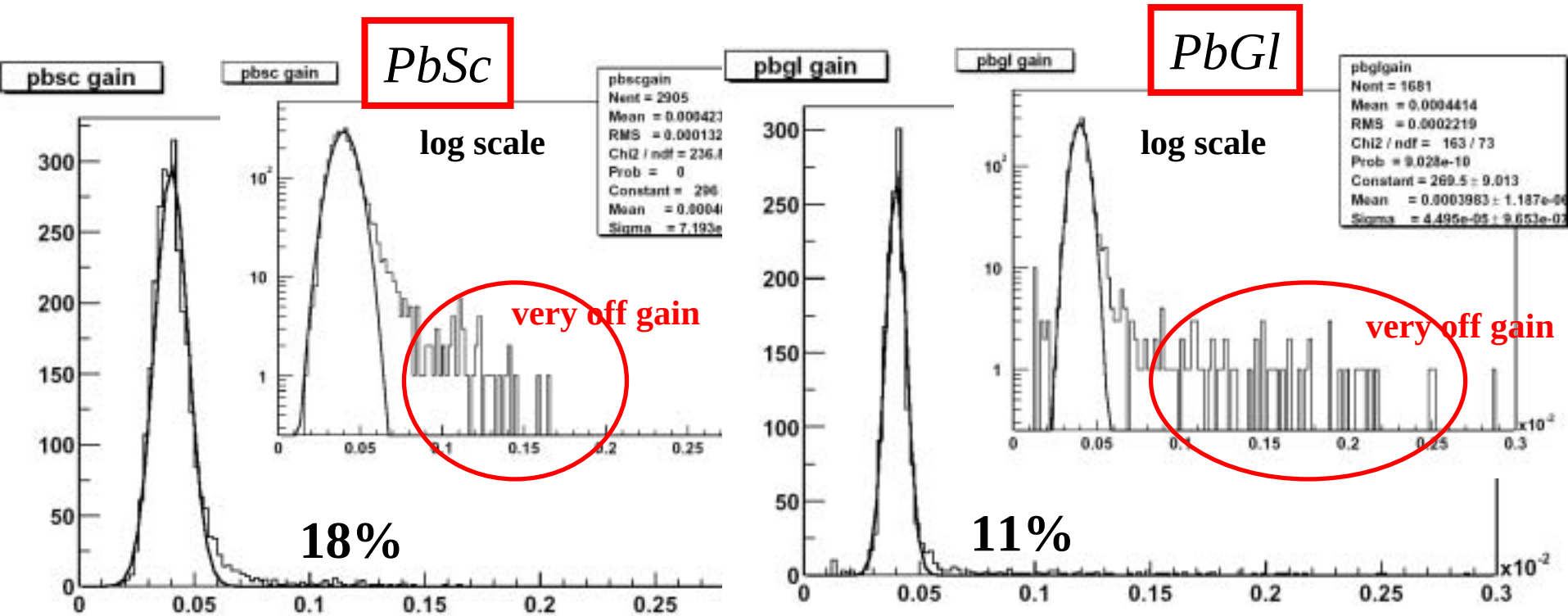
Cosmic Ray Run (2002/Jan)

- Just after pp-run
- The mean deposited energy in a tile is ~70MeV
  - Need to decrease the threshold
- Increased the multiplicity threshold into 5
- After repeating the threshold and mask scan, the threshold for 2x2 was set to
  - 19 (~0.05MeV)

→ The multiplicity threshold worked to reduce the noisy channels



Offline Analysis : Gain Variation

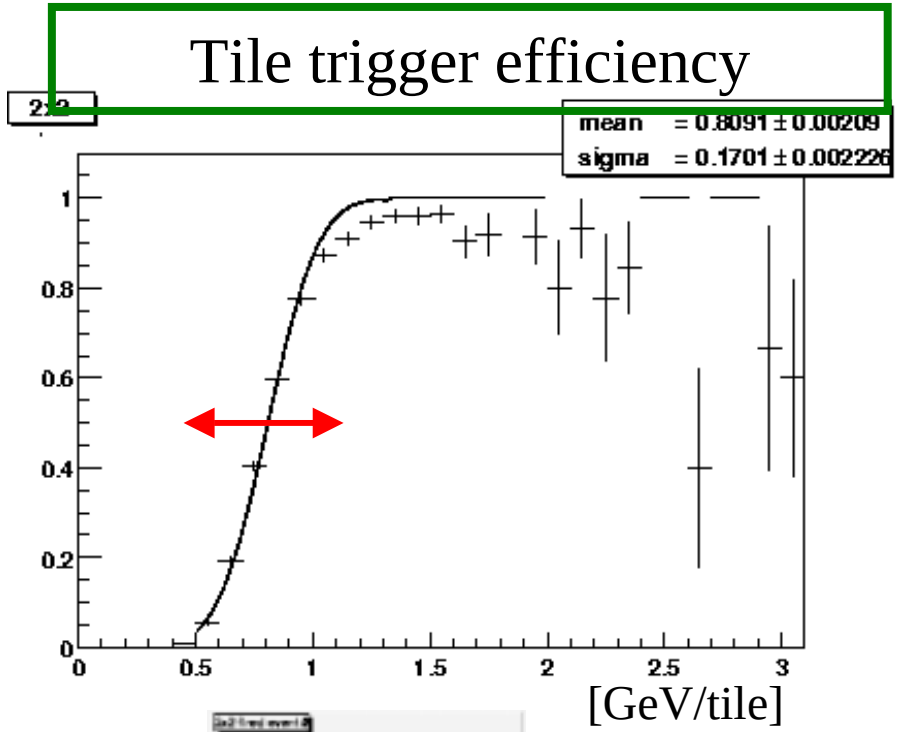


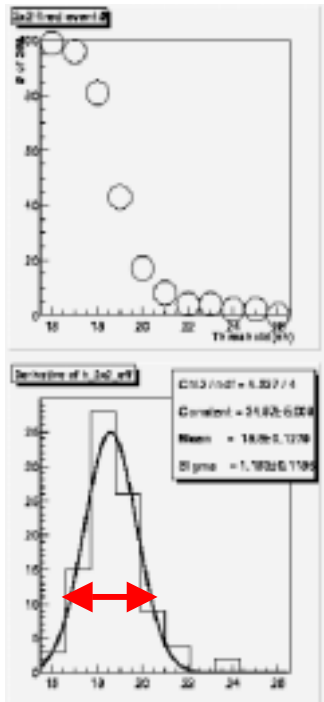
PbGl has better shape than PbSc.
Both of them have some very off gain PMTs.

Offline Analysis : Turn-on Width

- The width of turn-on curve was obtained from one threshold setting. (34 for 2x2)
- The threshold scan gave the idea about how much variation the DAC have.

→ For 4x4A/B, the DAC variation is dominant terms





Offline Analysis : Turn-on Width

- 2x2 (~0.8GeV threshold)
  - PbSc: 0.15GeV width = 0.15^2 + 0.10^2
  - PbGl: 0.10GeV width = 0.08^2 + 0.10^2
- 4x4A (~2.1GeV threshold)
  - PbSc 0.6GeV width = 0.38^2 + 0.56^2
  - PbGl 0.6GeV width = 0.22^2 + 0.62^2
- 4x4B (~2.6GeV threshold)
  - PbSc 0.6GeV width = 0.47^2 + 0.59^2
  - PbGl 0.6GeV width = 0.29^2 + 0.63^2

PMT/VGA gain variation

DAC variation?

* The value is based on 18%(PbSc) and 11%(PbGl) gaussian width

Future Plan : Turn-on Width

- PMT/VGA gain variation
  - 18% for PbSc, 11% for PbGl
  - Well known for all towers
    - Some towers with higher gain affected the turn-on curve.
  - Can be reduced by adjusting VGA gain for PbSc and HV setting for PbGl
- DAC variation?
  - Need one more proof
  - Kensuke will look at tower-by-tower threshold turn-on curve before APS meeting.

Future Plan : Noise

- Some ideas
  - Replace the FEM boards
    - Of course, it's best way.
    - But, it's hard to find the noisy channels.
  - The switch on/off in the test bench
  - Set DAC setting into maximum so that the noise won't fire the threshold
  - Increase the multiplicity threshold
    - If the noisy channels are always-fired, then this idea will be fine.
    - If not, ….

Summary

- From RunII
  - Always-fired channels existed probably in ASIC boards
  - Some channels may have wrong 4x4 algorithm.
  - To reduce noisy channels
    - “Switch on/off” didn’t work
    - “Multiplicity threshold” worked
  - Threshold behavior for 2x2/4x4A/B are known for each sectors, but not for each towers.
- Plan for RunIII
  - Noisy channels (20% of SMs)
    - Some ideas. They will be painful.
  - Threshold
    - VGA gain
    - DAC setting

Backup slides

Documentation

- ERT lvl-1 trigger Home Page

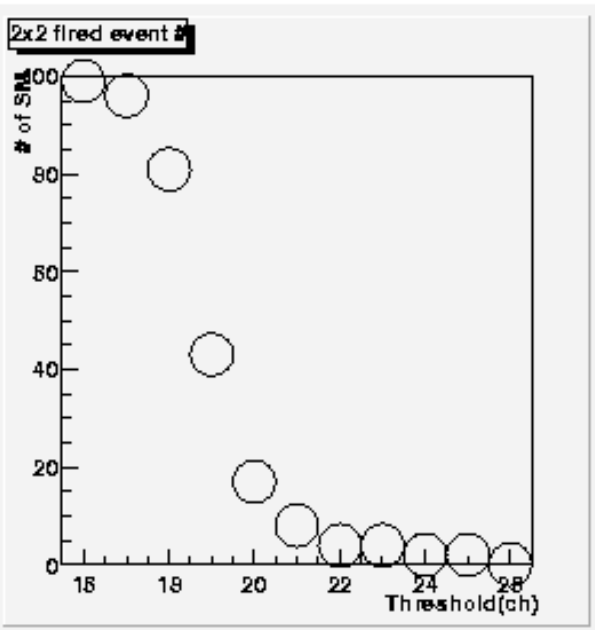
https://www.phenix.bnl.gov:8080/phenix/WWW/trigger/pp/c-arm/index.html

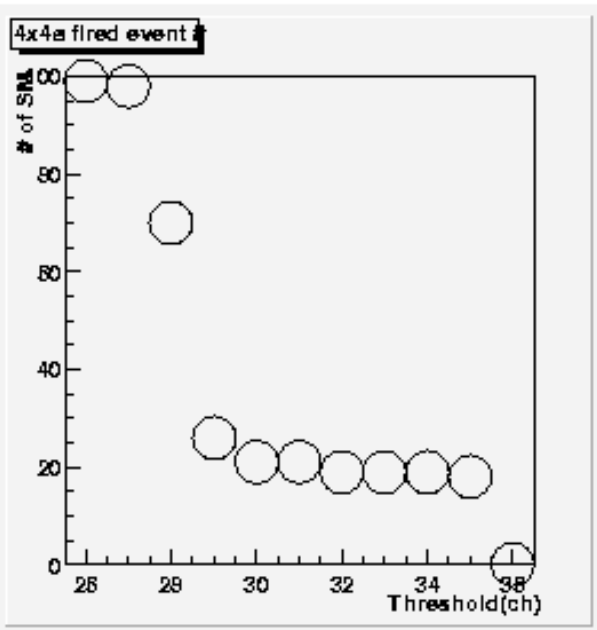
→ Nice RunII summary page by Kensuke

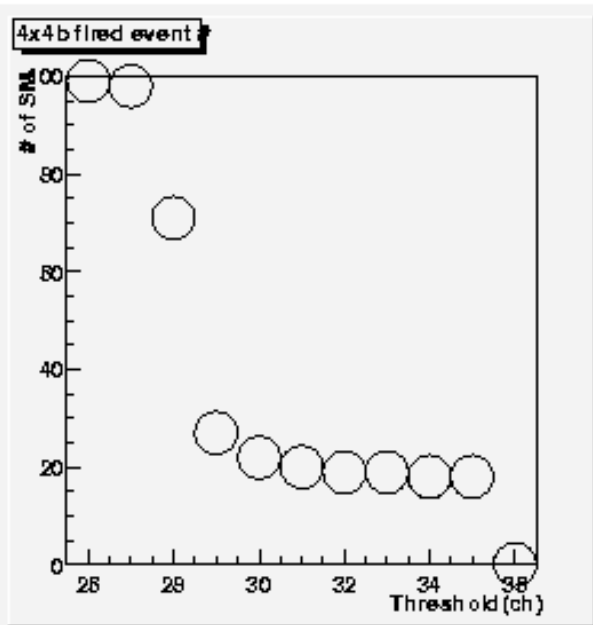
- ERT trigger Run2 note (still draft…)

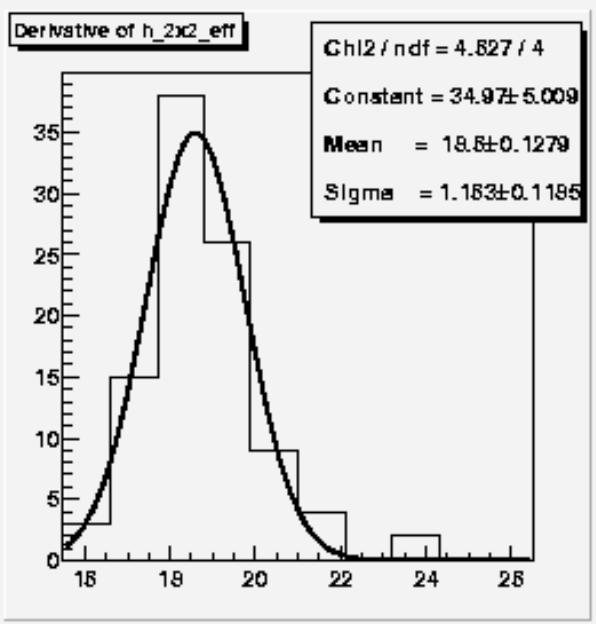
https://www.phenix.bnl.gov:8080/WWW/p/draft/htorii/ert/ert_note.pdf

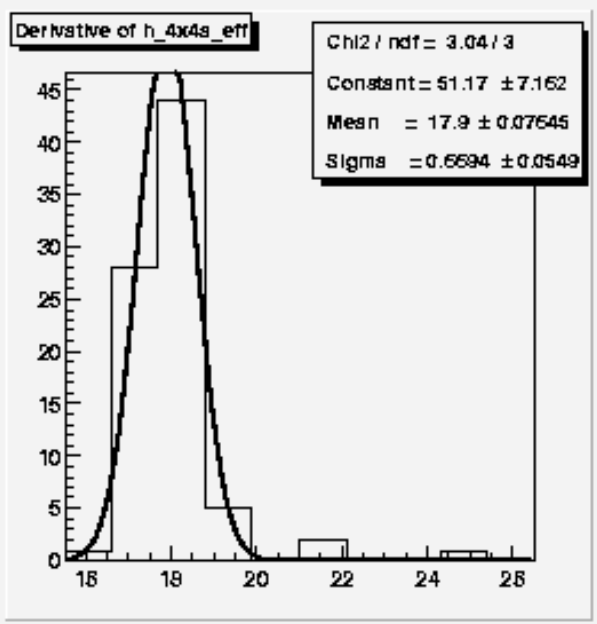
Threshold Scan

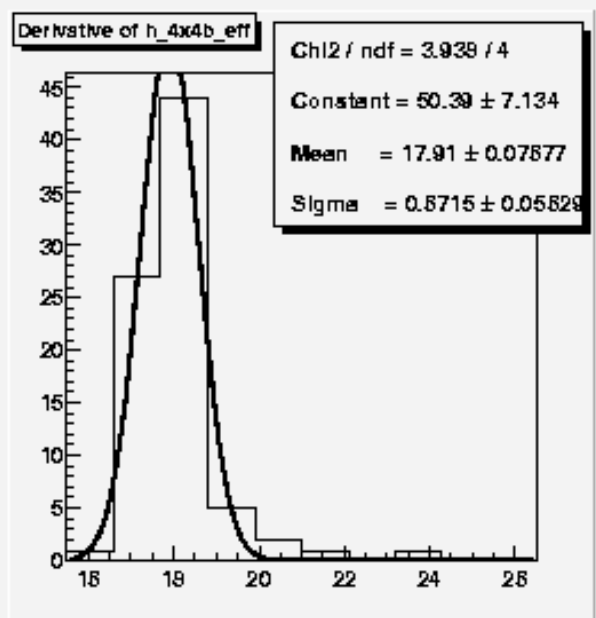












BAD ASIC behavior

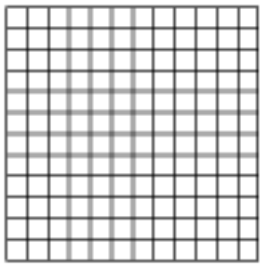
- Noisy
  - More than 3 times of RMS, typically ~100 RMS
  - It can be caused by AMU/ADC cells
- Overflow or low level
  - The average is 4096(overflow) or <~3000
  - Any tune up doesn't work.
- One channel dead

We salvaged 7 crates (42/70 ASIC)

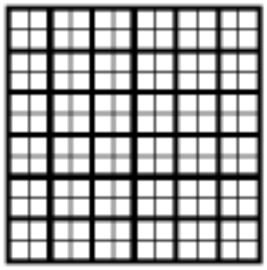
Correspond to~1000towers

• Noisy	
– HG	2
– LG	3
– TAC	2
• Overflow or low level	
– HG	6
– LG	2
– TAC	4
• One channel dead	4
• Etc	4
Total BAD ASIC	27

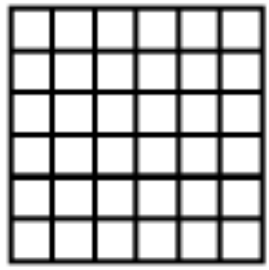
Algorithm explanation by Paul



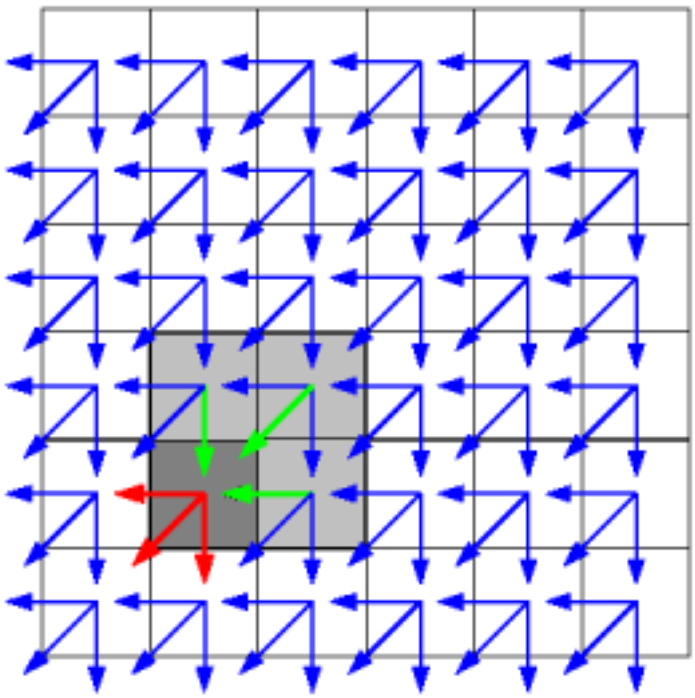
12x12 tower "Supermodule" to one FEM



Each ASIC chip services a 2x2 block



6x6 array of chips, each with a 2x2 sum



Each chip sends out 3 copies of its 2x2 sum to three neighboring chips (which may be on different ASIC cards or on different FEM's).

Each chip also receives 3 copies of sums from neighboring chips.

With its own 2x2 sum and the three incoming 2x2 sums, each chip constructs a 4x4 tile sum. Effectively, each 4x4 tile is "owned" by the chip in its lower left corner.

There are 36 2x2 disjoint sums per FEM, one for each chip. Each 2x2 sum is amplified and compared to a threshold, which fires the Muon bit, one per chip.

There are 36 4x4 overlapping tile sums per FEM, one for each chip. Each 4x4 tile sum is compared to three separately-programmable thresholds, which produce the Photon1, Photon2, and Electron bits, one each in each chip.

A total of 144 bits – 36 Muon and 36 of each Photon1, Photon2 and Electron – are presented to the Trigger Card on each clock tick.

Additionally, each chip passes its analog 2x2 sum to the Trigger Card to allow the construction of an analog 144-channel sum signal.

Kensuke's result

Fitting results

Trigger and detector	Mean (ADC value)	Width (ADC value)		Threshold* [GeV]	Width* [GeV]
2x2 PbGl	1872	261 (14%)		0.75	0.10
2x2 PbSc	1980	256 (13%)		0.79	0.10
4x4a PbGl	4911	1400 (29%)		2.0	0.56
4x4a PbSc	5378	1551 (29%)		2.2	0.62
4x4b PbGl	6201	1464 (24%)		2.5	0.59
4x4b PbSc	6769	1573 (23%)		2.7	0.63

) E[GeV]=0.0004(ADC value)