Summary of RICH Trigger in Year 2 p+p RUN

Fukutaro Kajihara
For the RICH trigger team

History of RICH Trigger commissioning

- End of December

  The RICH Trigger bits started to be seen through ERT

  The trigger has been *at least* working
- Early January (~7)
  - Both trigger bits through ERT and charge information of RICH are readout for each event
    - Estimated efficiency to be rather low
- Middle of January(8~20)

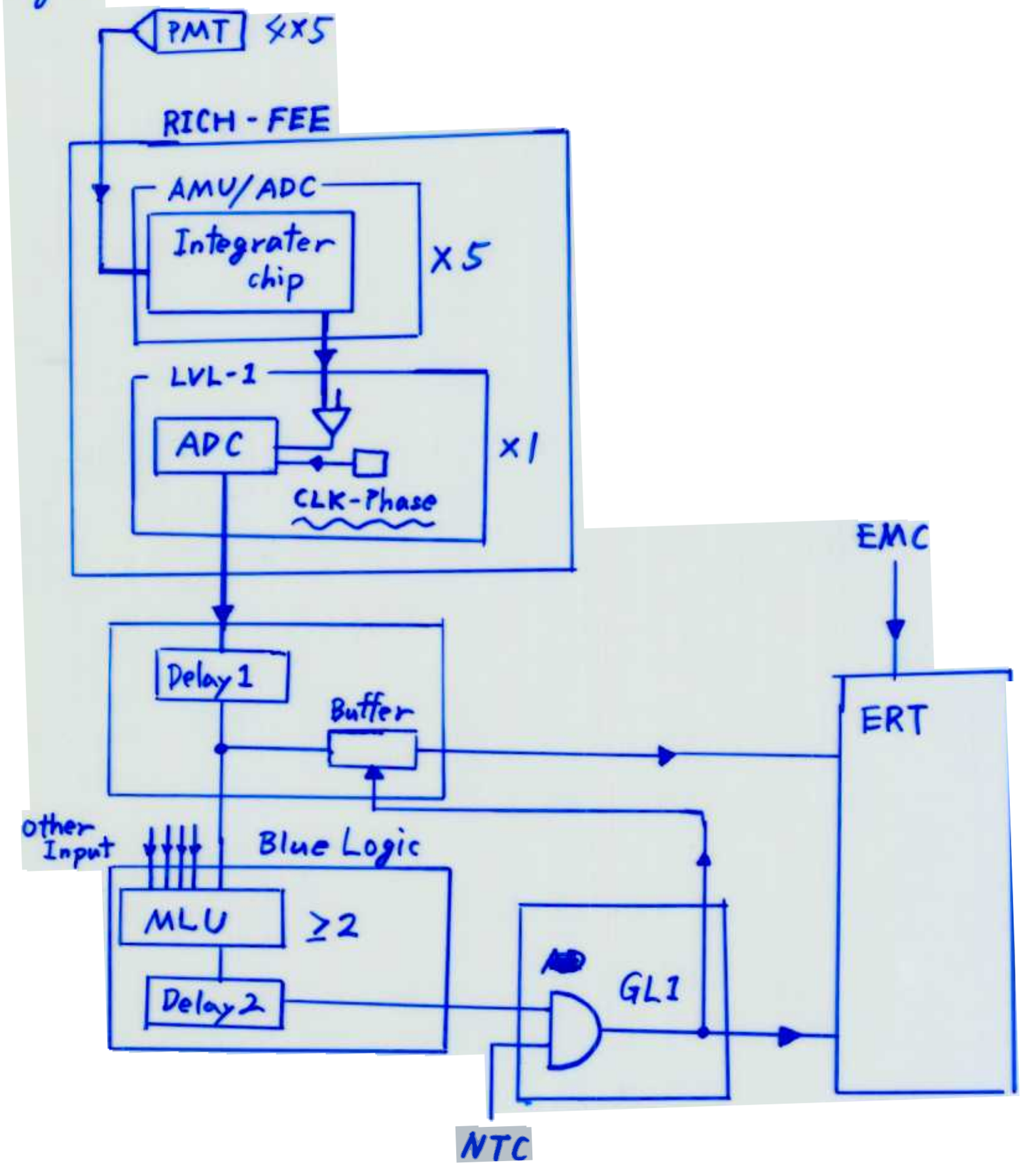
  Worked on both re-timing and hot channel masks

  Also worked on minimizing the dead channels

  Found FPGA code problem (2 of 4 ADC phase were not working)
    - Fixed on 18th.
- End of January(21~)
  - Obtained performance and efficiency using raw PRDF data.

  Found “dead channels” to be dead

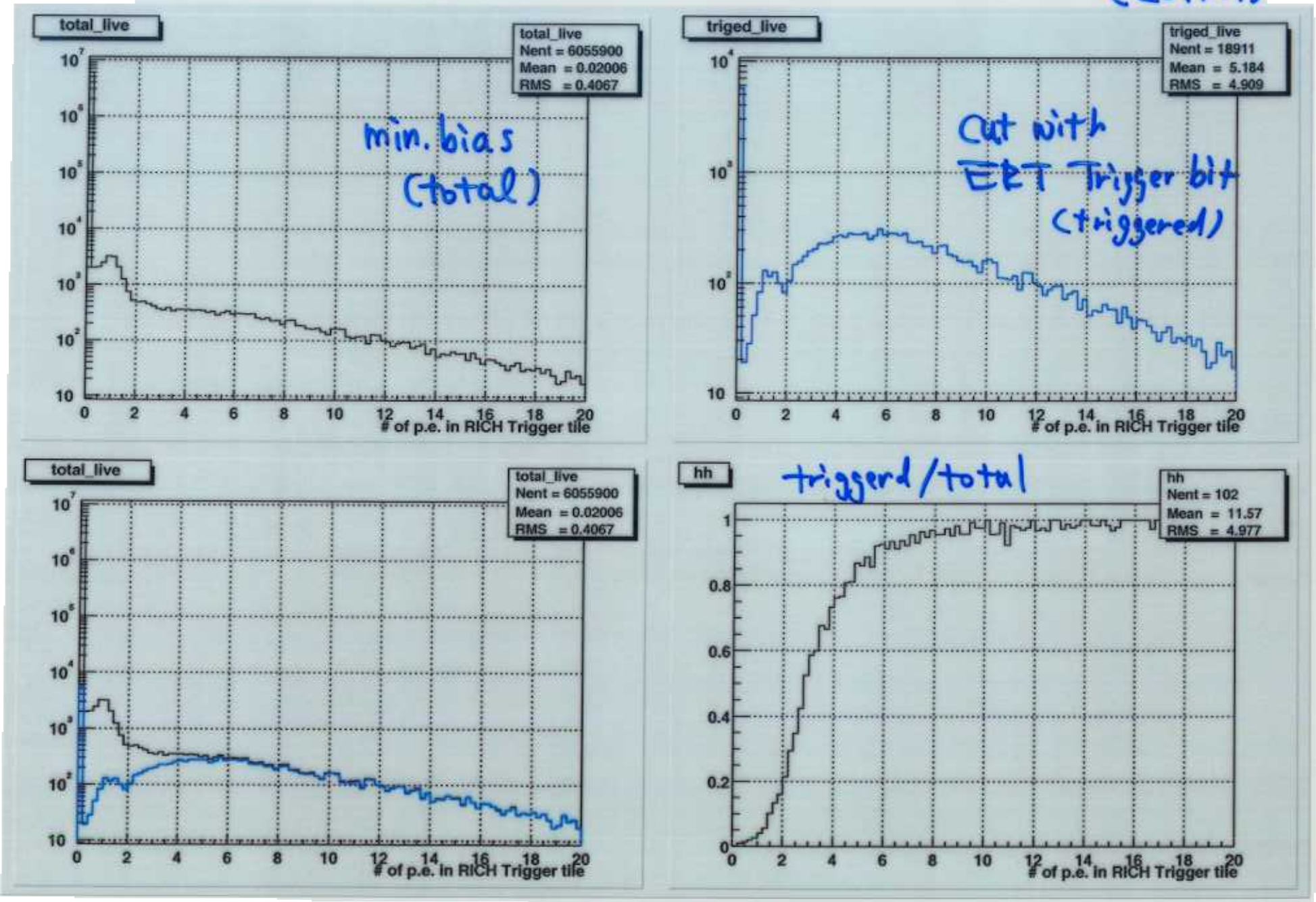
Fig 1.


PMT
4x5
RICH - FEE
AMU/ADC
Integrater chip
x5
LVL-1
ADC
x1
CLK-Phase
EMC
Delay 1
Buffer
ERT
other Input
Blue Logic
MLU
≥2
Delay 2
GL1
NTC

Current Status and performance

- Additional scans after last access
  - 4 ADC phase × 3 delay settings + 3 another settings = 15 scans
- Statistics obtained:
  - Working : 38 tiles (14.8%)
  - Masked (hot channels) : 74 tiles (28.9%)
  - Dead (No signals) : 144 tiles (56.3%)
- Oscillation problem
  - 2037 PMTs (39.7%) had oscillation problem
- Look at the plots seen!

run 40383 P.E. distribution in a RICH Trigger tile (20PMT)



Towards next Year RUN

- No signal channels
  - Problem mainly stays on Int-R Chips on AMU/ADC boards
  - Trigger sum signals have not been checked before the first installation of RICH FEE
  - Reship crates to Japan and check them
- Oscillation problem
  - Charge information from RICH packets has no problem
  - low frequency baseline noise that affects to trigger sum signal
  - Will be checked in Japan with two crates
- Trigger Logic used for Year-2 MUST be preserved
  - Will help checking if new LL-1 board works
  - Good Reference
- Less parameters! More Spy out!