Simple DAQ Systems for FPIX2 FPGA Development at LANL

PLM 12/11/06

We've assembled two DAQ systems to read out data from the FPIX2 through a Xilinx Virtex-4 FPGA development board. The goal was to use off the shelf components that require a minimum of programming to record the data. Optionally, the raw data is converted to a ROOT ntuple containing the hit row, column and amplitude value. We also have an Actel FPGA board that can be interfaced to these DAQ systems.

System 1. Provides ~1MB/sec sustained rate to disk/ntuple file. Three high-speed 8-bit parallel ports are used to read a 24-bit word from the FPGA, as shown in Figure 1. A control line from one port of the PC is used to clock the data from the output FIFO of the FPGA. The parallel ports can operate in PS/2 mode or EPP mode (which is about twice as fast). The software is very simple linux C code using direct I/O through the parallel ports. This system is adequate for measuring the FPIX noise, channel by channel, in about ten minutes. The software can also be compiled to run under windows. These PCI card based parallel ports are very inexpensive and easy to use. Data and clock lines are TTL, carried on regular ribbon cable. The FPGA output lines are set to 2.5 V CMOS. Interface connections between the FPGA, FPIX (single chip) and PC were bread-boarded using twisted pair and flat ribbon cabling.

System 2. Provides ~80MB/sec for a 64MB 32 bit transfer to memory. The sustained rate to disk has not yet been measured. This system uses the National Instrument PCI-6534 digital I/O card, as shown in Figure 2. Up to 32 bits of data can be collected at 20 MHz using pattern I/O. The PCI card generates pulses that are used as before to clock the data out of the FIFO. Cabling is done with commercial shielded twisted pair cable. The clock line is 5V TTL, resistively terminated and attenuated to 2.5V at the FPGA. The FPGA outputs are 2.5 V CMOS. The software is very simple, written in C for Windows using National Instrument's DAQmx driver.

We've used the PCI-6534 hardware to successfully read data at full speed from a 74F series TTL counter clocked at 20 MHz. We are presently connecting it to the FPGA board. This system appears capable of transferring data at the speed of existing PHENIX data collection modules. The PCI-6534 is somewhat expensive, costing about $2000 for the card and shielded cable. Interfacing between the FPIX (on an 8 chip HDI test card) and the FPGA was done with a 4 layer PCB adapter card and twisted pair cabling (Figure 3). The FPGA to PCI card interface was done with a 2 layer PCB and shielded cable (Figure 4).

I can supply the PC-based software to anyone interested.

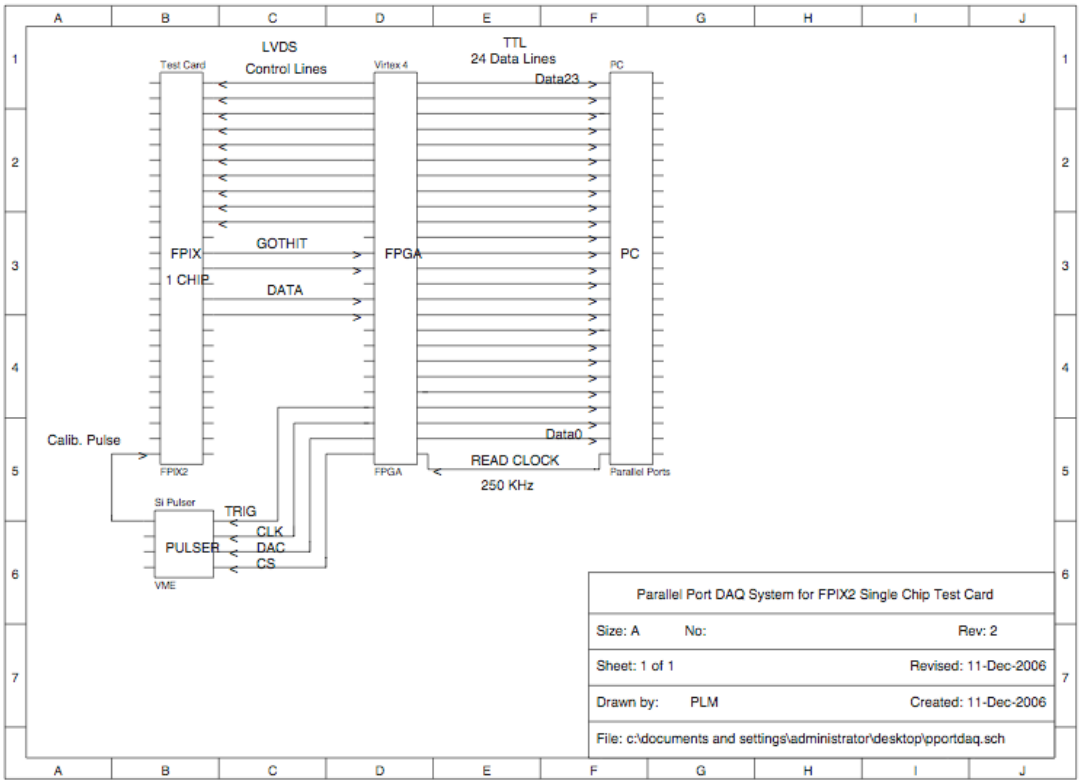

Figure 1. DAQ system for FPIX2 single chip test card using fast PC parallel ports.

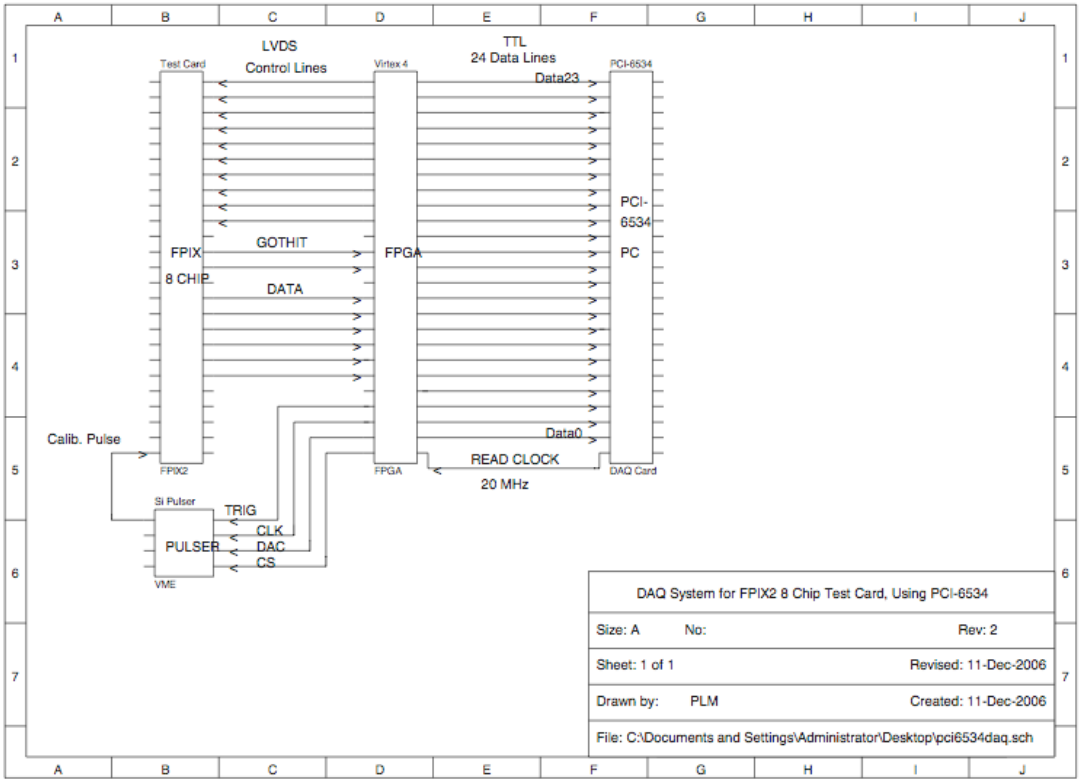

Figure 2. DAQ system for FPIX2 eight chip test card using NI PCI-6534 card.

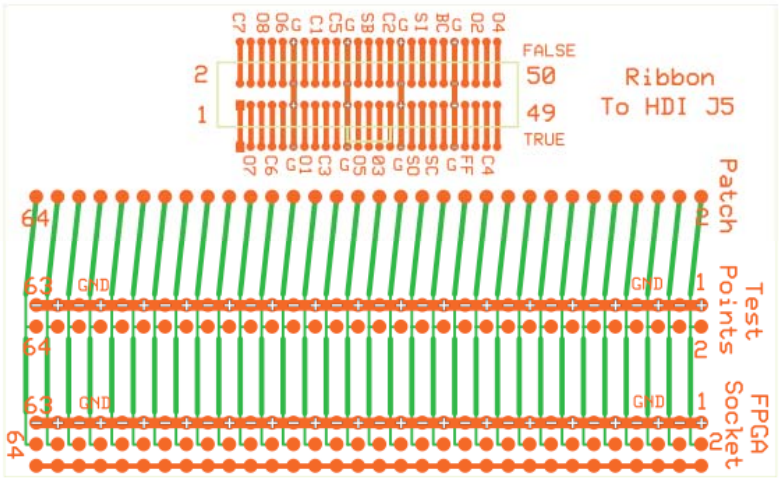

Figure 3. Interface card between FPIX 8 channel test card and Virtex 4 FPGA board. Top connector is attached through 50 pin .025 ribbon to FPIX. Bottom connector attaches to FPGA board.

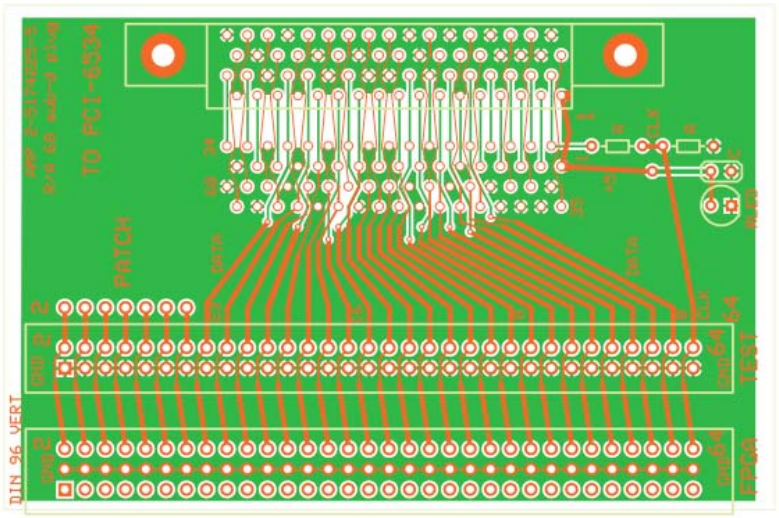

Figure 2. Interface card between Virtex 4 FPGA board and cable to PCI-6534. Top connector is for shielded cable to PCI-6534 card. Bottom connector attaches FPGA board.