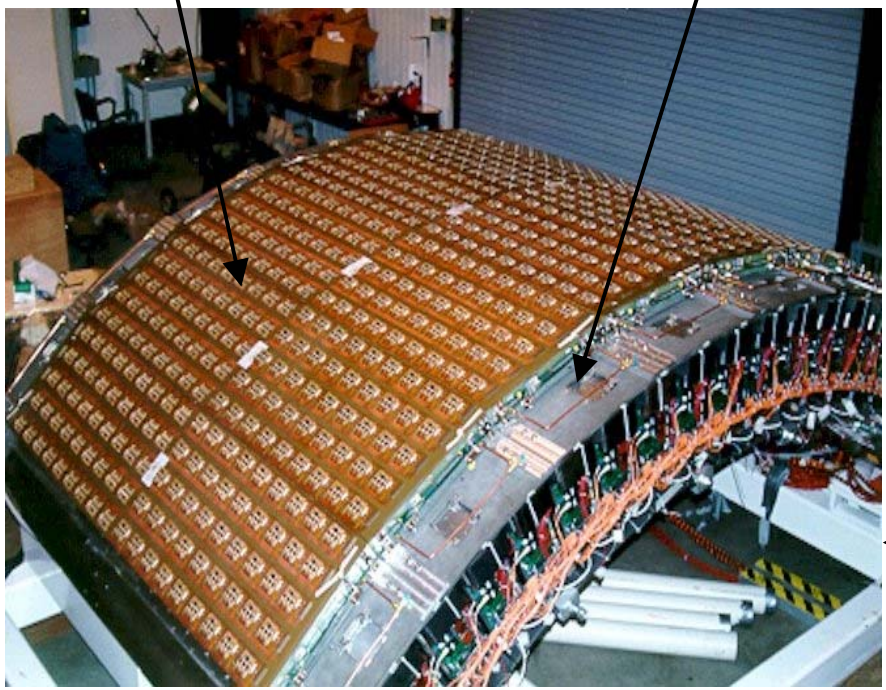
Pad Chambers

Readout Card (ROC) (Lund)

Front End Module (FEM) position (ORNL)



Eight fully instrumented PC1 mounted on top of the Drift Chamber.

Qualities

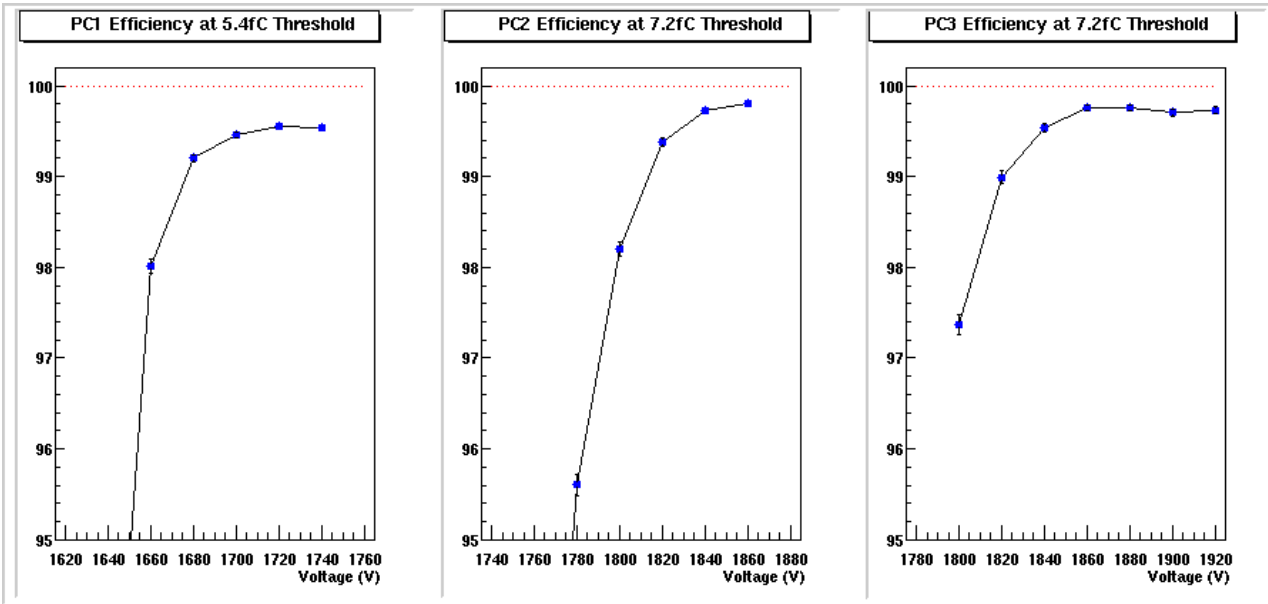
* Efficiency close to 100% and good spatial resolution. Noise free operation. Intricate pixel pattern also reduced needed number of channels, as well as insuring multiple channels firing for a single hit.

* Low mass to minimize the secondary particle production and multiple scattering

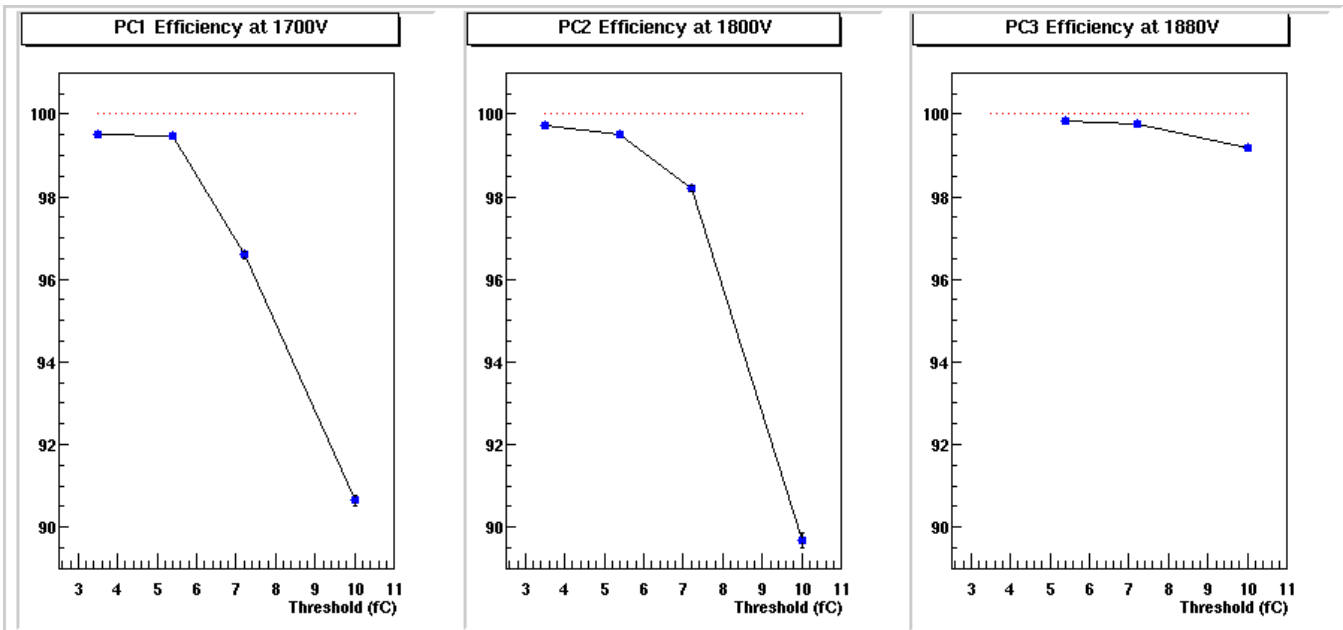
ROCs can give a LVL1 trigger signal with resolution of 4cmx4cm for PC1, (or 8 cm by 8 cm, if we blow up the size by a factor of 2, a.k.a. PC3 size).

Efficiency Studies

Efficiency as a function of HV



Efficiency as a function of threshold



Intrinsic efficiency is better than 99.5 %.
Results obtained with 4-fold coincidence.
No noise contributions down to 2 fC.

Position resolution: ~mm

PC by Numbers (details)

Parameter	PC1	PC2	PC3
Gas gap [mm]	6	10	12
Number of wires	58	116	116
Wire pitch [mm]	8.4	13.6	16
Anode wire thickness [um]	25	25	25
Number of cell rows	212	106	106
Cell pitch [mm]	8.45	14.25	16.7
Dimensions LxWxH [cm]	198x50x6.0	151x157x7.2	177x185x9.0
High Voltage [V]	1 700	1 840	1 880
Threshold [fC]	5	7	7
Gain factor [k]	14	15	13
Efficiency [%]	99.6	99.8	99.8
Position resolution [mm] (along wire)	1.7	3.1	3.3
Area [m2]	0.99	2.37	3.27

Feasibility for Muon arms

Location	Max Nhits	Area [m2]	Min # Channels / channels to get good resolution	Required resolution	Comment
MUTR Station 1	200	6 to 7	2000 / ~20k	~a few mm	PC1 segmentation ok, possibly complicated geometry
MUID Gap0	100	100	1000 / ~13k	~a few cm	Even PC3 segmentation is somewhat of an overkill

There are ~900 ready readout cards for about 43 k channels, or about 10 PC1s, or 20 FEMs.
There are additional chips for about 50k channels more.

Another batch of FEMs (handles 2160 channels = 45 ROCs or 5 rows of 9 ROCs each) would be needed as well as more connector cards (and/or different design for the Motherboard, chamber connections).

To get the trigger signals from the ROC, some additional soldering is needed.

Implementation ideas I

Simplest scenario: coverage before and/or after MUID. Instead of making complicated MWPCs, perhaps the simplest/most cost-effective is to use Iarocci tubes(?).
One readout-unit/"super-tube" could correspond to one row of 9 ROCs. Five rows make up one FEM. It would thus be advantageous to have the super-tube 9 times as long as it is wide.
Each ROC (48 channels; 9 pixels per channel) covers a square 12x12 area of readout cells (3 pixels per cell). The resolution would be approx. super-tube-width/12 (= readout cell size) divided by sqrt(12). Thus to get at a resolution of say X cm, a super-tube width of X*41.5cm would be needed.
A width of 6 normal MUID tubes (9mm cells, 8 cells/wires per tube) for a super-tube, is thus perhaps not a bad match(?), between a reasonable resolution and a not too big/reasonably robust object: 0.45 m*4m. Or perhaps a length of 5 m with slightly rectangular (not exactly quadratic) pad pattern. I assume that 1m * 9m is out of the question, otherwise that'd been my choice.. [1 super-tube = 12 MUID tubes]
This needs to be verified with Pol.Hi.Tech (M. Meoni).
With the 2.5m*4m per FEM we'd need 10 FEMs for one layer that covers full MUID acceptance. If we could go with the 1m*9m option, 2 FEMs could be enough per layer and orientation.. (some trick needed for square hole; skip 4 ROCs.., and chop up the Iarocci tube somehow?)

Implementation ideas II

Caveat; pixel-scheme might not work so well for streamer tubes – would need to be tested.
The trigger signals from the DMU assume the pixel-pattern; may work for pad pattern without interleaved pixels but am not completely sure about that. (Anders is thinking about it)

Alternative arrangement would be 3*16 channels or 4*12 channels (for one ROC) in a staggered pattern; however there is an intrinsic conflict between covering large areas and having multiple channels firing for a single particle!
As usual, the devil is in the details..

Large MWPCs similar to half a PC1 in design, but with a pixel size larger than PC3 should in principle work well: better efficiency and performance than with the Iarocci tubes. However, getting largish pixel- and mother-boards + building the chambers would require quite some work..