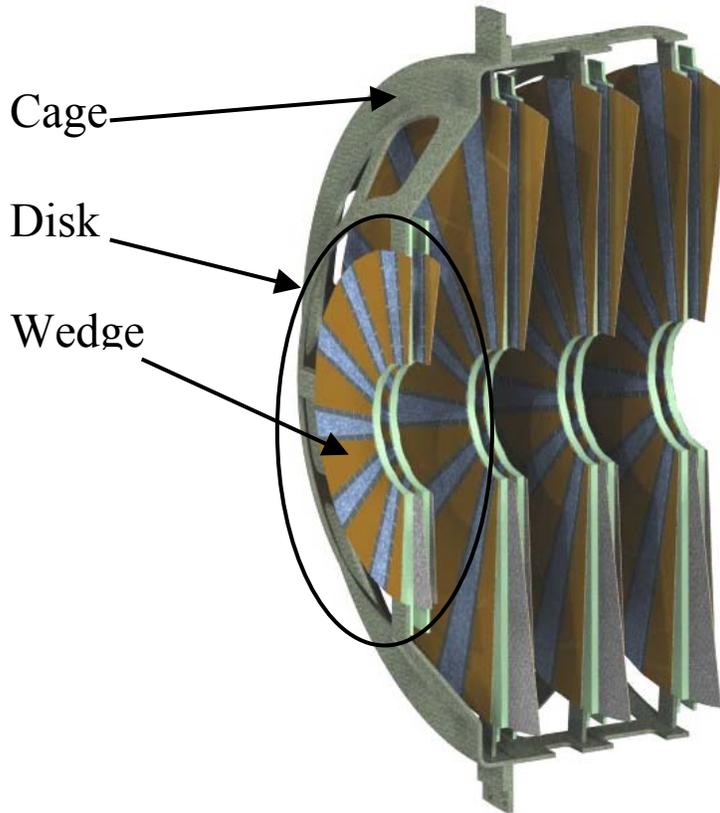


Project Name: PHENIX-FVTX  
Federal Project Director:  
Contract Project Manager: Melynda Brooks, LANL

Date: January, 2009

Reminder of some nomenclature:



Narrative of project highlights:

**WBS 1.4.1, Sensor Prototyping:** The sensors required for the FVTX project were specified, reviewed internally, and a request for quote for producing sensor prototypes as well as the production sensors was processed through the LANL purchasing department. The contract was awarded to Hamamatsu, and prototype sensors were delivered in October, 2008. Seventeen prototype FVTX sensors were delivered out of 20 requested – the shortfall was due to a manufacturing error. Hamamatsu performed quality acceptance testing on each sensor to ensure that they met our specifications criteria. All specifications were met or exceeded with the following single exception. The maximum resistance value of the polysilicon resistors on the sensors exceeded our maximum specification by about 5%. We accepted this exception because it has no negative impact on sensor performance. Work is underway at the University of New Mexico to duplicate the Hamamatsu tests. If all testing of the sensors, and sensors with readout chips pass our qualifications, then the procurement of the set of production sensors is expected take place in Q2 FY09.

**WBS 1.4.2, Silicon sensor readout chip (FPHX) prototyping:** FNAL completed the design and layout of the FPHX in May 2008 and the chip was submitted to MOSIS June 2, 2008. The prototype chips were received at FNAL on August 21, 2008 where initial power-up and verification of analog output was performed after having a single chip wire-bonded to a test board. The chip was then carried to LANL for more detailed testing of the chip with a test stand which was developed at LANL. All download functionality was exercised, data read-back was performed, and the analog output was studied versus the various chip download parameters. The chip was found to have approximately 200 electrons of noise with no sensor attached, had thresholds which were uniform to within the same noise levels, and the analog output varied with chip download parameters as expected. The noise levels measured (under somewhat less than optimum conditions because several long wire-bonds were included in the setup), can be compared to  $115 e + 134 e/pf$  expected noise levels, based on simulations from the FNAL chip designers. According to the analog engineer, the 200 electrons of measured noise is consistent with the expected baseline noise plus the extra capacitance that is introduced on the front end due to our setup.

Full analog tests which fully exercised all chip download parameters were performed by the analog engineer, Tom Zimmerman of FNAL, and he found the chip to fully perform as expected. Tom has however suggested that he can change the physical layout of the chip in such a way as to reduce threshold dispersion among the channels of the chip. We expect to take advantage of this possibility for redesign since he says it is a straight-forward change for the chip.

The digital portion of the chip was further exercised at LANL to check for beam-clock and hit output stability. The chip was pulsed several hundred thousand times with fixed amplitude, fixed spacing between pulses, and fixed numbers of channels unmasked. The data was then checked to see that the ADC output, beam clock number (which should be fixed for these data sets) and channel ID were stable across the entire data set. The relative timing of the pulsing with respect to the beam clock edge was also varied. It was found in these tests that there is an error in the digital chip logic that causes a fraction of beam clock numbers to march out of time when a large number of channels fire at once and when the pulse is near the beam clock edge. The digital designer, Jim Hoff, has since diagnosed the logic problem with the chip and has informed us that a straight-forward fix is in hand. To date this is the only flaw we have found with the current chip design.

A set of all chip modifications required between this round and next round has been transferred to FNAL. Most of these changes just require removing a number of test features that were on this first round prototype chip that we do not want on the production chip. FNAL has agreed to review this list and suggest a schedule for redesign, and ultimately resubmission of the chip. We will not, however, resubmit the chip until all system tests with readout chip, sensor and HDI have been performed (see next).

**WBS 1.4.3, HDI:** The kapton HDI layout was completed by UNM and submitted to Dyconex for manufacture. The first prototype HDIs are expected to be delivered in February 2009.

Following our November 2008 FVTX Annual Review, we agreed to in parallel develop a PCB-version HDI so that earlier sensor-readout chip system tests could potentially be performed and so that we would be less likely to incur additional schedule delays if the more complex kapton HDI 1<sup>st</sup> round prototype was not fully functional. The design of this PCB HDI is mostly complete as of January 9, 2009 and we expect to go out for manufacture shortly. The design and layout work were completed by our LANL engineer and designers (of AOT division).

Based on this schedule, we expect to have wedge tests with PCB and kapton HDIs commencing by February, 2009.

**WBS 1.5, DAQ development:** The first round ROC prototype board has been assembled and is was delivered to LANL by the week of January 11, 2009. The board will first undergo basic power-up tests by the engineer and will then be passed to LANL physicists for more complete tests. We have FPGA software in hand which will allow us to connect prototype FPHX chips to the ROC board, and download and read back data from the chips. This will be used to verify basic functionality of the ROC board. Loop-back tests will likely be used to perform more complete tests of the full board.

This first round prototype ROC board has all the functionality needed for the FVTX detector, but is physically configured to read out our LDRD detector planes. The layout work for a version needed to read out FVTX planes is in progress at LANL. The first round FEM board layout is also in progress. A clock distribution board, which will be needed in the Interaction Region, between the counting house and the ROC boards, has been designed and laid out. One remaining board, a slow controls interface board which will sit in the FEM VME crates, remains to be designed.

**WBS 1.6, Mechanical Design:** Final design drawings of the backplane, disk, and cage designs have been completed, pending final review. A backplane prototype was procured from FNAL and a cage prototype will be procured from LBNL. Cost estimates from LBNL for production backplanes are somewhat less than our project estimates, and the estimate for the cage currently appears to be within the project estimates. Rapid prototype versions of the cage and disks are to be purchased this quarter to test out assembly procedures.

**WBS 1.4 and 1.7, Assembly Plans:** After a visit to the FNAL SiDet laboratory, it was decided to pursue having wedges assembled at SiDet rather than at an FVTX institution(s). SiDet is receiving \$15k of construction funds to work toward a wedge prototype and to produce a quote for full production. SiDet worked with HYTEC and Walter Sondheim to design assembly fixtures, and these have been manufactured and are being used at SiDet with mock-up wedge components. To date, the fixtures

appear to be fully functional, though some slight modifications may be suggested for for the final fixtures to improve ease of assembly.

Steve Pate, of NMSU has advanced the disk and full detector assembly plans and is taking a sabbatical at BNL from August 2008 – May 2009 to make preparations of detector assembly areas. Steve has worked with Ed O'Brien to identify lab space for assembly and has selected two rooms at BNL. Equipment for assembly and testing tasks will be identified so the rooms can be made fully functional while Steve is at BNL.

**WBS 1.8, Systems Integration** – Walter Sondheim, LANL, has continued to provide the mechanical integration for the project, working with HYTEC on the mechanical design and working with the VTX group to ensure that the VTX and FVTX detectors are compatible with each other inside the enclosure. Eric Mannel has provided the electrical integration for the project, coordinating our electrical reviews, and working with the groups to provide a detailed grounding & shielding plan.

Control milestones covered during review period:

- 1) **Milestone description:** HDI tested  
**Forecast vs actual start/completion date:** forecast Q3 FY08, actual Q2 FY09  
**Milestone result or impact of delay to project:** This milestone is now expected to be completed in Q2 FY09 as the first prototype is slated to arrive in February, 2009. The HDI is now considered to be on the critical path because we do not wish to procure the next round FPHX chips until system tests have been performed with readout chips and sensors on an HDI. To help alleviate the possibility of further slippage of the critical path, we have in parallel started development of a PCB-version HDI which should have no manufacturing challenges yet be fully sufficient to allow us to perform all system tests. The design of this HDI is basically complete and we expect to procure these PCB HDIs in January, 2009.
- 2) **Milestone description:** Sensor Prototype tested  
**Forecast vs actual start/completion date:** forecast Q1 FY01, actual Q1/Q2 FY09  
The first prototype sensor was delivered, and fully tested by Hamamatsu in Q1 FY09. Verification tests which will be performed at the University of New Mexico have not yet been fully completed because of technical issues setting up their probe station. We expect these issues to be fully solved shortly, and the delay in the verification tests does not cause any schedule slippage.
- 3) **Milestone Description:** First prototype wedge assembly complete.  
**Forecast vs actual start/completion date:** forecast Q1 FY01, actual Q2 FY09  
The wedge assembly has been delayed by the delay of the prototype HDI. The kapton and PCB HDIs are both expected to be available by February, 2009, so we expect this task to be completed in Q2 FY09.
- 4) **Milestone Description:** PHENIX system test complete.  
**Forecast vs actual start/completion date:** forecast Q1 FY01, actual Q2/Q3 FY09  
As with the previous milestones, this has slipped because of the late delivery of the HDI. We have attempted to mitigate any future additional delays by adding the PCB

version HDI, which is simpler to manufacture than the kapton HDI, and are considering the suggestion of our Annual Review Committee to make our second round FPHX prototype production also function as our engineering run. This could allow us to make up for schedule slippage that we have already suffered.

Brief summary of project issues, concerns, successes:

To date, the testing of the FPHX chip has shown the chip to be mostly operating as expected with only one small flaw in digital logic uncovered. We will continue these tests with prototype wedge assemblies once a PCB or kapton HDI is available. We are currently investigating with FNAL when the FPHX design engineers can be made available for redesign work for 2<sup>nd</sup> round submission.

After a number of schedule delays, the HDI is now expected to be delivered in February 2009 and a PCB version HDI available in January or February, depending on manufacturing schedules. With these HDIs we will perform system tests of FPHX readout chips and sensors. Once these tests are complete, we expect to be ready to complete any FPHX redesign work and submit the second round. We will have a review to determine whether this second round should also be used as a pre-production run.

The Continuing Resolution caused an unexpected (to LANL) reduction in funds transferred to LANL in FY09. To date, this has not resulted in any schedule delay because the missing funds almost exactly match the cost of our production sensor order, which is not expected to be placed until February or later.

Some additional expenses to the project have been incurred since the submission of the Management Plan. We describe those below, and how the costs will be covered.

Summary of total expenditures:

A WBS	B ITEM	C Baseline Total  Cost (AY\$)	D Costed & Committe d (AY\$)	E Estimate to Complete (AY\$)	F Estimated Total Cost (AY\$)	G Baseline Continge ncy (AY\$)	H Remaining Contingenc y (AY\$)
1.4.1	Wedge Sensors	1118	126	760	886	206	232
1.4.2	FPHX Chip	692	194	409	602	174	89
1.4.3	HDI	194	4	261	266	39	-71
1.4.4	Flex Cables	70	0	60	60	9	10
<b>1.4 Total</b>		<b>2074</b>	<b>324</b>	<b>1490</b>	<b>1814</b>	<b>428</b>	<b>260</b>
1.5.1	Fiber	21	0	19	19	3	2
1.5.5	Ancillary	246	0	116	116	23	130
1.5.2	ROC	615	21	522	544	139	72

1.5.3	FEM	578	0	435	435	130	143
<b>1.5 Total</b>		<b>1461</b>	<b>21</b>	<b>1092</b>	<b>1114</b>	<b>295</b>	<b>348</b>
1.6.2	Cage	174	89	77	167	35	7
1.6.3	Wedge	188	0	63	63	38	125
	Backplane						
1.6.4	Support Disk	114	5	81	86	23	28
1.6.5	Jigs	80	11	49	60	15	20
<b>1.6 Total</b>		<b>555</b>	<b>105</b>	<b>270</b>	<b>376</b>	<b>110</b>	<b>180</b>
1.7	Assembly	42	9	24	33	8	9
1.8	Integration	500	51	336	387	58	113
1.9	Management	249	49	169	218	28	31
<b>Total</b>		<b>790</b>	<b>110</b>	<b>528</b>	<b>638</b>	<b>94</b>	<b>152</b>
<b>Grand Total</b>		<b>4881</b>	<b>560</b>	<b>3381</b>	<b>3941</b>	<b>927</b>	<b>940</b>

The expenditures that have changed since the Management Plan, and how we will cover them are listed here:

- We have shifted part of the FPHX testing funds (\$30k) from FNAL to LANL since the FNAL engineers have been only minimally available for testing and Jon Kapustinsky has been instead coordinating these efforts. Since we currently expect only ~\$90k of the \$145k of funds allocated for FPHX prototype I work at FNAL to be invoiced, we believe this cost is still covered under the FPHX Management Plan costs as listed.
- A total of \$30k of sensor testing costs are also being transferred to LANL to cover efforts by Jon Kapustinsky to oversee the testing. This fits within the total sensor testing budget in the Management Plan.
- Following our FVTX Annual Review, we agreed to add a new task to our project: develop and procure a PCB-version HDI to allow sensor and readout chip testing at an earlier date. We estimate this task to cost \$40k.
- Clock and DAQ interface boards were not specifically called out in our initial estimate of the DAQ system. As the design evolved, we realized these boards should be separate boards from the ROC/FEM boards. Only a few boards are needed and the design/prototype work is estimated to cost \$40k. We do not have enough cost information yet to know if this fits within the ROC/FEM design and production costs as already listed in the Management Plan.
- \$37k has been added for ROC FPGA programming and testing of prototype boards.
- We share the costs with the VTX group for Eric Mannel's time for his job of Electrical Integration Manager for the FVTX and VTX projects. We have spent less for WBS 1.8 than was expected in the Management Plan because we budgeted for close to his full salary but paid a smaller fraction because of our cost sharing. For FY08 and FY09 we have spent \$61k less than budgeted for this task and will use this savings to cover some of the above added costs.
- We estimate we have \$940k remaining contingency, compared to \$927k baseline contingency, after all the added costs and savings have been included in the project.

Summary of expenditures by FY:

	FY 2008	FY 2009	FY 2010
a) Funds allocated	\$500k	\$2200k	
b) Costs accrued	\$144.4 k	\$188.7k	
c) Uncosted commitments	\$264.7 k	\$197.3k	
d) Uncommitted funds (d=a-b-c)	\$90.9	\$1814k	
e) Remaining total contingency			

Summary of schedule:

	Baseline Start Date mo/year	Baseline Completi on Date mo/year	Forecast Start Date mo/year	Forecast Completi on mo/year	% Co mplete Baseline	% Comple e Actual
Design						
1.4.1 Sensor*	4/08	7/08	6/08	10/08	100%	80%
1.4.2 FPHX**	10/07	4/08	10/07	5/08	100%	100%
1.5.2 ROC***	12/08	4/09	12/08	4/09	25%	25%
1.5.3 FEM	12/08	4/09	12/08	4.09		
1.4.3 HDI	4/08	8/08	6/08	11/08	100%	95%
1.6.2 Cage****, 1.6.3 wedge, 1.6.4 disk	4/08	10/08	4/08	10/08	100%	95%
Procurement					0%	0%
1.4.1 Sensor	11/08	6/09	3/09	8/09	0%	0%
1.4.2 FPHX	9/09	12/09	10/09	1/10	0%	0%
1.5.2 ROC	10/09	1/10	10/09	1/10	0%	0%
1.5.3 FEM	10/09	1/10	10/09	1/10		
1.4.3 HDI	1/09	3/09	6/09	9/09	0%	0%
Fabrication					0%	0%
1.6.3 Sensor wedge	4/09	11/10	10/09	3/11	0%	0%
1.6.2 Cage, disk	1/09	7/09	6/09	12/09	0%	0%
Operation	3/11	6/11	3/11	6/11	0%	0%

\*Sensor Design : design and manufacture prototype

\*\*FPHX Design : 1<sup>st</sup> round prototype designed

\*\*\*ROC/FEM Design : start with pre-production prototype, end with prototype produced, tested and approved

\*\*\*\*Mechanical Design : final design drawings completed

Summary of control milestones:

WBS Number	Control Milestone Name	Baseline Date	Actual/ Forecast Date
<b>WBS 1.1</b>	<b>DOE construction funds received</b>	<b>Q3 FY08</b>	<b>Q3 FY08</b>
<b>Accounts open</b>	<b>Accounts open</b>	<b>Q3 FY08</b>	<b>Q3 FY08</b>
<b>WBS 1.6.2.2.2</b>	<b>Review and Approve wedge, disk, cage design</b>	<b>Q3 FY08</b>	<b>Q3 FY08</b>
<b>WBS 1.4.3.2.5</b>	<b>HDI tested</b>	<b>Q3 FY08</b>	<b>Q2 FY09</b>
<b>WBS 1.4.1.2.3</b>	<b>Sensor prototype tested</b>	<b>Q1 FY09</b>	<b>Q1 FY09</b>
<b>WBS 1.4.1.2.5</b>	<b>First prototype wedge assembly</b>	<b>Q1 FY09</b>	<b>Q2 FY09</b>
<b>WBS 1.5.2.2.6</b>	<b>PHENIX system test complete</b>	<b>Q1 FY09</b>	<b>Q2 FY09</b>
<b>WBS 1.5.2.2.8</b>	<b>Review and Approve FEM and ROC</b>	<b>Q2 FY09</b>	<b>Q3 FY09</b>
<b>WBS 1.4.1.3.1</b>	<b>Sensor Procurement complete</b>	<b>Q3 FY09</b>	<b>Q3 FY09</b>
<b>WBS 1.4.1.2.6</b>	<b>Wedge assembly test complete</b>	<b>Q4 FY09</b>	<b>Q4 FY09</b>
<b>WBS 1.4.2.5.1</b>	<b>FPHX engineering run complete</b>	<b>Q1 FY10</b>	<b>Q1 FY10</b>
<b>WBS 1. 5.3</b>	<b>ROC and FEM production Complete</b>	<b>Q2 FY10</b>	<b>Q2 FY10</b>
<b>WBS 1.7.1.1</b>	<b>Disk Assembly begins</b>	<b>Q3 FY10</b>	<b>Q3 FY10</b>
<b>WBS 1.5.5.6</b>	<b>Install ancillary Equipment</b>	<b>Q4 FY10</b>	<b>Q4 FY10</b>
<b>WBS 1.7.1.1</b>	<b>Disk Assembly complete</b>	<b>Q1 FY11</b>	<b>Q1 FY11</b>
<b>WBS 1.7.2.1 ½</b>	<b>Cage Assembly finished</b>	<b>Q2 FY11</b>	<b>Q2 FY11</b>
<b>WBS 1.7.3</b>	<b>Install into VTX enclosure</b>	<b>Q2 FY11</b>	<b>Q2 FY11</b>
<b>WBS 1.7.3</b>	<b>Project Complete</b>	<b>Q3 FY11</b>	<b>Q3 FY11</b>