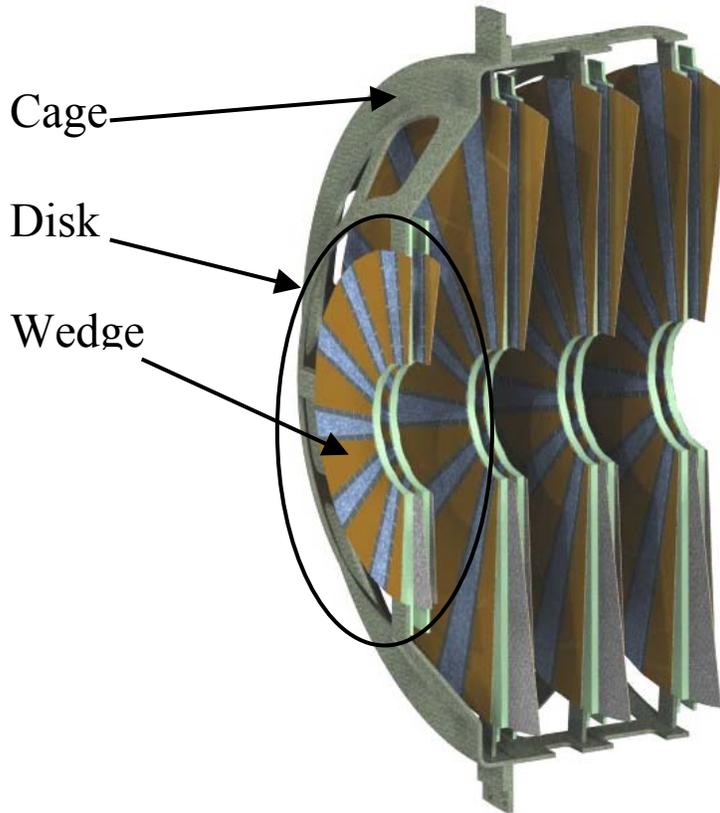


Project Name: PHENIX-FVTX
Federal Project Director:
Contract Project Manager: Melynda Brooks, LANL

Date: April, 2009

Reminder of some nomenclature:



Narrative of project highlights:

WBS 1.4.1, Sensor Prototyping: The sensors required for the FVTX project were specified, reviewed internally, and a request for quote for producing sensor prototypes as well as the production sensors was processed through the LANL purchasing department. The contract was awarded to Hamamatsu, and prototype sensors were delivered in October, 2008. Seventeen prototype FVTX sensors were delivered out of 20 requested – the shortfall was due to a manufacturing error. Hamamatsu performed quality acceptance testing on each sensor to ensure that they met our specifications criteria. All specifications were met or exceeded with the following single exception. The maximum resistance value of the polysilicon resistors on the sensors exceeded our maximum specification by about 5%. We accepted this exception because it has no negative impact on sensor performance. Work has been completed at the University of New Mexico to duplicate the Hamamatsu tests. No issues with the Hamamatsu results were found. If all testing of the sensors, and sensors with readout chips pass our qualifications, then the procurement of the set of production sensors is expected take place in Q3 FY09.

WBS 1.4.2, Silicon sensor readout chip (FPHX) prototyping: FNAL completed the design and layout of the FPHX in May 2008 and the chip was submitted to MOSIS June 2, 2008. The prototype chips were received at FNAL on August 21, 2008 where initial power-up and verification of analog output was performed after having a single chip wire-bonded to a test board. The chip was then carried to LANL for more detailed testing of the chip with a test stand which was developed at LANL. All download functionality was exercised, data read-back was performed, and the analog output was studied versus the various chip download parameters. The chip was found to have approximately 200 electrons of noise with no sensor attached, had thresholds which were uniform to within the same noise levels, and the analog output varied with chip download parameters as expected. The noise levels measured (under somewhat less than optimum conditions because several long wire-bonds were included in the setup), can be compared to $115 e + 134 e/pf$ expected noise levels, based on simulations from the FNAL chip designers. According to the analog engineer, the 200 electrons of measured noise is consistent with the expected baseline noise plus the extra capacitance that is introduced on the front end due to our setup.

Full analog tests which fully exercised all chip download parameters were performed by the analog engineer, Tom Zimmerman of FNAL, and he found the chip to fully perform as expected. Tom has however suggested that he can change the physical layout of the chip in such a way as to reduce threshold dispersion among the channels of the chip. We expect to take advantage of this possibility for redesign since he says it is a straight-forward change for the chip.

The digital portion of the chip was further exercised at LANL to check for beam-clock and hit output stability. The chip was pulsed several hundred thousand times with fixed amplitude, fixed spacing between pulses, and fixed numbers of channels unmasked. The data was then checked to see that the ADC output, beam clock number (which should be fixed for these data sets) and channel ID were stable across the entire data set. The relative timing of the pulsing with respect to the beam clock edge was also varied. It was found in these tests that there is an error in the digital chip logic that causes a fraction of beam clock numbers to march out of time when a large number of channels fire at once and when the pulse is near the beam clock edge. The digital designer, Jim Hoff, has since diagnosed the logic problem with the chip and the design fix has been produced and simulated.

We have also begun testing the chips with one or multiple chips mounted onto and HDI, and bonded or not bonded to a sensor. One additional design problem was uncovered when we went through some extra effort to make our test stand always pulse the chip on a given beam clock, by resetting the chip clock counter a fixed time before issuing pulses. When we did this, we found that the beam clock number that was produced by the chip had one of two values, rather than a single value. We have passed this information on to Jim Hoff and he has promised to get back to us once he compares the problem we have with the design that he implemented.

A set of all chip modifications required between this round and next round has been transferred to FNAL. All of the digital design fixes have been implemented, with the exception of the newly uncovered clock counter reset problem. The analog fixes that are required are considered to be relatively minor and we have been told by FNAL that they will be completed by the middle of May, 2009.

WBS 1.4.3, HDI: The kapton HDI layout was completed by UNM and submitted to Dyconex for manufacture. The first prototype HDIs were delivered to UNM March 5, 2009. The bare HDIs were visually inspected and electrically tested to make sure that they matched the schematics and no issues were uncovered. We then sent a few HDIs to FNAL to have one chip bonded to one HDI and, after the single chip readout was verified to work, we had 13 chips plus a sensor bonded to another HDI. Testing on the 13-chip assembly has been slow because (1) there appears to be a high resistance connection between the sensor bias and ground, which we believe arose because the kapton HDI had holes punched through the middle (by Dyconex) and the conductive epoxy connection between the sensor bias and the HDI bias was placed over one of these holes. We believe that through this hole, some indirect connection to ground has possibly been achieved. We are currently trying to determine how much testing can be accomplished without sensor bias (in this case the chip will assuredly look noisy), how much bias we can apply even with the resistive connection to ground, and whether we can get another HDI assembled which will not have a sensor biasing issue.

Following our November 2008 FVTX Annual Review, we agreed to in parallel develop a PCB-version HDI so that earlier sensor-readout chip system tests could potentially be performed so that we would be less likely to incur additional schedule delays if the more complex kapton HDI 1st round prototype was not fully functional. The design of this PCB HDI was completed, HDIs were delivered, and we are currently having some chips and sensors bonded to PCB HDIs. We hope that with this version of the HDI we will have no sensor biasing issues and can carry out testing of multiple chips more straight-forwardly.

WBS 1.5, DAQ development: The first round ROC prototype board has been assembled and was delivered to LANL by the week of January 11, 2009. The board underwent basic power-up tests by the engineer and was then passed to LANL physicists for more complete tests. We have been exercising the ROC board to read out single chips and the assembled HDI wedges continuously for several weeks. We uncovered several minor issues with the board which we were able to patch on the board we have on hand, and the design fixes have already been incorporated into the next rev design.

This first round prototype ROC board has all the functionality needed for the FVTX detector, but is physically configured to read out our LDRD detector planes. The layout work for a version needed to read out FVTX planes is in progress at LANL. The first round FEM board layout is also in progress. A clock distribution board, which will be needed in the Interaction Region, between the counting house and the

ROC boards, has been designed, laid out, and procured, but not tested yet. One remaining board, a slow controls interface board which will sit in the FEM VME crates, remains to be designed.

WBS 1.6, Mechanical Design: Final design drawings of the backplane, disk, and cage designs have been completed, pending final review. Some additional work needs to be completed on the final construction drawings before procurement can be made on the disks and cage. A backplane prototype was procured from FNAL and a cage prototype will be procured from LBNL. Cost estimates from LBNL for production backplanes are somewhat less than our project estimates, and the estimate for the cage currently appears to be within the project estimates. Rapid prototype versions of the cage and disks were purchased and will be used to test out assembly procedures.

WBS 1.4 and 1.7, Assembly Plans: After a visit to the FNAL SiDet laboratory, it was decided to pursue having wedges assembled at SiDet rather than at an FVTX institution(s). SiDet received \$15k of construction funds to allow them to work on assembly fixtures and assembly of our first wedge prototypes. SiDet worked with HYTEC and Walter Sondheim to design assembly fixtures, and these have been manufactured and were used at SiDet with mock-up wedge components, and with the real prototype wedges. A few modifications to fixtures were requested after the prototype wedges were assembled, and updated drawings have been produced. New fixtures will be manufactured once we are confident that no further modifications are needed.

Steve Pate, of NMSU has advanced the disk and full detector assembly plans and is taking a sabbatical at BNL from August 2008 – May 2009 to make preparations of detector assembly areas. Steve has worked with Ed O'Brien to identify lab space for assembly and has selected two rooms at BNL. Equipment for assembly and testing tasks is being identified so the rooms can be made fully functional and ready for disk assembly and testing while Steve is at BNL.

WBS 1.8, Systems Integration – Walter Sondheim, LANL, has continued to provide the mechanical integration for the project, working with HYTEC on the mechanical design and working with the VTX group to ensure that the VTX and FVTX detectors are compatible with each other inside the enclosure. Eric Mannel has provided the electrical integration for the project, coordinating our electrical reviews, and working with the groups to provide a detailed grounding & shielding plan.

Control milestones covered during review period:

1) **Milestone description:** HDI tested

Forecast vs actual start/completion date: forecast Q3 FY08, actual Q2 FY09

Milestone result or impact of delay to project: Tests of the HDIs are in progress. The delivered HDIs passed tests of the implementation of the schematics, and clock propagation was tested on a bare HDI and found to be acceptable. The completion of

tests currently hinges on our ability to get full readout with a biased sensor. We have readout to a chip on the HDI working, but the sensor on our one assembled wedge has not been fully biased because of a resistive path that was found between the sensor bias and analog ground. We expect that a new wedge will need to be assembled to fully complete our HDI tests. Completion is anticipated in Q3FY09.

- 2) **Milestone description:** Sensor Prototype tested
Forecast vs actual start/completion date: forecast Q1 FY09, actual Q1/Q2 FY09
The first prototype sensor was delivered, and fully tested by Hamamatsu in Q1 FY09. Verification tests were performed at the University of New Mexico and no issues were uncovered. This milestone is complete.
- 3) **Milestone Description:** First prototype wedge assembly complete.
Forecast vs actual start/completion date: forecast Q1 FY09, actual Q2 FY09
The first wedge assemblies have been made and are currently under test.
- 4) **Milestone Description:** PHENIX system test complete.
Forecast vs actual start/completion date: forecast Q1 FY09, actual Q2/Q3 FY09
The full system test is still underway. We expect this milestone to be completed in Q3 FY09.
- 5) **Milestone Description:** Review and approve FEM and ROC.
Forecast vs actual start/completion date: forecast Q3 FY09, actual anticipated Q4 FY09
The ROC and FEM design work has been delayed both because funding was diverted away from these tasks in FY09 and because the electrical designer availability within the project is limited enough to not allow them to progress as quickly as projected when we simultaneously had other electrical design projects in progress (PCB HDI design, etc.) The 2nd round ROC and 1st round FEM are still in progress. If we are able to secure enough electrical design effort, we could hope to have both boards out for procurement in Q3 FY09 and reviewed in Q4 FY09.
- 6) **Milestone Description:** Sensor procurement complete.
Forecast vs actual start/completion date: forecast Q3 FY09, actual expected to begin Q3 FY09, completed perhaps in Q4 FY09.
The sensor procurement waits for the completion of wedge tests. Once we are satisfied with the wedge tests, we will give the go-ahead for sensor procurement. We expect that to take place in Q3FY09 and need to receive Hamamatsu's re-bid for production to give an end-date for procurement.

Brief summary of project issues, concerns, successes:

Our primary concern at this date is whether we can complete all wedge tests in a timely manner. Our critical path depends upon us completing these tests but progress has been slow due to unforeseen issues with sensor biasing on the kapton HDI and unforeseen issues with making an interconnect between the kapton HDI and the DAQ system. We are actively working to solve the particular kapton HDI issues and at the same time move forward on tests with a PCB version of the HDI to keep tests progressing.

Across the project we are having difficulties maintaining the staffing levels we need for electrical design work. The engineering work and the physicist liaison work are being accomplished in a timely manner for the most part, but board layout has been hampered by unavailability of designers or designers who are not as skilled at board layout as needed to produce articles in a timely manner. We are actively searching for a solution to this problem, across the laboratory and across the participating FVTX institutions.

The FPHX digital redesign work was completed in a very timely manner by FNAL engineer Jim Hoff, and the analog redesign work is expected to be completed shortly. This removes one important schedule concern from our critical path.

We are very happy to hear that the full funding for the FVTX project will become available to us shortly. With the addition of these funds to the project, we can look forward to not having any funding issues holding up the project's progress.

The status of cost and schedule is summarized below.

Summary of total expenditures:

A WBS	B ITEM	C Baseline Total Cost (AY\$)	D Costed & Committed (AY\$)	E Estimate to Complete (AY\$)	F Estimated Total Cost (AY\$)	G Baseline Contingency (AY\$)	H Remaining Contingency (AY\$)
1.4.1	Wedge Sensors	1118	116	775	891	206	227
1.4.2	FPHX Chip	692	149	453	602	174	89
1.4.3	HDI	194	35	224	259	39	-64
1.4.4	Flex Cables	70	0	62	62	9	7
1.4 Total		2074	300	1514	1814	428	260
1.5.1	Fiber	21	0	19	19	3	2
1.5.5	Ancillary	246	0	116	116	23	130
1.5.2	ROC	615	44	500	544	139	72
1.5.3	FEM	578	2	433	435	130	143
1.5 Total		1461	46	1068	1114	295	348
1.6.2	Cage	174	72	125	197	35	-23
1.6.3	Wedge Backplane	188	7	56	63	38	125
1.6.4	Support Disk	114	8	78	86	23	28
1.6.5	Jigs	80	15	45	60	15	20
1.6 Total		555	101	305	406	110	149
1.7	Assembly	42	10	23	33	8	9
1.8	Integration	500	66	321	387	58	113
1.9	Management	249	66	152	218	28	31
Total		790	142	496	638	94	152
Grand Total		4881	589	3383	3972	927	909

The expenditures that have changed since the Management Plan, and how we will cover them are listed here:

- We have shifted part of the FPHX testing funds (\$30k) from FNAL to LANL since the FNAL engineers have been only minimally available for testing and Jon Kapustinsky has been instead coordinating these efforts. Since we currently expect only ~\$90k of the \$145k of funds allocated for FPHX prototype I work at FNAL to be invoiced, we believe this cost is still covered under the FPHX Management Plan costs as listed.
- A total of \$30k of sensor testing costs are also being transferred to LANL to cover efforts by Jon Kapustinsky to oversee the testing. This fits within the total sensor testing budget in the Management Plan.
- Following our FVTX Annual Review, we agreed to add a new task to our project: develop and procure a PCB-version HDI to allow sensor and readout chip testing at an earlier date. We estimate this task to cost \$40k.
- Clock and DAQ interface boards were not specifically called out in our initial estimate of the DAQ system. As the design evolved, we realized these boards should be separate boards from the ROC/FEM boards. Only a few boards are needed and the design/prototype work is estimated to cost \$40k. We do not have enough cost information yet to know if this fits within the ROC/FEM design and production costs as already listed in the Management Plan.
- \$37k has been added for ROC FPGA programming and testing of prototype boards.
- We share the costs with the VTX group for Eric Mannel's time for his job of Electrical Integration Manager for the FVTX and VTX projects. We have spent less for WBS 1.8 than was expected in the Management Plan because we budgeted for close to his full salary but paid a smaller fraction because of our cost sharing. For FY08 and FY09 we have spent \$61k less than budgeted for this task and will use this savings to cover some of the above added costs.
- We added \$30k to the cost to complete the mechanical design work on the cage, backplane and disks, based on updated costs from HYTEC.
- We got a manufacturer's quote on production HDIs. The quote fits within the cost+contingency that we had allocated for the HDIs, but is more than the original cost estimate alone.
- We estimate we have \$909k remaining contingency, compared to \$927k baseline contingency, after all the added costs and savings have been included in the project.

Summary of expenditures by FY:

	FY 2008	FY 2009	FY 2010
a) Funds allocated	\$500k	\$2200k	
b) Costs accrued	\$144.4 k	\$188.7k	
c) Uncosted commitments	\$264.7 k	\$197.3k	
d) Uncommitted funds (d=a-b-c)	\$90.9	\$1814k	
e) Remaining total contingency			

Summary of schedule:

	Baseline Start Date mo/year	Baseline Completion Date mo/year	Forecast Start Date mo/year	Forecast Completion Date mo/year	% Complete Baseline	% Complete Actual
Design						
1.4.1 Sensor*	4/08	7/08	6/08	10/08	100%	80%
1.4.2 FPHX**	10/07	4/08	10/07	5/08	100%	100%
1.5.2 ROC***	12/08	4/09	12/08	4/09	75%	25%
1.5.3 FEM	12/08	4/09	12/08	4/09		
1.4.3 HDI	4/08	8/08	6/08	11/08	100%	95%
1.6.2 Cage****, 1.6.3 wedge, 1.6.4 disk	4/08	10/08	4/08	10/08	100%	95%
Procurement						
1.4.1 Sensor	11/08	6/09	3/09	8/09	50%	0%
1.4.2 FPHX	9/09	12/09	10/09	1/10	0%	0%
1.5.2 ROC	10/09	1/10	10/09	1/10	0%	0%
1.5.3 FEM	10/09	1/10	10/09	1/10		
1.4.3 HDI	1/09	3/09	6/09	9/09	100%	0%
Fabrication					0%	0%
1.6.3 Sensor wedge	4/09	11/10	10/09	3/11	0%	0%
1.6.2 Cage, disk	1/09	7/09	6/09	12/09	40%	0%
Operation	3/11	6/11	3/11	6/11	0%	0%

*Sensor Design : design and manufacture prototype

**FPHX Design : 1st round prototype designed

***ROC/FEM Design : start with pre-production prototype, end with prototype produced, tested and approved

****Mechanical Design : final design drawings completed

Summary of control milestones:

WBS Number	Control Milestone Name	Baseline Date	Actual/Forecast Date
WBS 1.1	DOE construction funds received	Q3 FY08	Q3 FY08
Accounts open	Accounts open	Q3 FY08	Q3 FY08

WBS 1.6.2.2.2	Review and Approve wedge, disk, cage design	Q3 FY08	Q3 FY08
WBS 1.4.3.2.5	HDI tested	Q3 FY08	Q2 FY09
WBS 1.4.1.2.3	Sensor prototype tested	Q1 FY09	Q1 FY09
WBS 1.4.1.2.5	First prototype wedge assembly	Q1 FY09	Q2 FY09
WBS 1.5.2.2.6	PHENIX system test complete	Q1 FY09	Q3 FY09
WBS 1.5.2.2.8	Review and Approve FEM and ROC	Q2 FY09	Q4 FY09
WBS 1.4.1.3.1	Sensor Procurement complete	Q3 FY09	Q3 FY09
WBS 1.4.1.2.6	Wedge assembly test complete	Q4 FY09	Q4 FY09
WBS 1.4.2.5.1	FPHX engineering run complete	Q1 FY10	Q1 FY10
WBS 1. 5.3	ROC and FEM production Complete	Q2 FY10	Q2 FY10
WBS 1.7.1.1	Disk Assembly begins	Q3 FY10	Q3 FY10
WBS 1.5.5.6	Install ancillary Equipment	Q4 FY10	Q4 FY10
WBS 1.7.1.1	Disk Assembly complete	Q1 FY11	Q1 FY11
WBS 1.7.2.1 ½	Cage Assembly finished	Q2 FY11	Q2 FY11
WBS 1.7.3	Install into VTX enclosure	Q2 FY11	Q2 FY11
WBS 1.7.3	Project Complete	Q3 FY11	Q3 FY11