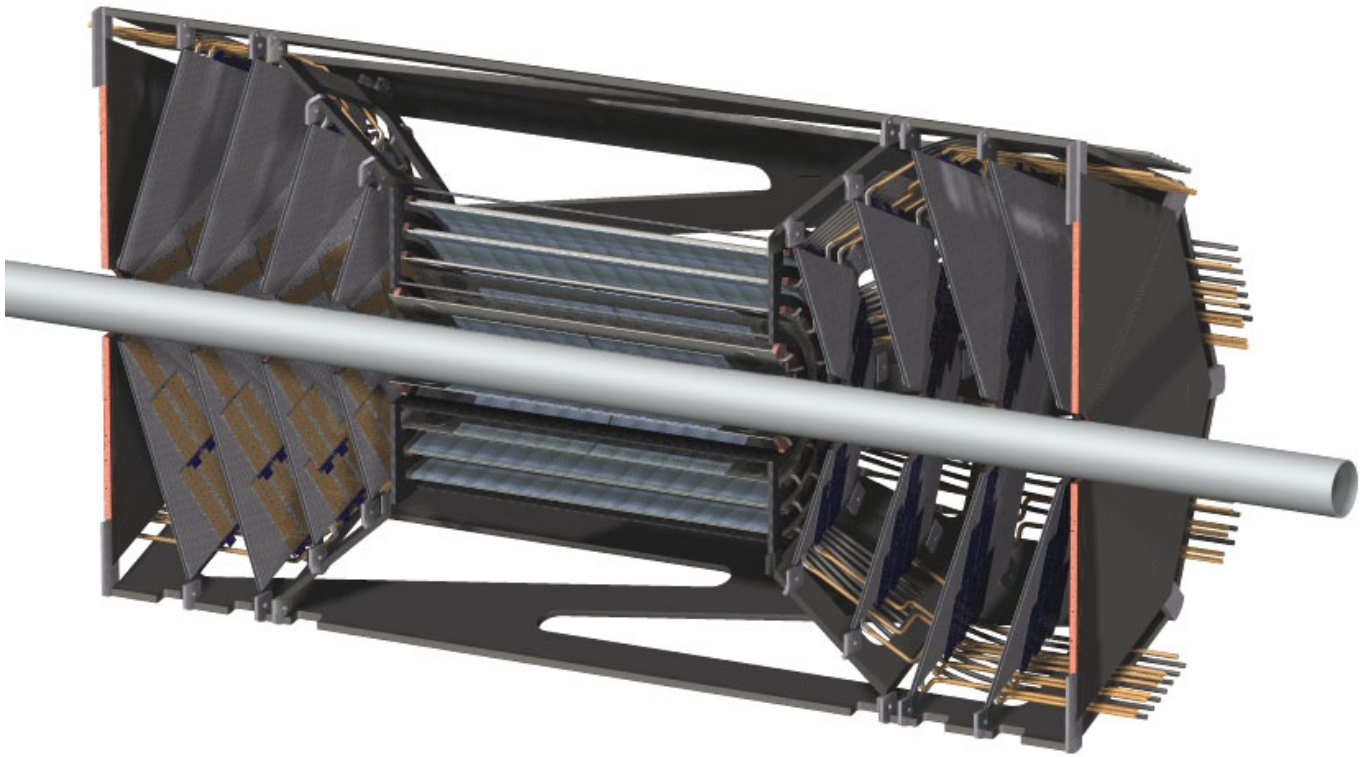
Silicon Vertex Detector Upgrade

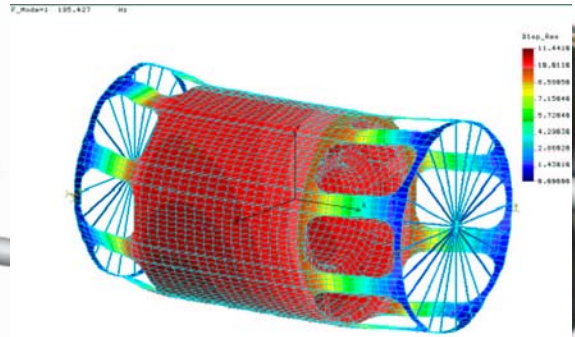
Endcaps

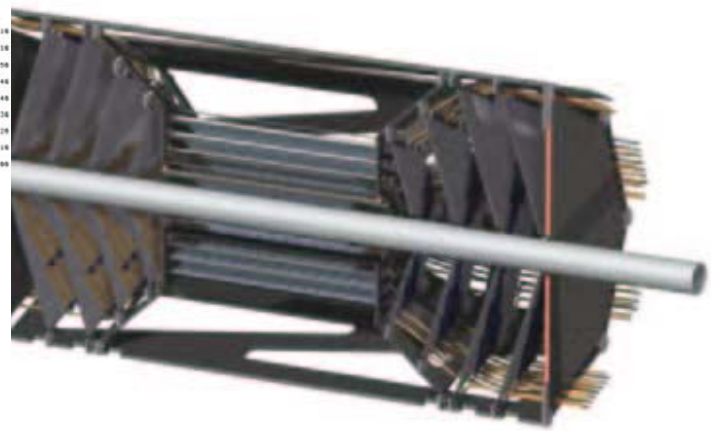


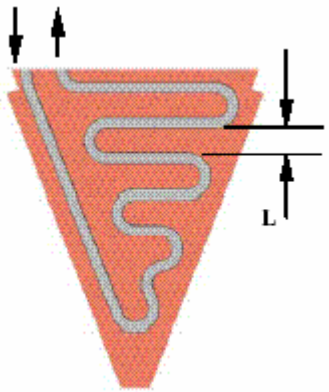
Status of the End Cap Silicon Upgrade
(or it's still a paper tiger)

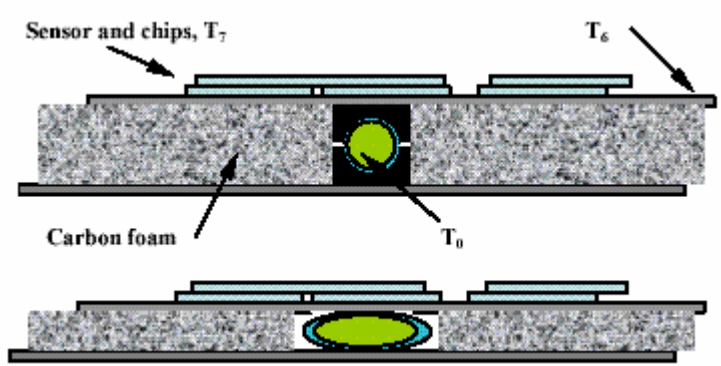
- LOI submitted Mar 2003
- Conceptual Mechanical Design HYTEC– Jan 2003
- Conceptual Electronic Design FNAL – June 2003
- First Pass Simulations – 2002-2003

Silicon Tracker Upgrade
Mechanical Conceptual Design Studies

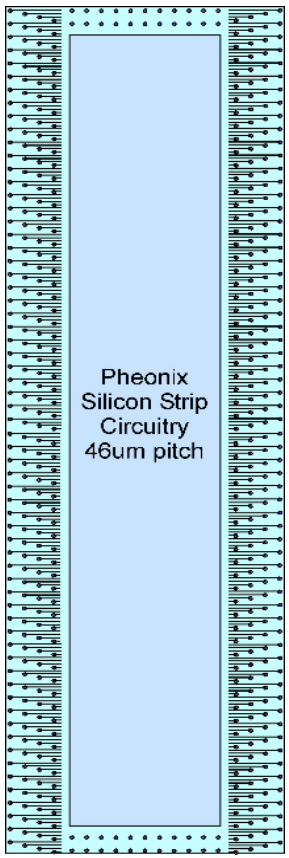








Silicon Tracker Upgrade
Proposed PHX chip by Ray Yarema



Phenix Chip Layout:

2 columns

256 channels/column

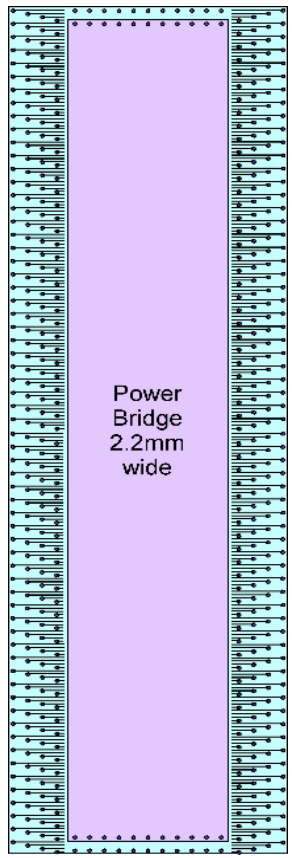
3.8 mm x 13 mm = 49.4 mm^2

Bump bonds on 200 um pitch

50 µm diameter bumps

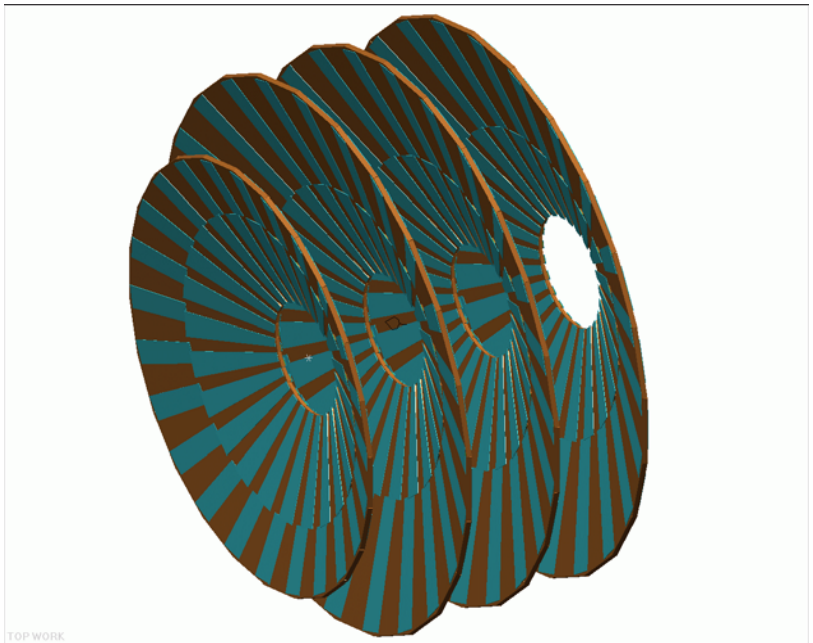
512 bumps plus inter-chip bumps

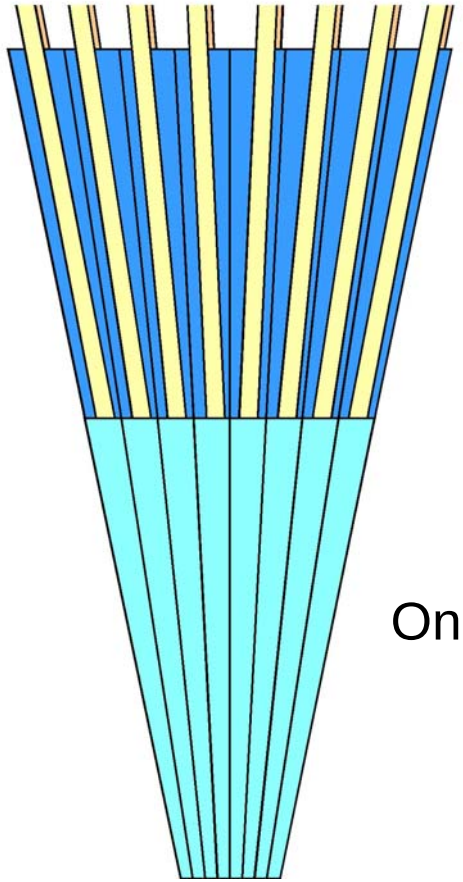
Simulated noise performance is < 250 electrons



Wedge Assembly Idea

Go to 16 wedges/lampshade to reduce the size of silicon detector pieces and sub assembly size for better yields





One wedge

Silicon Tracker Upgrade

Benefits of using the Modified FPIX2 chip in the Endcap ministrips

Allows us to tailor strips to keep occupancy low

Low noise

Low power – simplifies mechanics

Can provide trigger, if desired

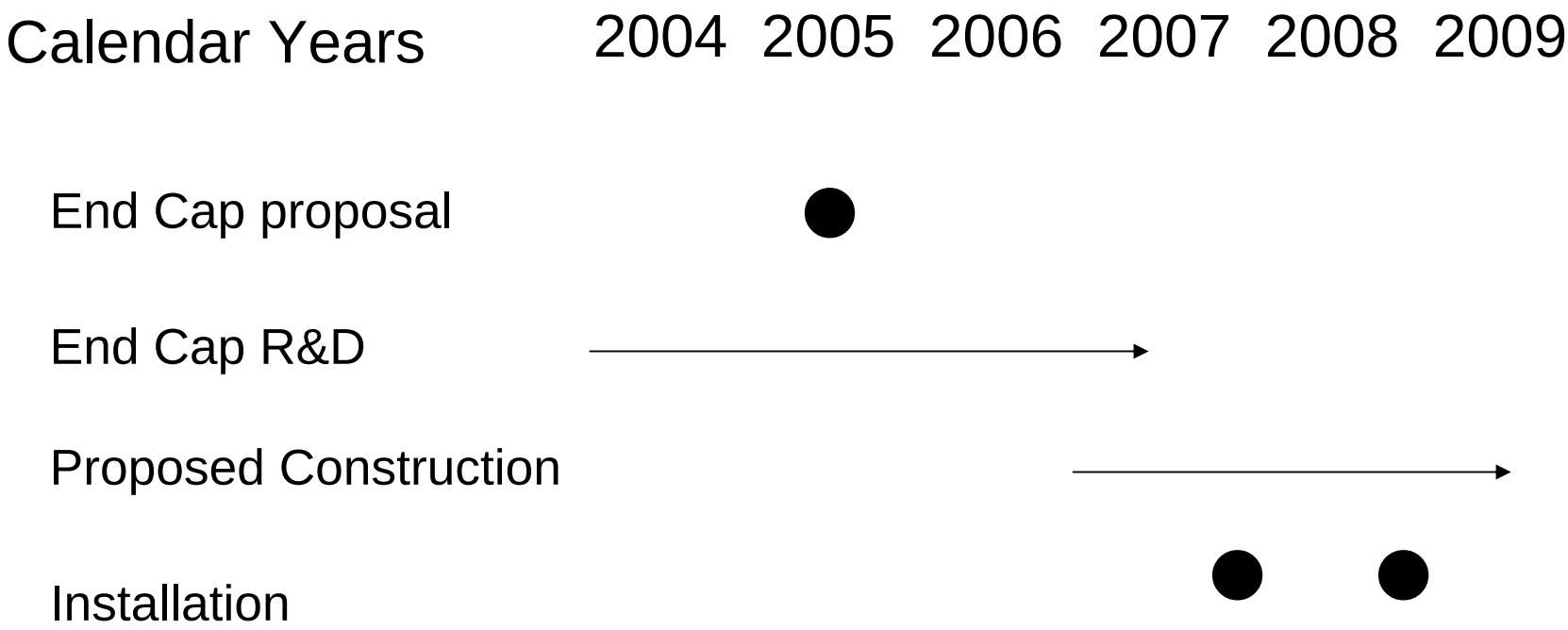
Room temperature operation - simplifies mechanic

Integrated bus is very attractive

Future Plans for End Cap Silicon

- Procure and test Btev chip and sensor assemblies – this summer
- Obtain Heidelberg readout chip and attach to the Btev assemblies. Test complete functionality – Fall 2004
- Initiate Electronic R&D with FNAL – Fall 2004
- Initiate Mechanical R&D with HYTEC – Fall 2004
- Prepare proposal for BNL – Spring 2005

Schedule


Calendar Years
2004
2005
2006
2007
2008
2009
End Cap proposal
End Cap R&D
Proposed Construction
Installation

DOE Costs Per Year

	FY04	FY05	FY06	FY07	FY08	FY09
Barrel R&D	150K	200K				
BNL Operations Equipment		280K				
Barrel Proposed DOE construction			2800K	2000K	400K	
Endcap R&D	100K	250K	320K	150K		
Endcap Proposed* DOE construction				2050K	2050K	2050K

* Includes ~ $1.1M for Lvl 1 trigger and 50% contingency