Multi-Event Buffering

For PHENIX Muon Tracking System

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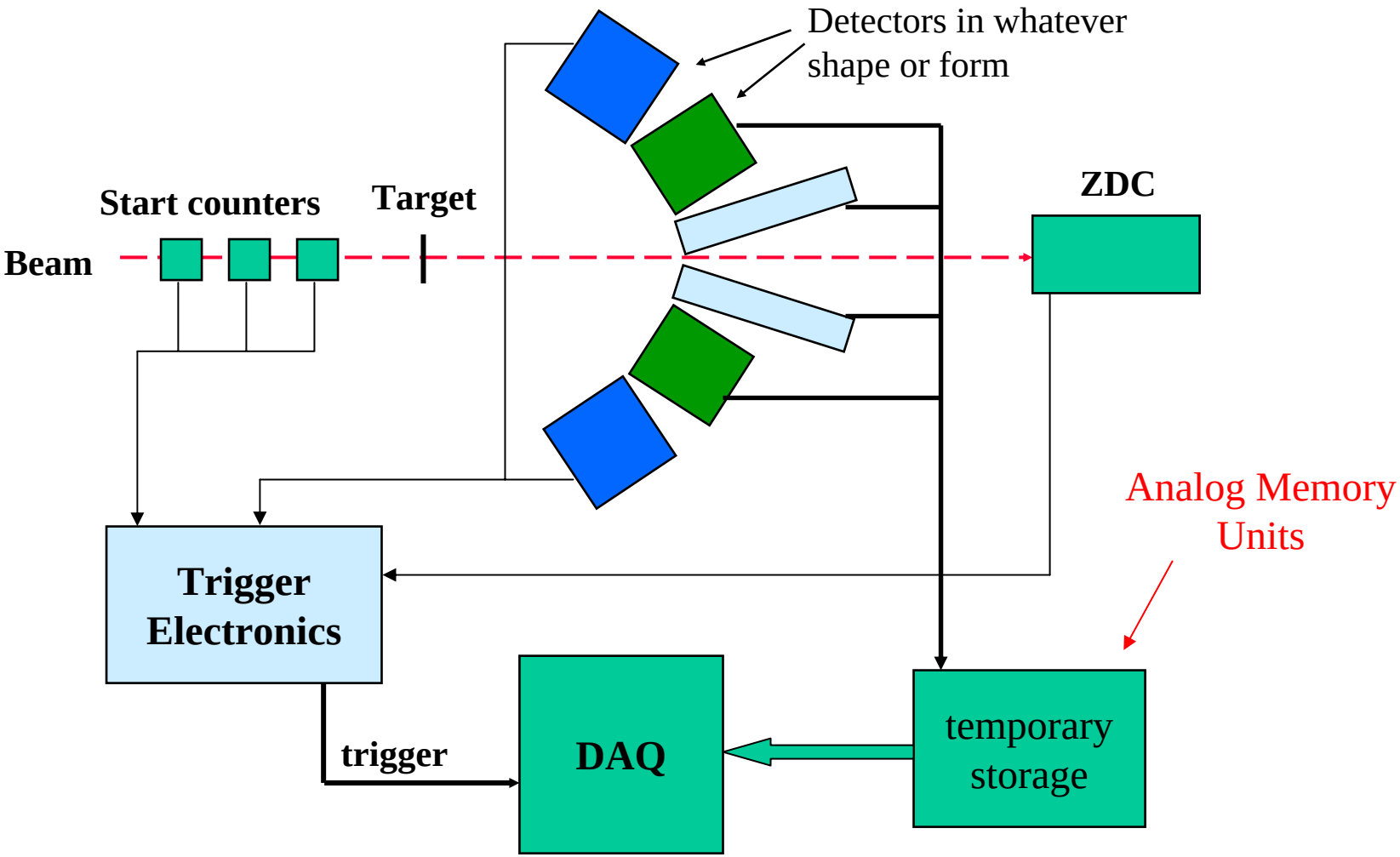
Outline

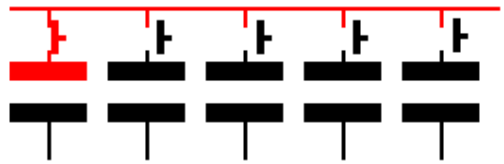
1. Multi event buffering.
2. Bench test results.
3. Online monitoring.
4. Current status.

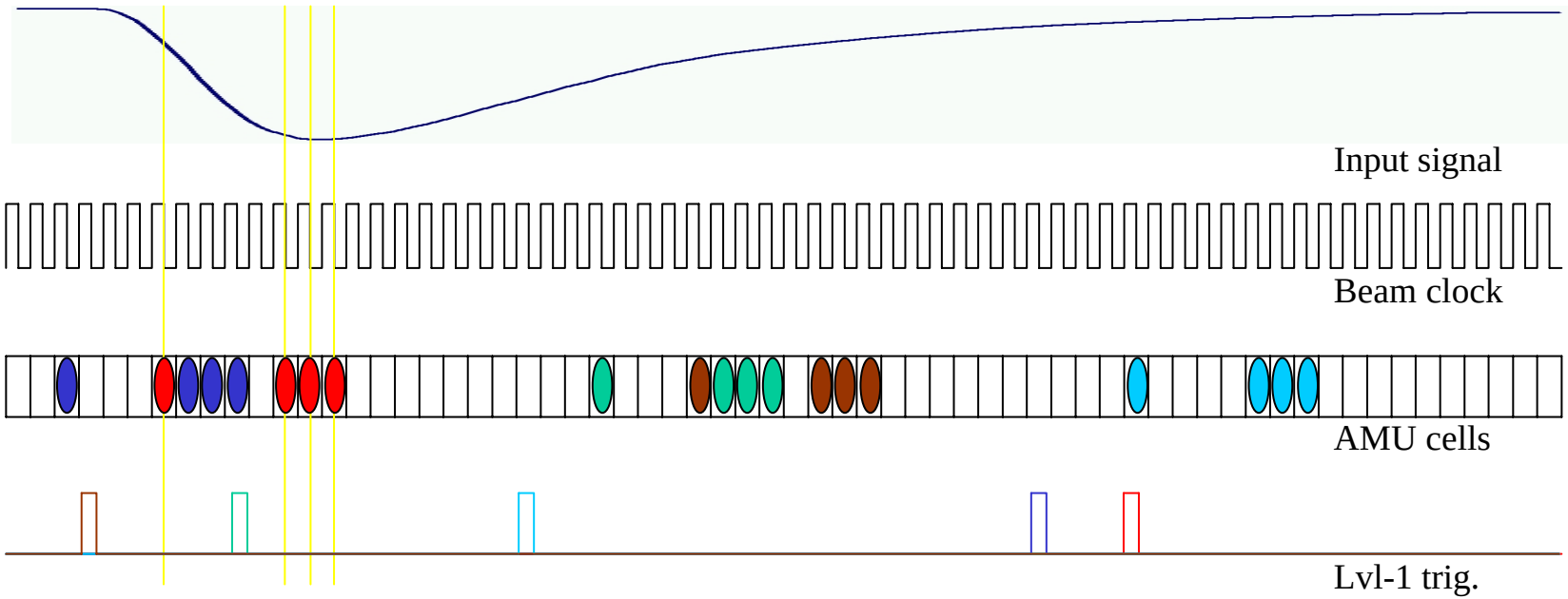
some facts….


Detectors in whatever
shape or form
Start counters
Target
ZDC
Beam
Trigger
Electronics
Analog Memory
Units
trigger
DAQ
temporary
storage

Analog Memory Units

Signal samples are stored in Analog Memory Units. On Level 1 trigger, signal from corresponding unit is digitized.

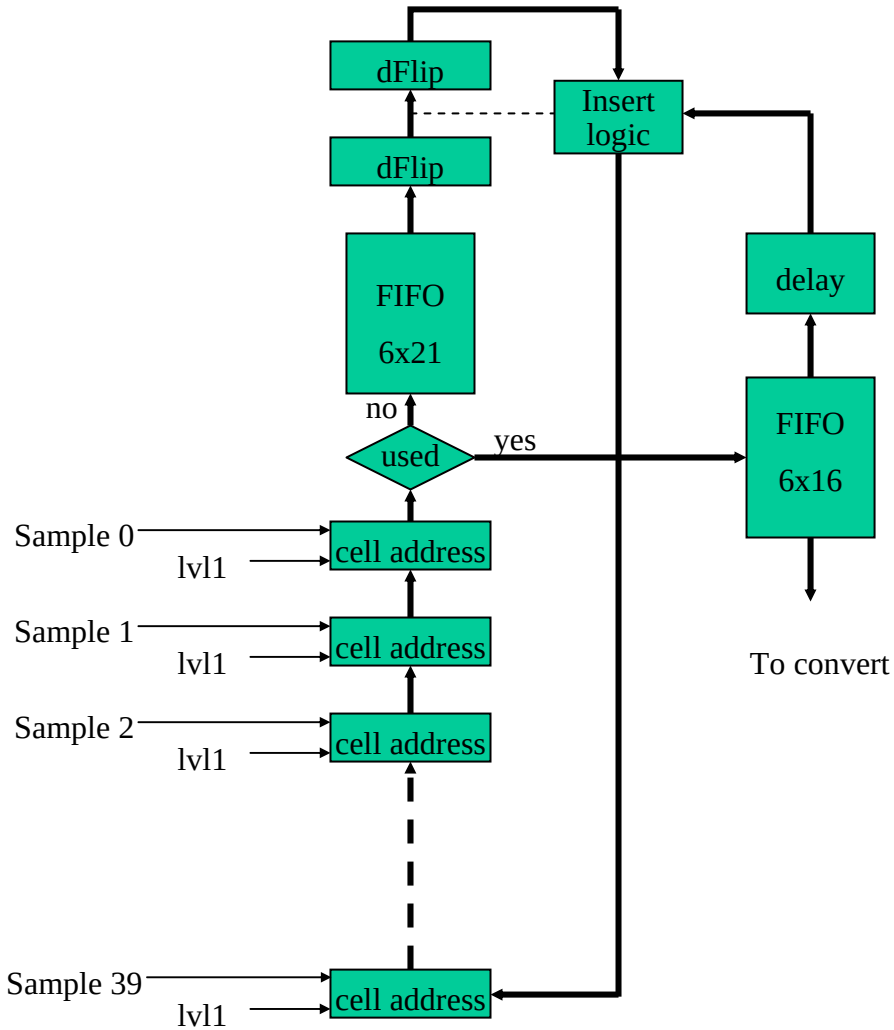




MuTr Front End Electronics

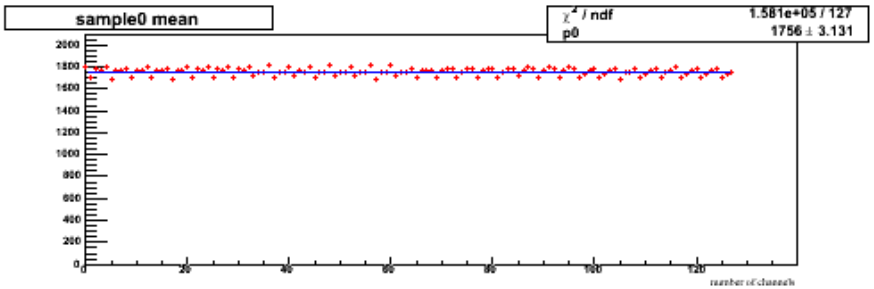
- Each data “packet” contains 128 channels
  - 2 Cathode Read Out Circuit Boards, 4 AMU/ADC chips.
  - 1 Controller Board, FPGA chip,
- FPGA code contains:
  - Timing logic, AMU cell manager, etc….
- Current FPGA code (ver. 124) cannot handle Multi-event buffering.
- New FPGA code (ver. 139) worked perfectly on test bench.

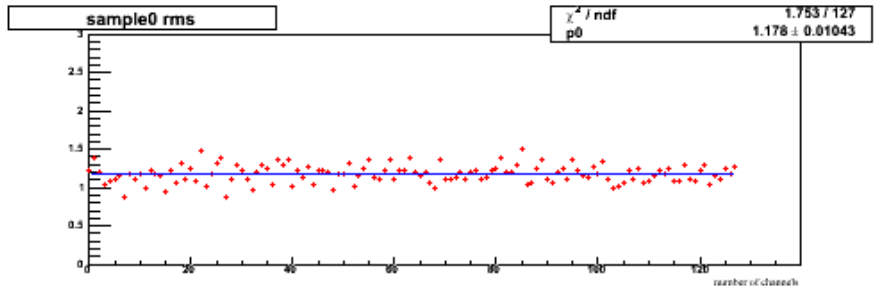
AMU Cell Manager

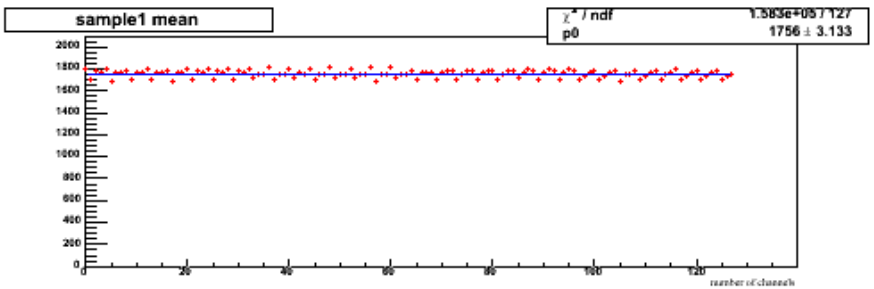


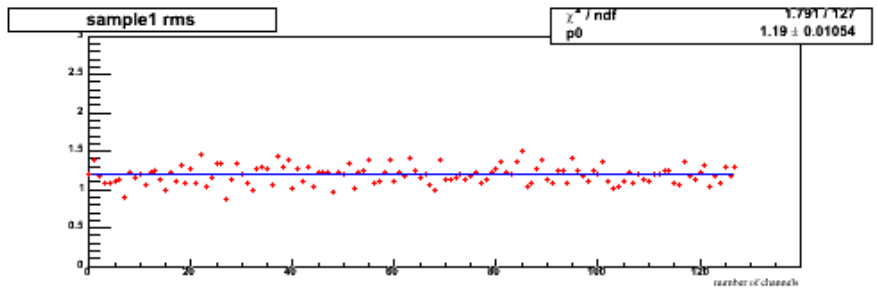
Conversion Time

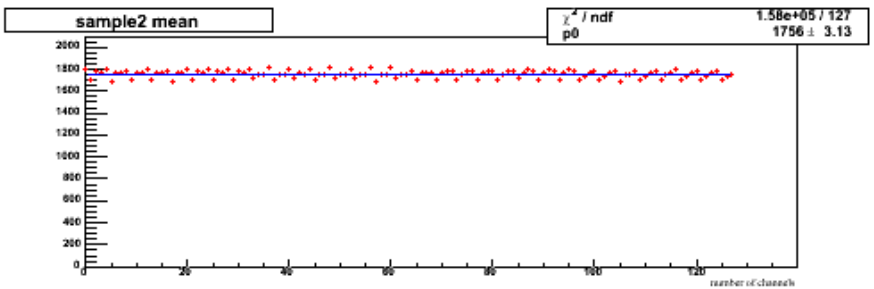
single event; random triggers.

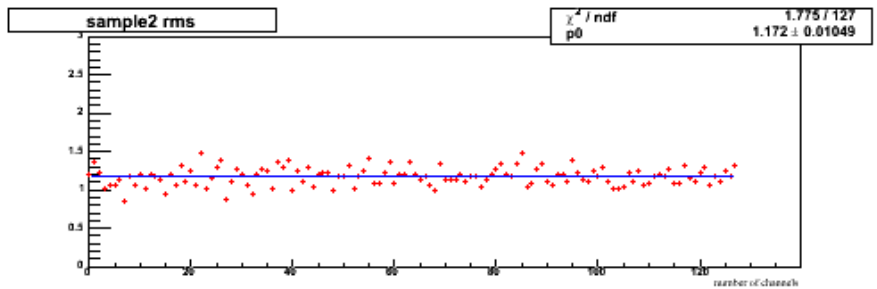


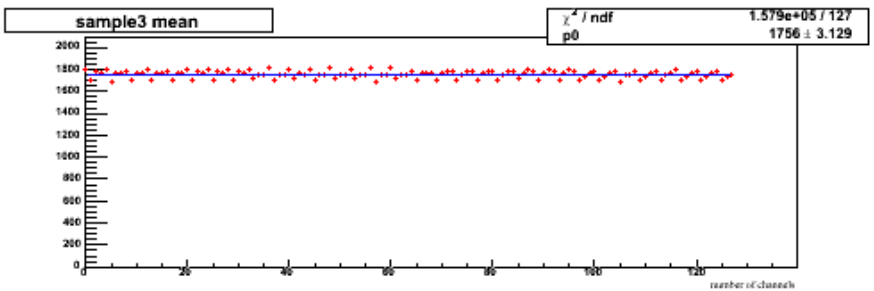


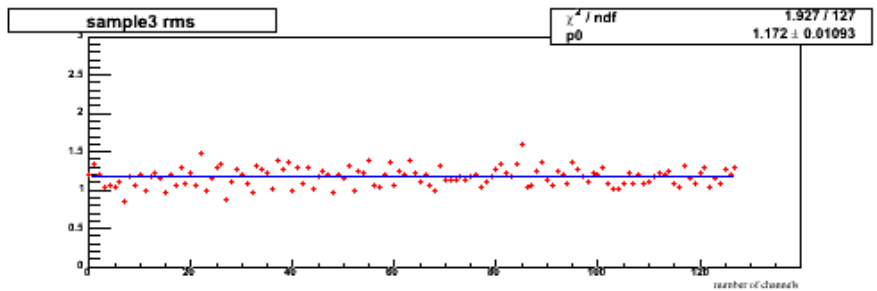




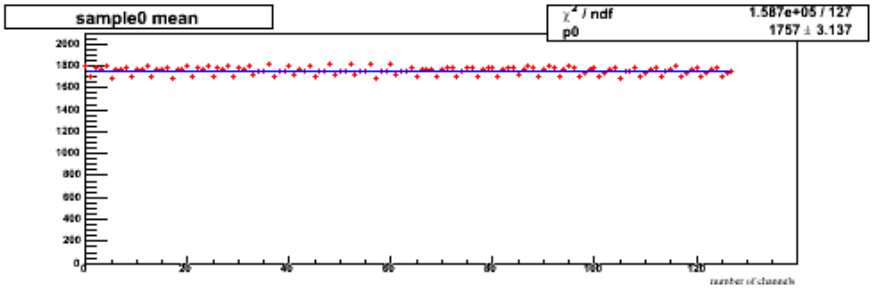


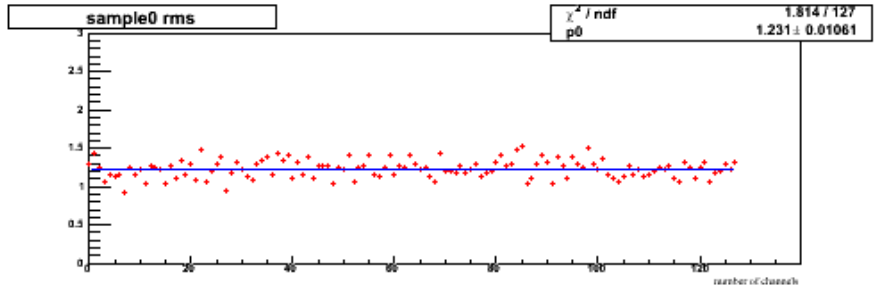


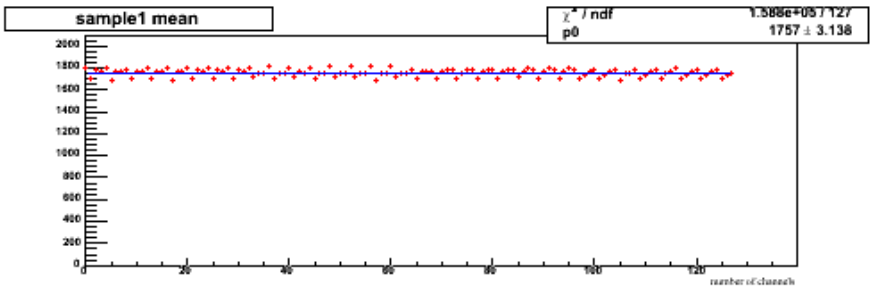


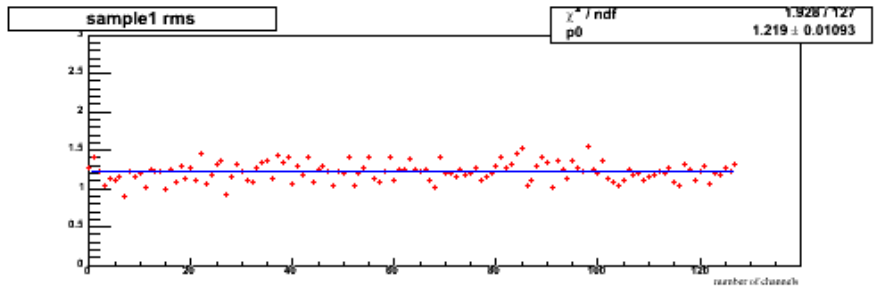


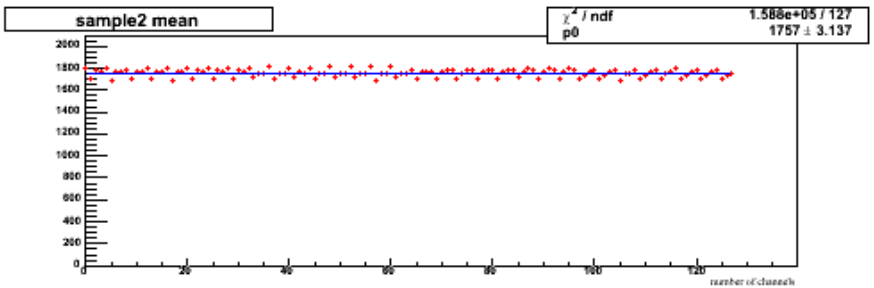
5 event buffering, random triggers.

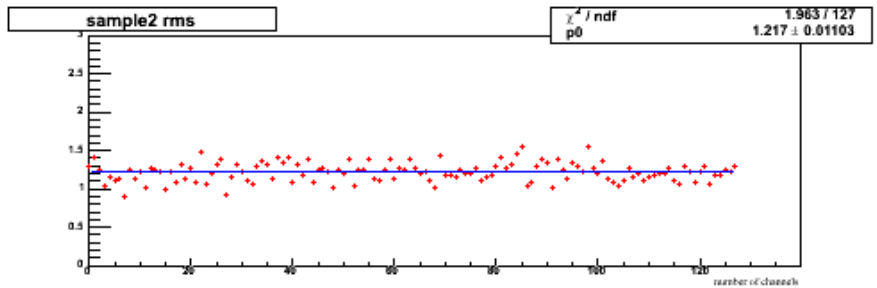


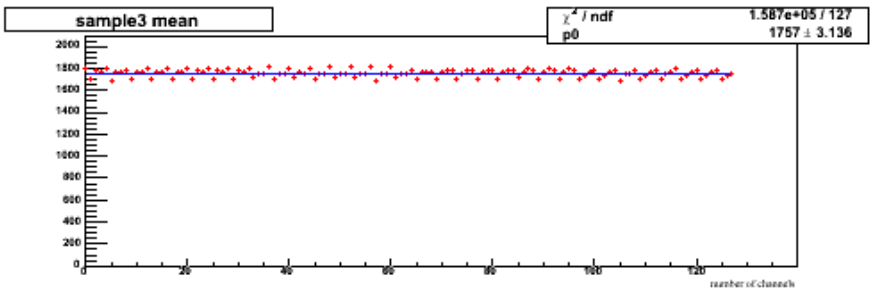


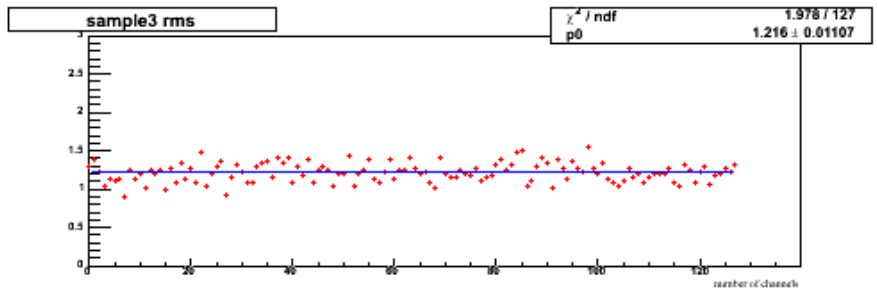




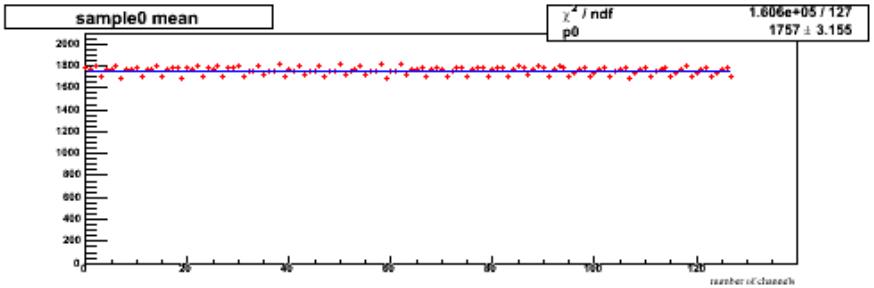


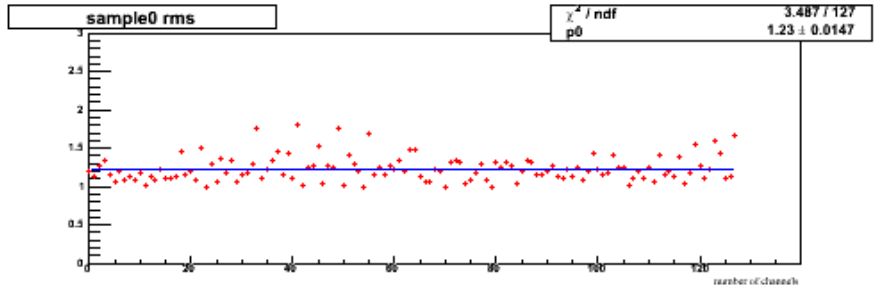


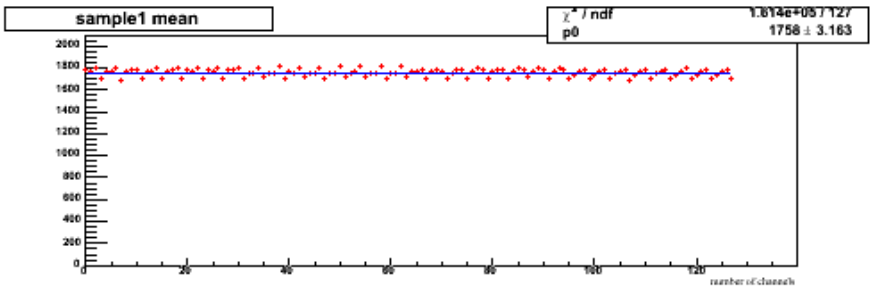


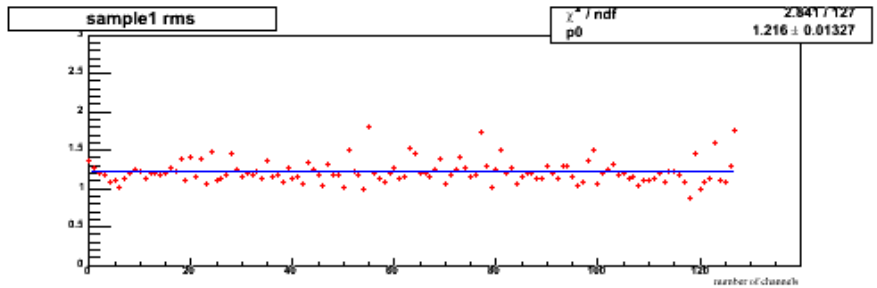


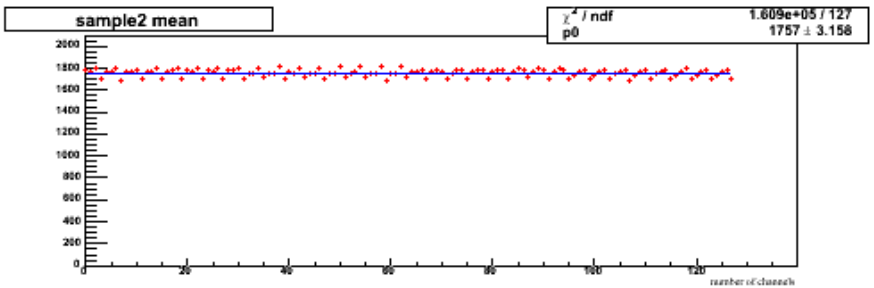
4 even buffering, at 1Hz.

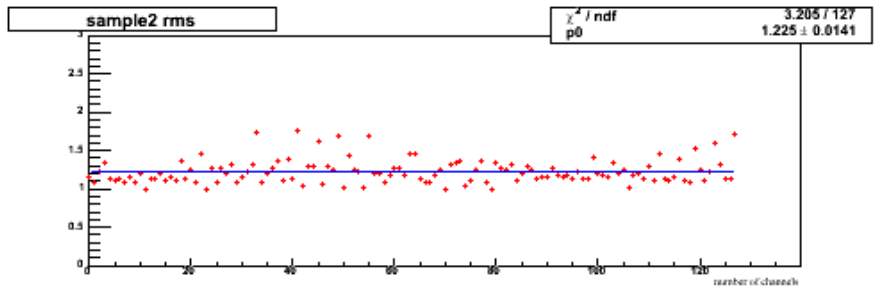


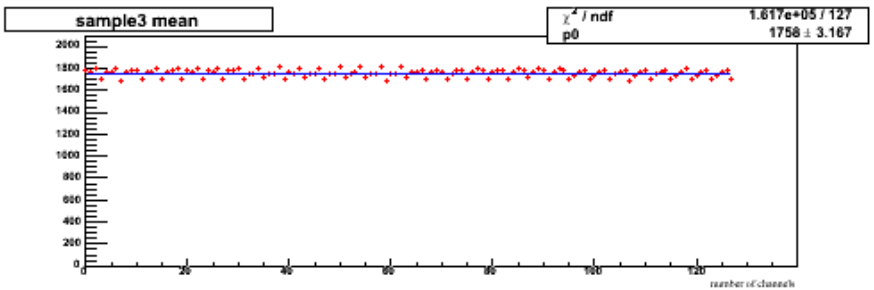


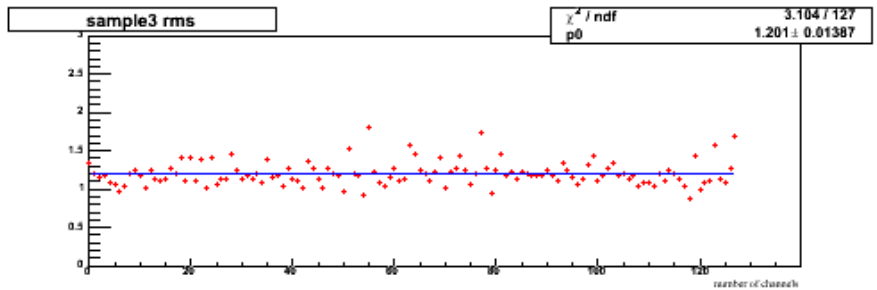




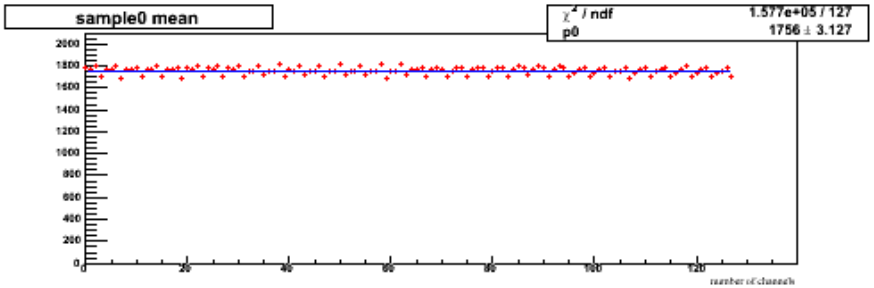


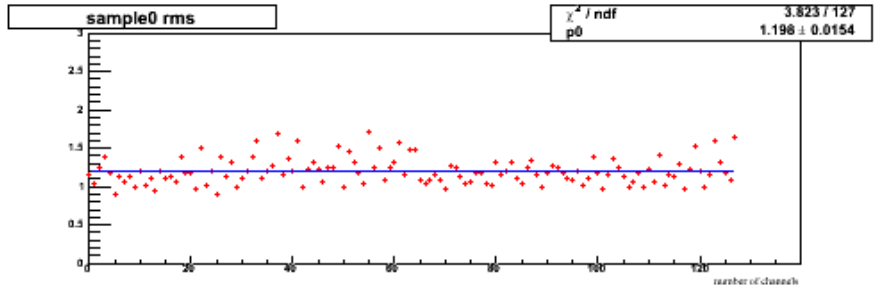


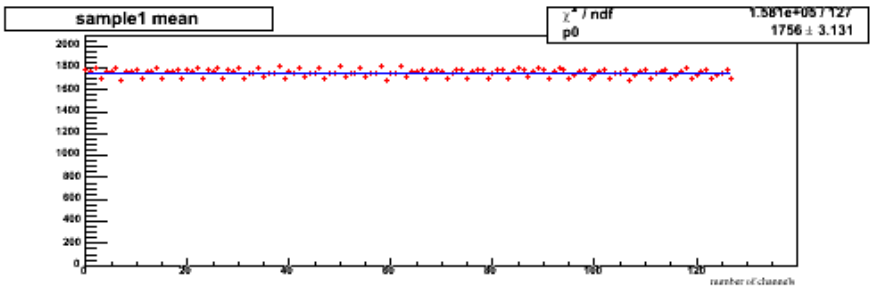


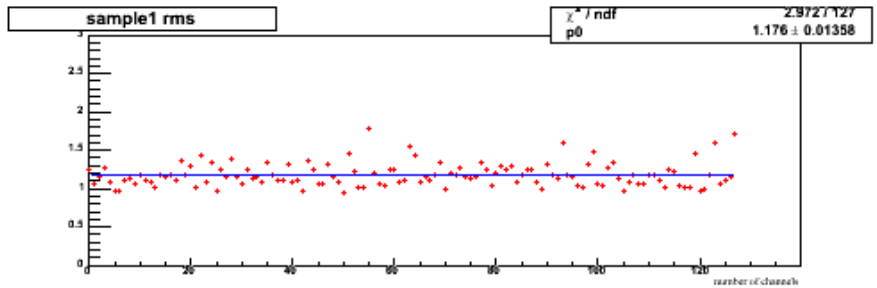


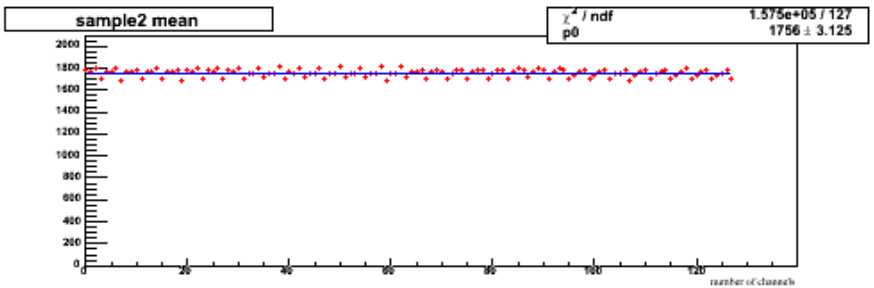
4 even buffering, at 10kHz.

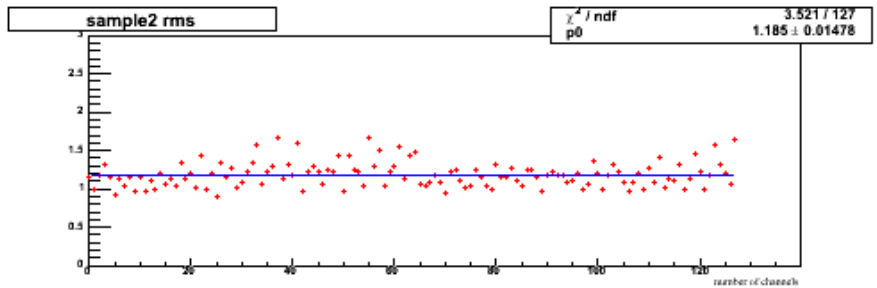


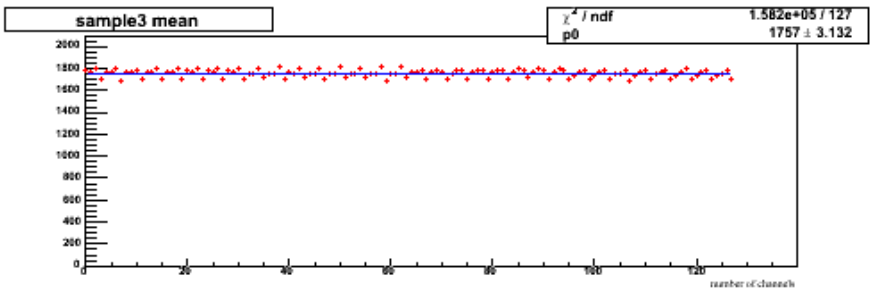


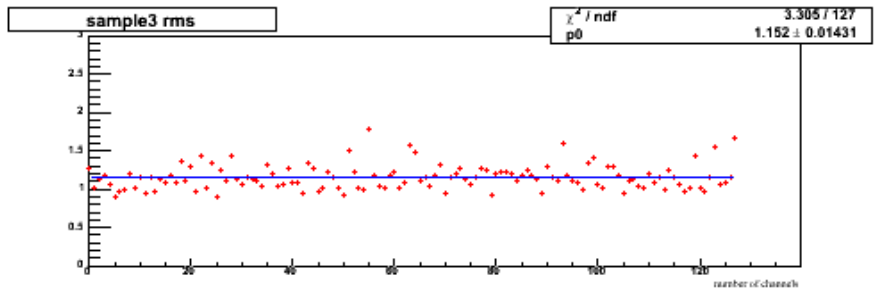






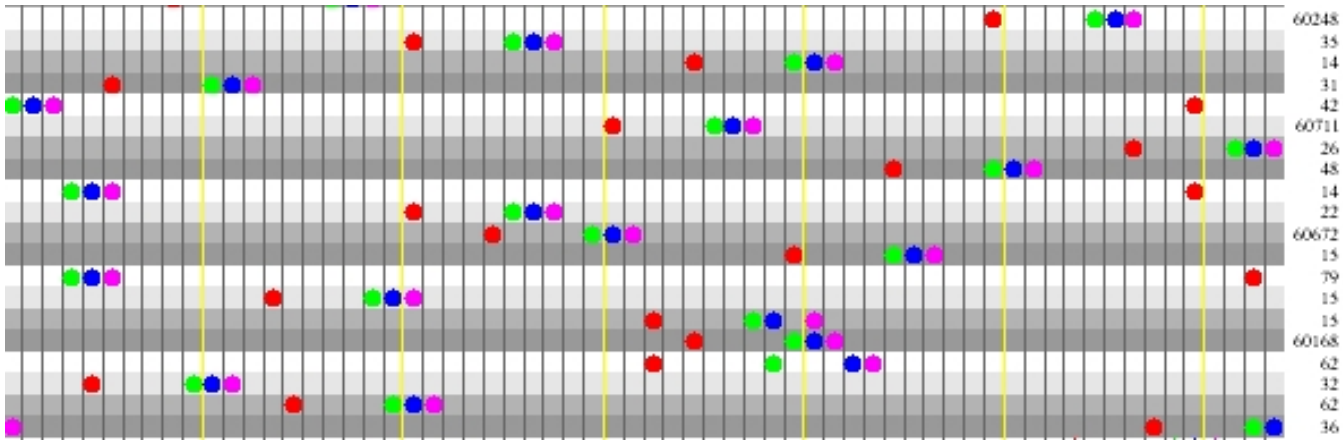




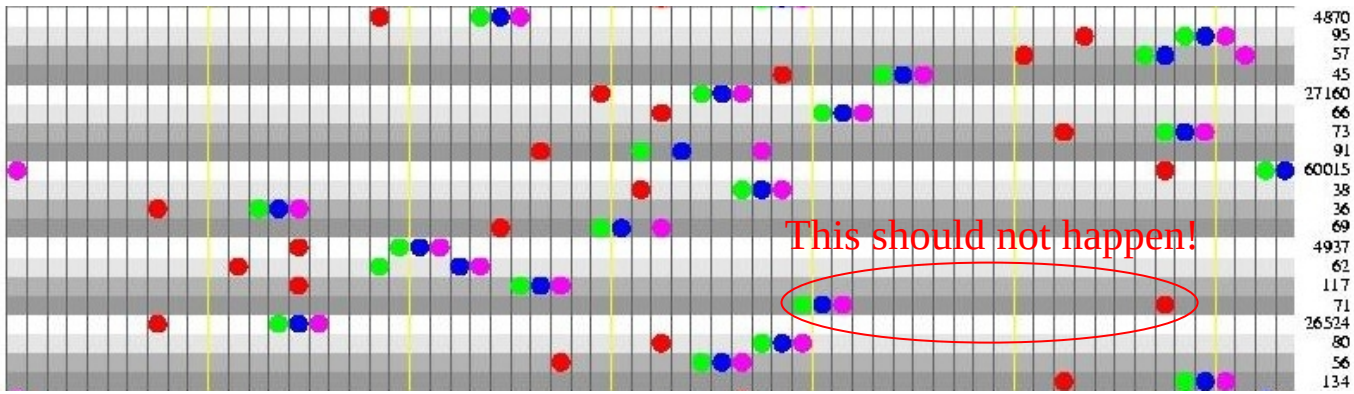


Online Monitoring.

AMU cell pattern can be “predicted” by looking at the time between events!!

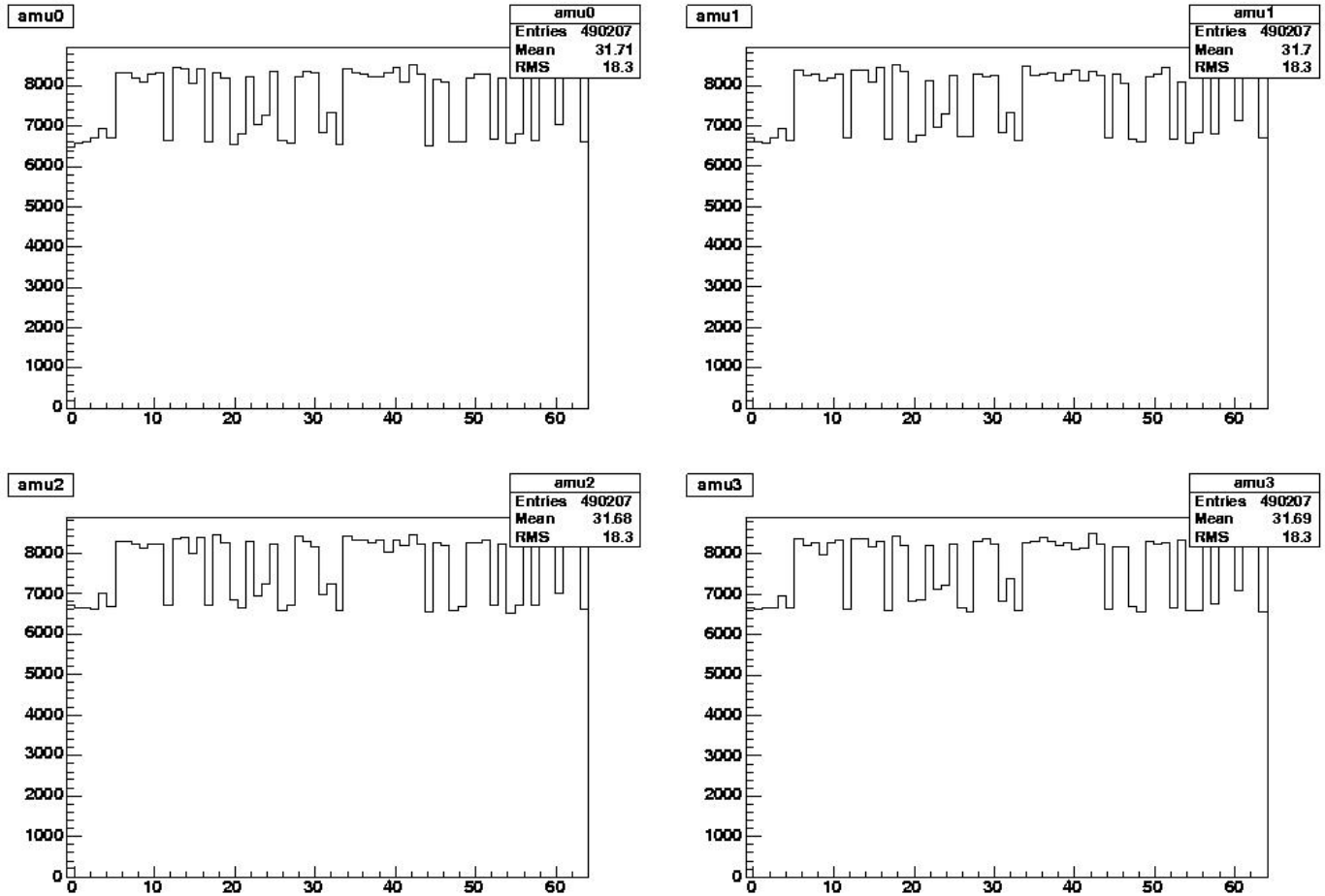


Caveat: The time taken by a cell to become available is not fixed!
Can vary between 110nS – 6.2uS (even though the conversion time is fixed).



Online Monitoring.

AMU cell distribution can be added for “experts”.



So, where we're now?

- FGPA ver139 worked perfectly on test bench (with 10MHz clock).
- Downloading FPGA through ARCnet was successful (Thanks to John H. and Olivier).
- BUT the code didn't work in the detector (with 9.4MHz clock).
- More "R&D", that's where we're now.