

1K serial EEPROM
Storage for FPGA setup values.
128 by 8 or 64 by 16 organization

Reference resistor on ORG pin
By 8 memory with resistor installed
By 16 memory with resistor not installed

De-caps for the FPGA

De-caps for buffer chips

All 74AHCT16245's are connected to +5V

mLAN

TFC_DATA(20:0)
TFC_CLK
TFC_PdN

DCM_DATA(20:0)
DCM_CLK
DCM_PdN

Calculated value of 1.6k. Use
2 1k's to reduce
parts counts.

Red LED

On when board is powered and FPGA not configured
Off when board is powered and FPGA configured
Flash when 4K beam clock present

Place LEDs near the
front edge of board

Green LED

Off when board is powered and FPGA not configured
On when board is powered and FPGA configured
Flash when DCM data is transmitted

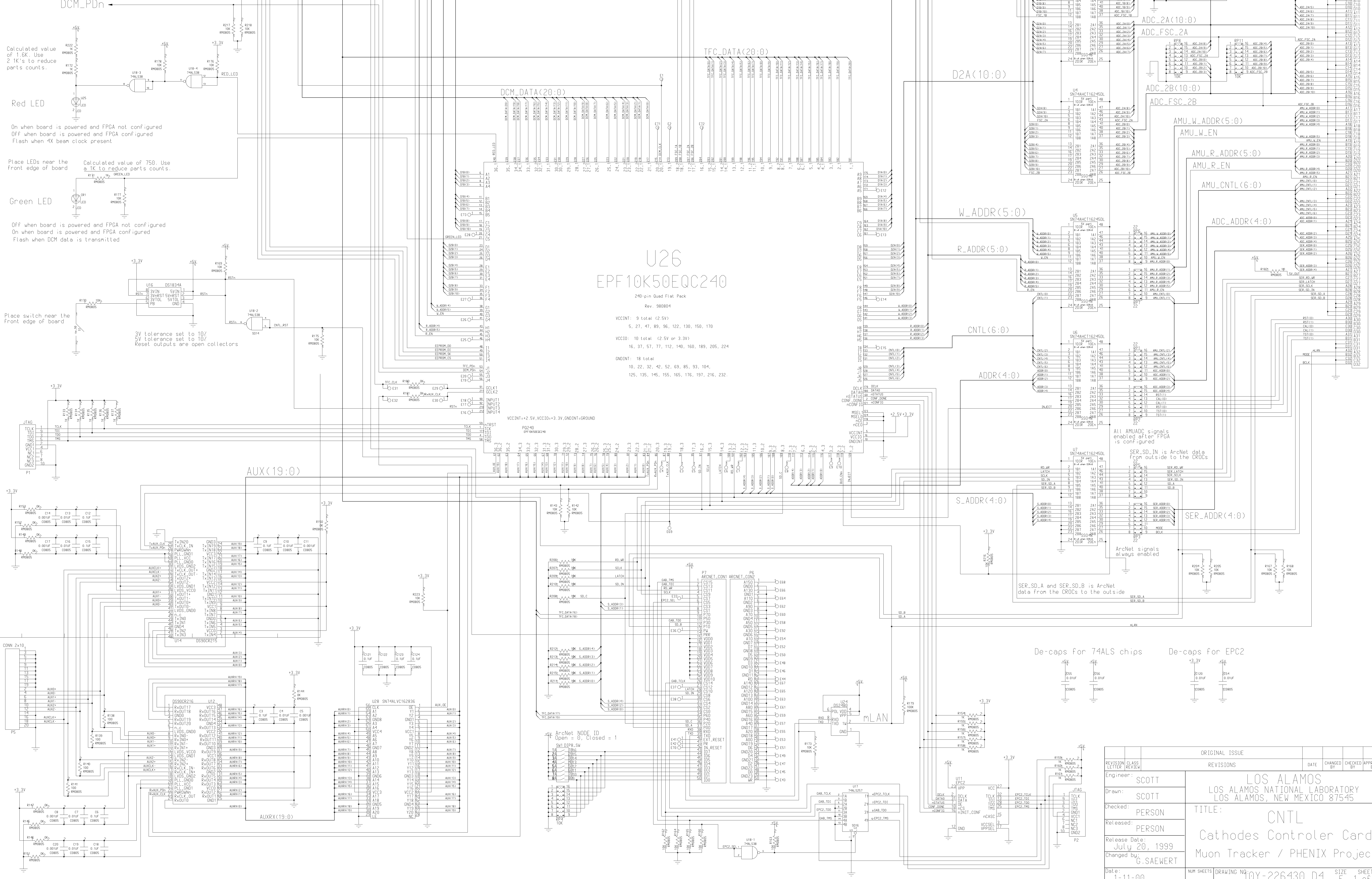
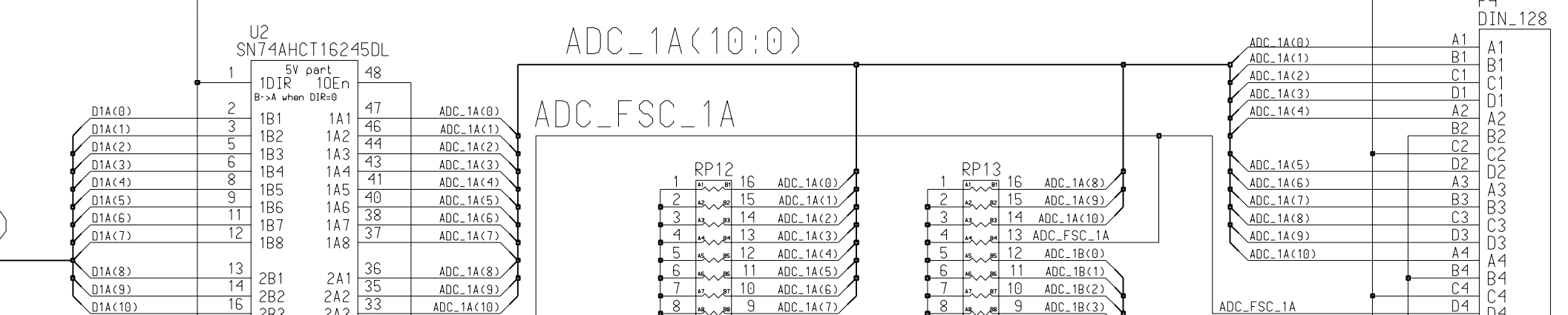
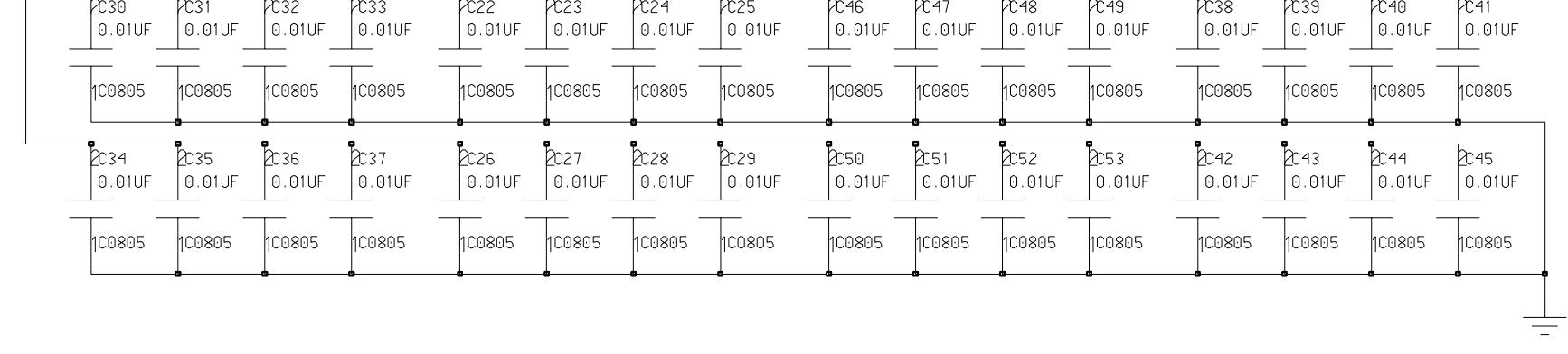
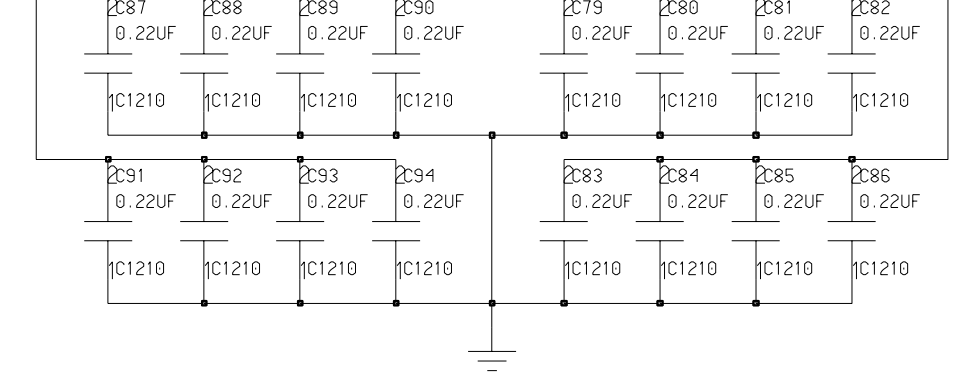
Place switch near the
front edge of board

JTAG

AUX(19:0)

CONN 2x10

AUXRX(19:0)



U26
EPF 10K50EQC240
240-pin Quad Flat Pack
Rev. 988904

VCCINT: 9 total (2.5V)
5, 27, 47, 89, 96, 122, 130, 150, 170

VCCIO: 10 total (2.5V or 3.3V)
16, 37, 57, 77, 112, 140, 160, 189, 205, 224

GNDFIN: 18 total
10, 22, 32, 42, 52, 69, 85, 93, 104,
125, 135, 145, 155, 165, 176, 197, 216, 232

All AMUADC signals
enabled after FPGA
is configured

SER_SD_IN is ArcNet data
from outside to the CROCs

ArcNet signals
always enabled

SER_SD_A and SER_SD_B is ArcNet
data from the CROCs to the outside

REVISION CLASS LETTER REVIEW	ORIGINAL ISSUE	REVISIONS	DATE	CHANGED BY	CHECKED APPROVED BY
Engineer:	SCOTT				
Drawn:	SCOTT				
Checked:	PERSON				
Released:	PERSON				
Release Date:	July 20, 1999				
Changed by:	G.SAEWERT				
Date:	1-11-00				

LOS ALAMOS
LOS ALAMOS NATIONAL LABORATORY
LOS ALAMOS, NEW MEXICO 87545

TITLE:
CNTL
Cathodes Controller Card
Muon Tracker / PHENIX Project

NUM SHEETS DRAWING 10Y-226430 D4 SIZE SHEET 1 OF 2