W+Si Forward Tracking Calorimeter for the ALICE upgrade

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For the ALICE FoCAL team

Outline

- *Introduction of the ALICE upgrade plans*
- *Physics Motivation of ALICE-FOCAL*
- *Location of FOCAL in the ALICE*
- *Key parameters*
- *Conceptual Detector Design*
- *Brief results of simulations*
- *Hardware readiness and beamtest in 2011*
- *Summary and Development ideas for the PHENIX cEMC*

ALICE upgrade plans

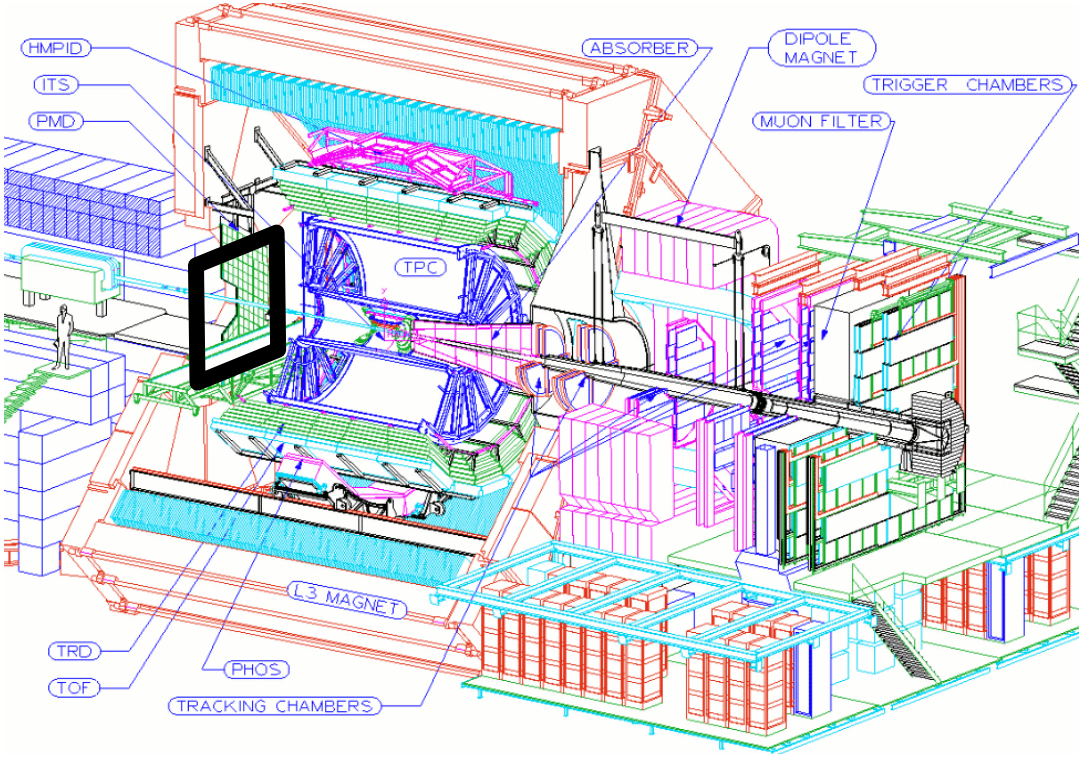
- *Detector upgrades for 10 years are being discussed.*
- *Current upgrade activities in the ALICE:*
  - *Completion of EMCal(2010), TRD(2011-2012), (and PHOS)*
  - *Di-jet Calorimeter (DCAL) (2011-2012)*
  - *TPC fast readout upgrade using new gas/electronics*
  - *Very high momentum particle identification (VHMPID)*
    - *Cherenkov radiator + photon detector using CsI+(RETTH)GEM/MWPC*
  - *2nd generation of vertex detectors (ITS)*
    - *Monolithic active pixel sensor (MAPS/MIMOSA/LePIX)*
  - *Forward Calorimeter (FOCAL)*
    - *W+Si tracking calorimeter covering forward rapidities*
  - *Backward Tracking vertex detectors in front of muon absorber*
  - *DAQ/HLT Upgrade (DDL-SIU interface, new IO bus, etc)*

Physics Motivation of ALICE-FOCAL

- *Main physics topics:*
  - *Gluon saturation (pA)*
    - *Fully exploit the opportunity at the LHC to access smaller-x region & large saturation scale by going to forward rapidity.*
    - *RHIC forward rapidity (η=3) ⇔ LHC mid-rapidity. Importance to understand initial state effects systematically at the LHC (pA).*
  - *Thermalization mechanism (saturation → glasma) (AA)*
  - *Systematic measurements of hot and dense medium (AA)*
    - *Elliptic flow/ridge/jet quenching (AA)*
- *Provide forward (η>3) coverage for identified particle measurements*
  - *EM calorimeters for (prompt) γ, π^0, η, heavy quark(onia), jets*
  - *Requires high granularity (lateral and longitudinal)*
- *Favored technology: W+Si calorimeter*

Location of FOCAL in ALICE

- *Detector Location*
  - *Stage 1 (z=3.5m, 2.5<η<4.5) in 2016*
  - *Stage 2 (downstream, 4.5<η<6) in 2020.*
    - *Need to modify the beam pipes and support stuffs.*

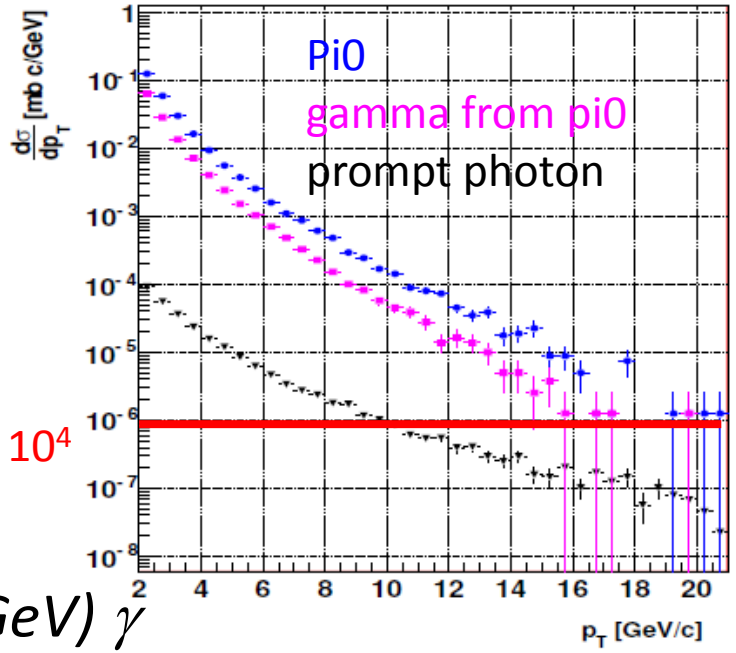


Project Institution

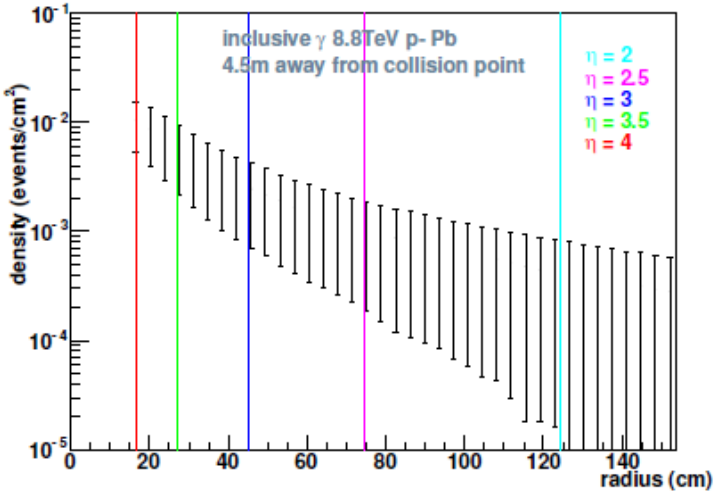
CNS Tokyo, Yonsei, Kolkata, Mumbai, Jammu, Utrecht/Amsterdam, Prague, Jyväskylä, Copenhagen, Bergen, Oak Ridge, Nantes, Jaipur

Key parameters

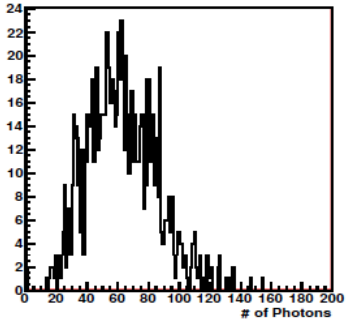
- *Dynamic range*
  - *Annual yield of π^0 (p+p)*
    - *pT<30-40GeV is the maximum reach in annual year. → 500 GeV in total E.*
- *Particle density*
  - *$N_\gamma \sim N_{ch} \sim 0.03$ /cm^2 (η=4) in p+A*
  - *N_γ is dominated (95%) by low pT(<1GeV) γ*

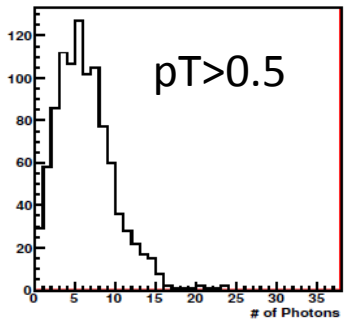


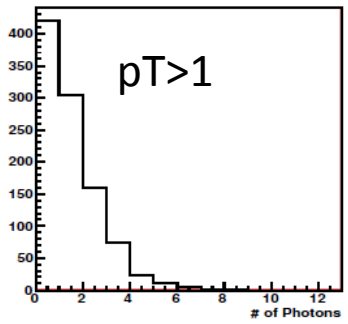
Particle density (HIJING p+A)



of γ in FoCAL in central p+Pb (Pb going direction)



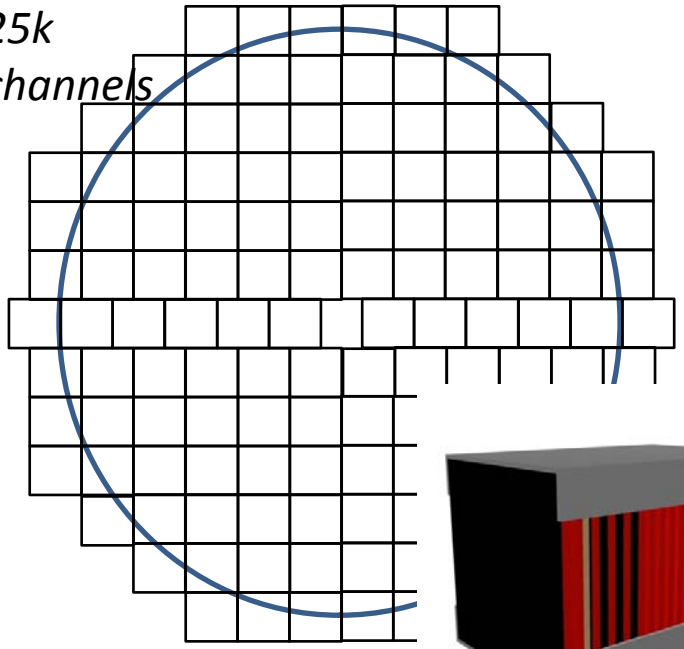


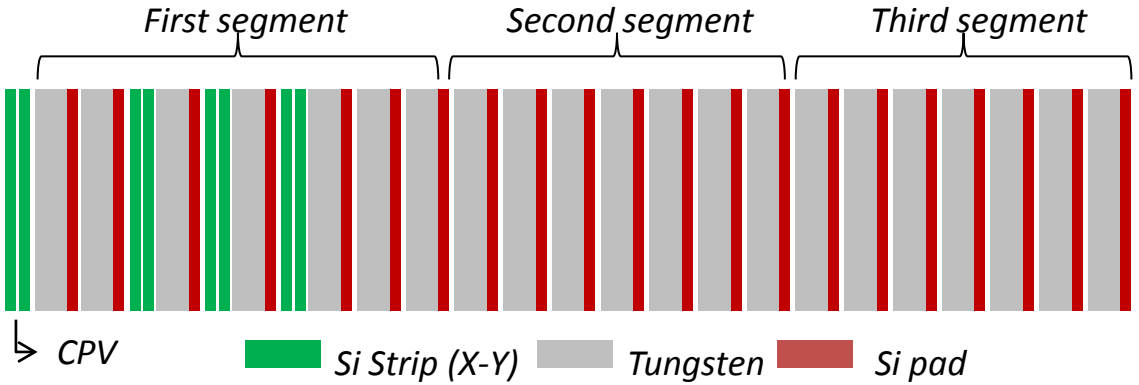


Conceptual Detector Design-I

- *"Standard" W+Si (pad/strip) calorimeter (CNS)*
  - *Similar to the PHENIX FOCAL but 3.5m away from IP*

Total 25k channels

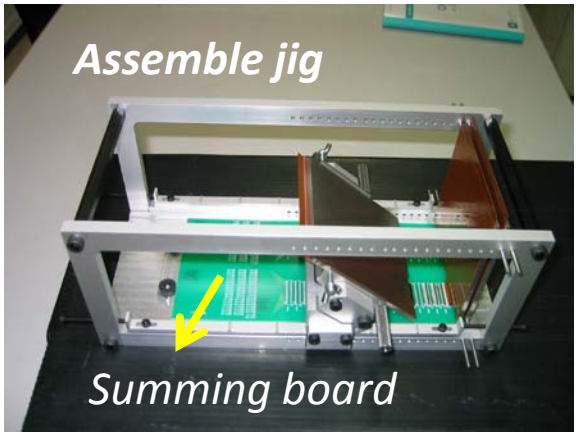




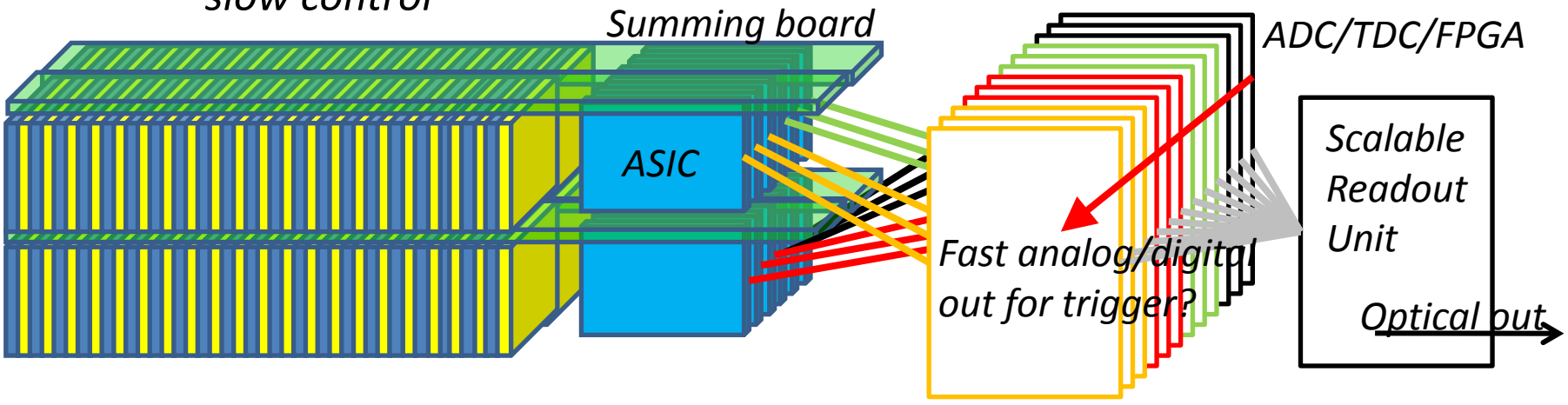
- *W thickness: 3.5 mm ($1X_0$)*
- ***wafer size: 9.3cmx9.3cmx0.525mm***
- ***Si pad size: 1.1x1.1cm² (64 ch/wafer)***
- *W+Si pad : 21 layers*
  - *3 longitudinal segments*
  - *Summing up raw signal longitudinally in segments*

- *Single sided Si-Strip ($2X_0$-$6X_0$)*
  - *2γ separation, 6 inch wafer*
  - *0.7mm pitch (128ch/wafer)*

Readout Flow

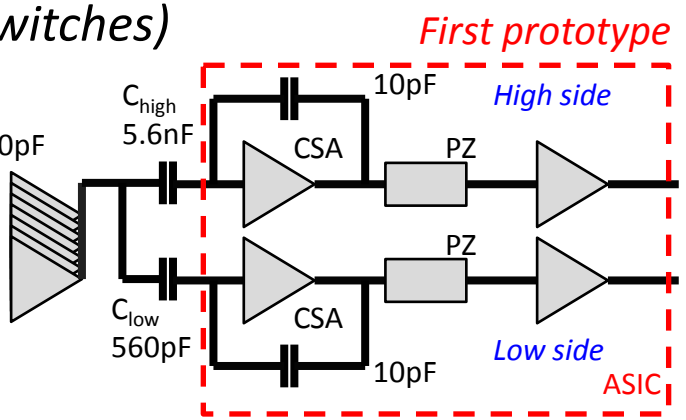


- *Composition*
  - *Summing board: (1.5mm thickness)*
    - *sum up signals in segments longitudinally, biases*
  - *ASIC cards :*
    - *Preamplifer + shaper (analog out) or preamplifer with QTC (digital out)*
  - *ADC(12-14bit)/TDC(TMC)+FPGA board:*
    - *Digitizer, ZS, feature extraction, formatting, trigger handling, buffering*
  - *SRU (scalable readout unit):*
    - *Developed by RD51. Trigger handling, data format & transfer, master of slow control*



ASIC development

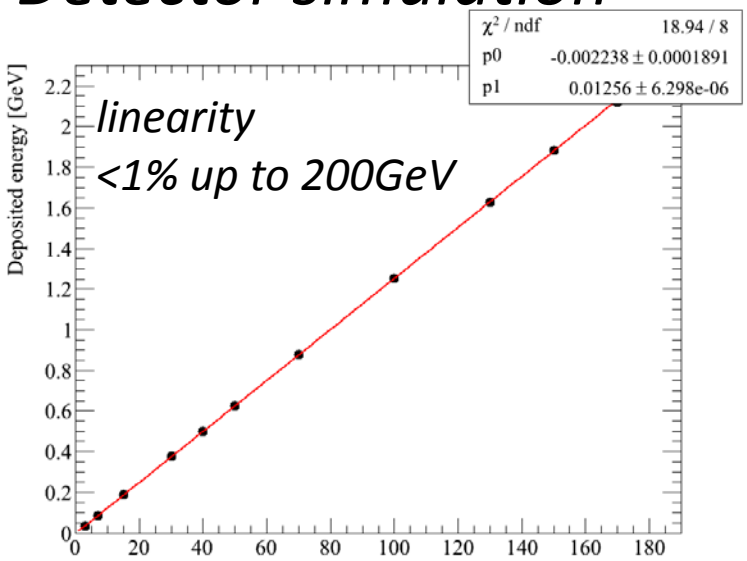
- *Pads readout :*
  - *Dynamic range: 50fc – 200pC . Cross talk < 1%. S/N=10@MIP*
  - *Relatively fast readout is needed for L0 trigger generation.*
  - *R&D of the ASIC is being done by CNS+RIKEN/KEK and ORNL*
    - *Dual charge sensitive preamplifier using capacitive division*
    - *QTC (charge-to-time converter, no CMOS switches)*
    - *Dual transimpedance preamplifier*
    - *(details are in backup 23-31 and Chuck's slides.)*

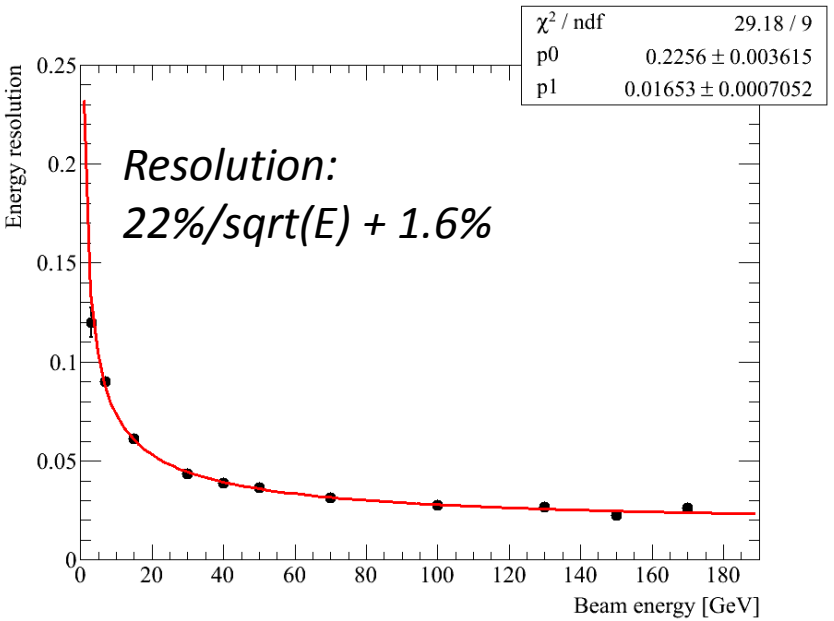


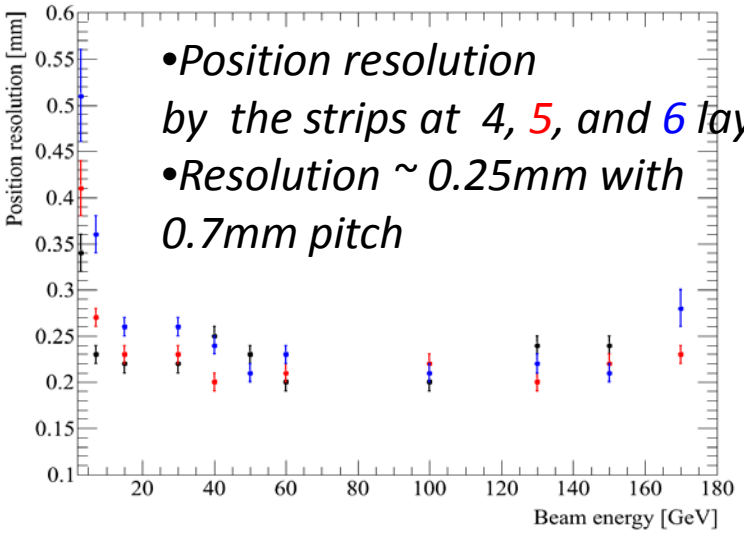
- *Strip readout:*
  - *Dynamic range: 4fc – 2pC.*
  - *PACE-III (CMS preshower counter, LHCf W+Si readout)*
    - *Discussion to use PACE-III has been started with CMS.*

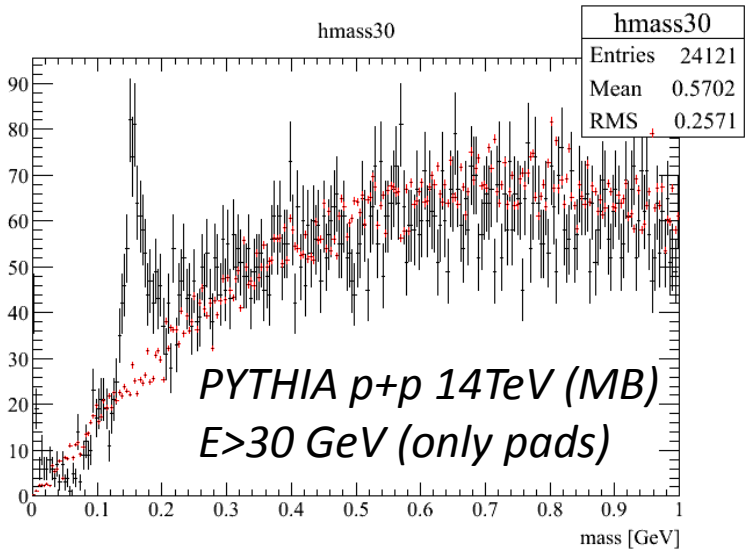
Detector Performance (Simulation)

- *Detector simulation*





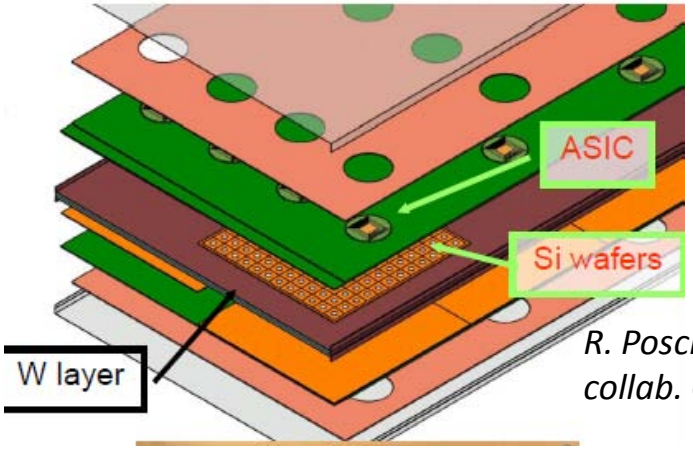




Another choice of Readout

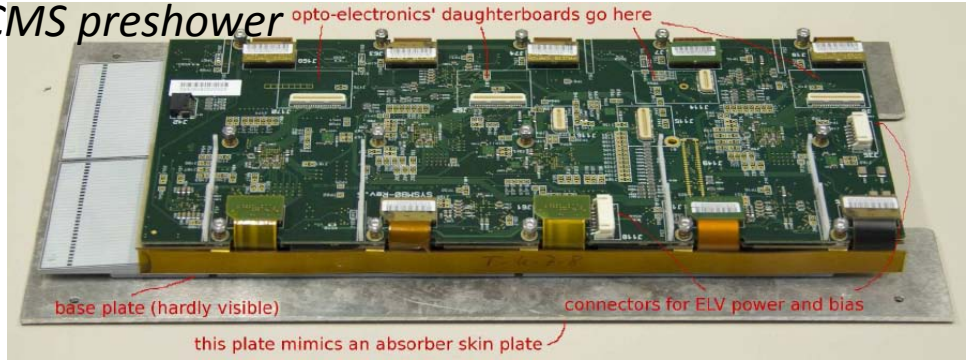
- *Readout individual layers. Amplification, shaping, digitization, serialization are done behind the wafer.*
  - *Lower noise compared to raw signal driving on summing board and smaller dead space between towers.*

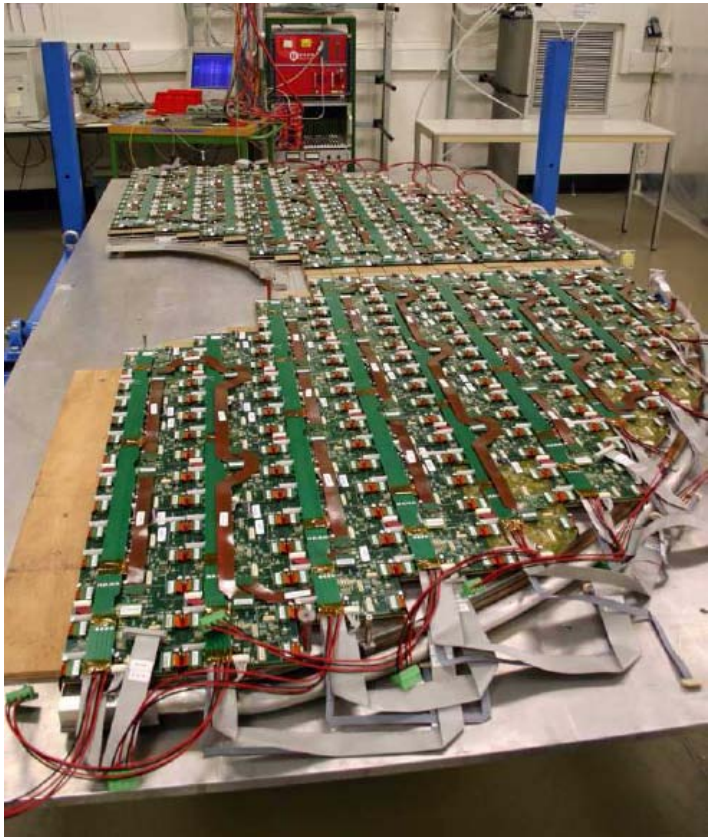
CMS preshower



R. Poschl for the CALICE collab. Calor2010 conf.

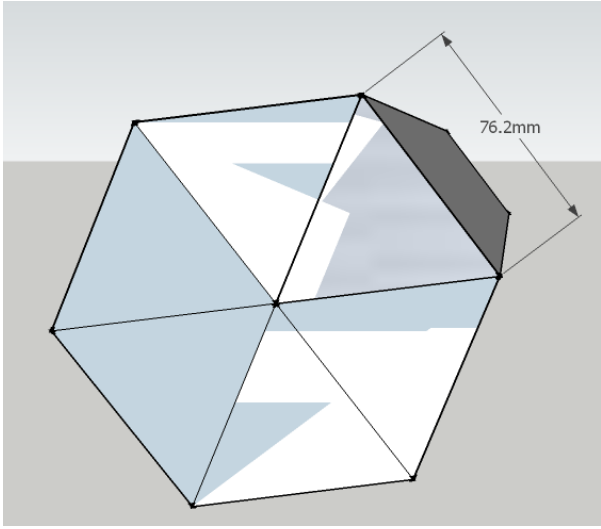
CMS preshower



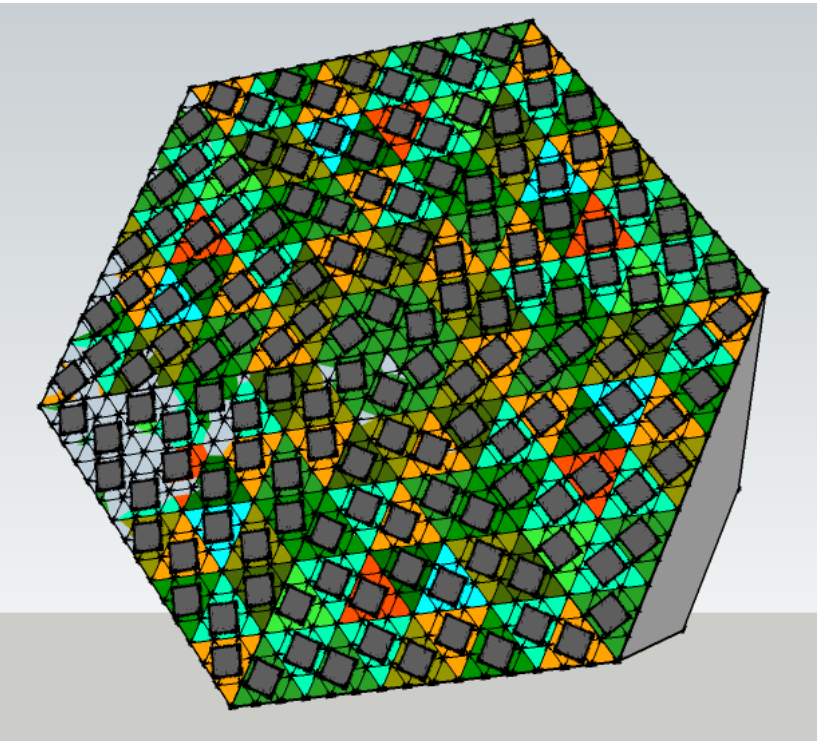


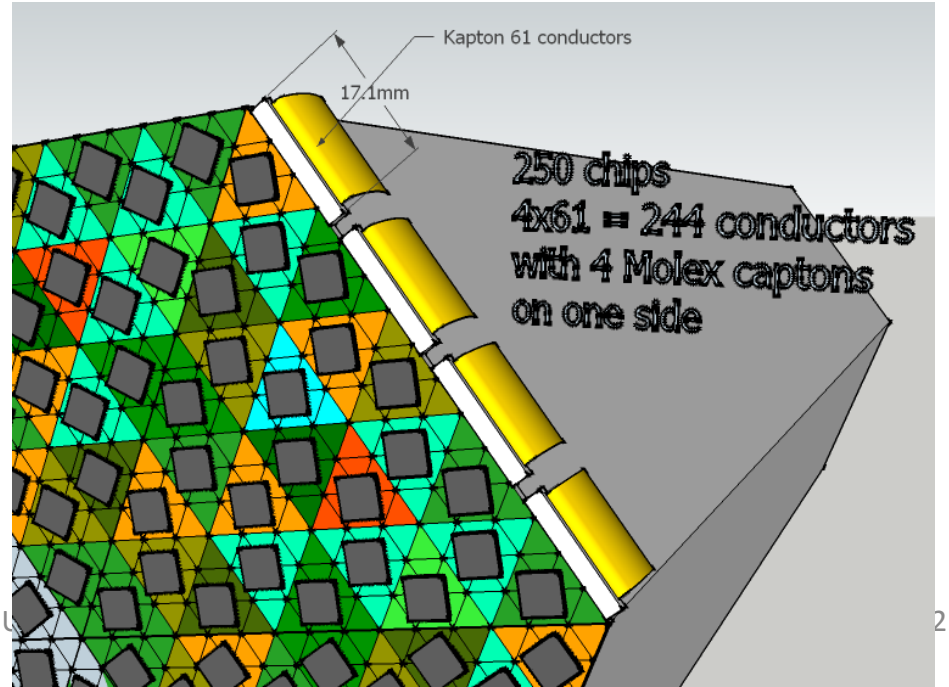
Another geometrical Idea

- *hexagonal towers*
  - *fit nicely in circles around beam-pipe*
  - *uses more silicon surface of cylindrical ingot*
- *triangular pads*



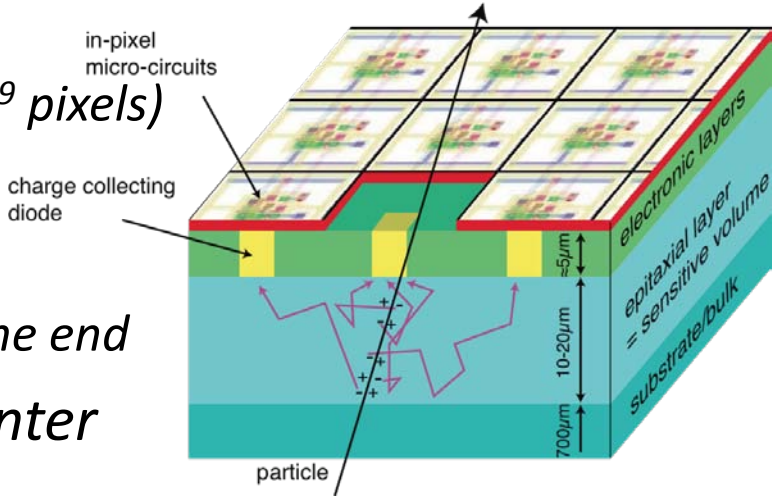
Terry Awes
Hans Muller

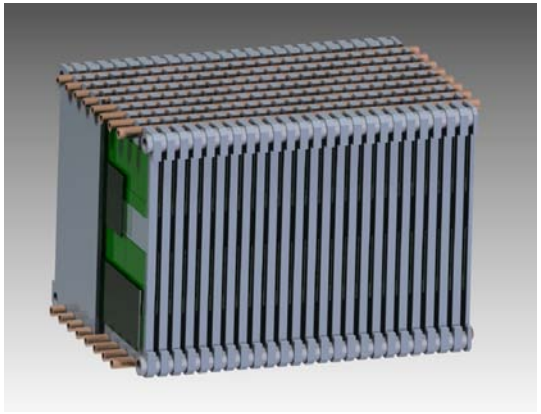


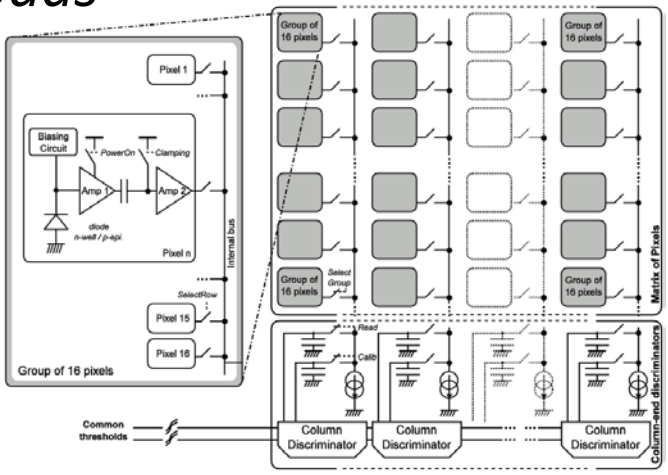


Conceptual Detector Design-II

- *W absorber + Monolithic pixel sensor*
  - *MIMOSA chips (digital readout) are promising to use.*
  - *Development has been started.*
    - *20um pixel size → 100 um pixel size (10^9 pixels)*
    - *suppress data volume, reduce RO time*
    - *avoid saturation ….*
    - *GBT/GBR being developed by CERN in the end*
  - *Personal interests as preshower counter and hybrid with pads*



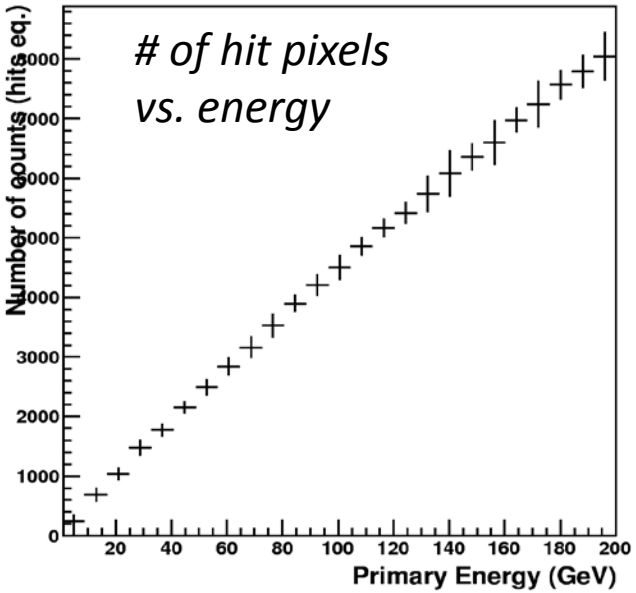


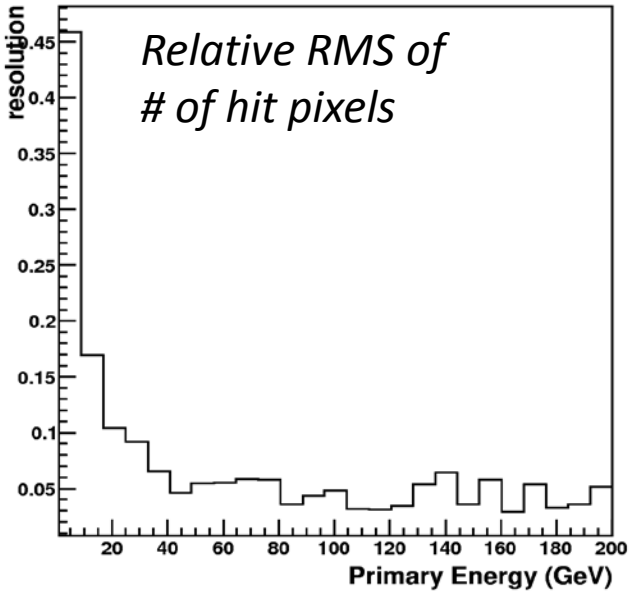


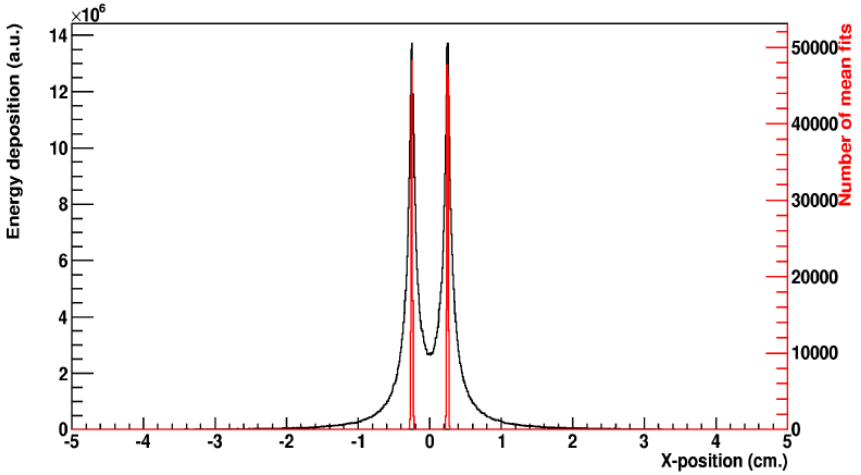
- *CMOS wafer including thin sensitive volume and electronic layers*
- *charge from traversing particles collected at diodes*

Detector Performance (Simulation)

- *Detector simulation for pixels*





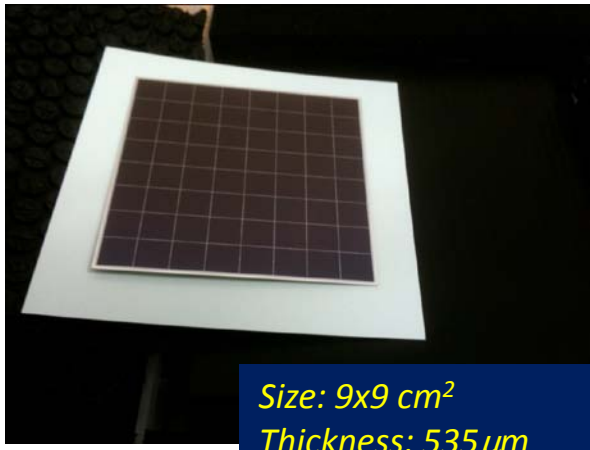


←*Energy projection from all layers in case that two gammas are injected with 5mm separation.*

- *good separation capability*
- *this is conformed up to 2.5mm at least. Still under studying.*

Hardware readiness and beamtest

- *Hardware readiness*
  - *Alloy (94W-4Ni-2Cu) for one tower (Japan Tungsten Co. Ltd)*
  - *Si pad and Si strip for one tower (Hamamatsu Co. Ltd)*
  - *Jig for assembling layers*
- *Beamtest in 2011 at PS/SPS@CERN*
  - *Currently, LHC will shutdown in 2012.*
    - *PS/SPS will not be available in 2012.*
    - *FOCAL beamtest is planned in 2011.*
  - *One tower of W+Si pad/Si strip configuration.*
    - *Performance test (linearity, resolution)*
  - *Partial of W+MIMOSA pixel configuration*
    - *Proof of principle.*



Size: 9x9 cm²
Thickness: 535μm
Pad size: 1.1x1.1 cm²
Number of pads : 64

Summary and Development ideas for the PHENIX cEMC

- *There are a lot of activity, design considerations, options, and ideas for the ALICE FOCAL.*
  - *Still needs to be developed in hardware and lots of quantitative studies by simulations are needed.*
  - *There might be overlap efforts for the ALICE FOCAL and PHENIX cEMC.*
- *We (CNS, ORNL) hope for some collaboration between ALICE FOCAL and PHENIX cEMC.*
- *Chuck will discuss this more just after this talk.*

Thank you for your attention.

Backup slides

"Possible" HI Plan at LHC

Studying QGP Era (MB)

2010 (official) - $\sqrt{s_{NN}}$ = 2.76 TeV Pb + Pb (4 weeks) L~10^{25} $cm^{-2}s^{-1}$

2011 (anticipated)-$\sqrt{s_{NN}}$ = 2.76 TeV Pb + Pb (4 weeks) L ~ few 10^{26} $cm^{-2}s^{-1}$

2012 (official) – Shutdown for maintenance, installation & repair

2013 - $\sqrt{s_{NN}}$ = 5.5 TeV Pb + Pb, L~10^{27} $cm^{-2}s^{-1}$

2014 - $\sqrt{s_{NN}}$ = 5.5 TeV Pb + Pb, L~10^{27} $cm^{-2}s^{-1}$

Control experiments

2015 – $\sqrt{s_{NN}}$ = 8.8 TeV p + Pb & Pb + p or lighter A + A

2016 – Shutdown – LINAC4 /Collimation/RF & detector upgrade

2017 – $\sqrt{s_{NN}}$ = 5.5 TeV lighter A + A or $\sqrt{s_{NN}}$ = 8.8TeV p+Pb/Pb+p

Detail Studying Era (rare probes)

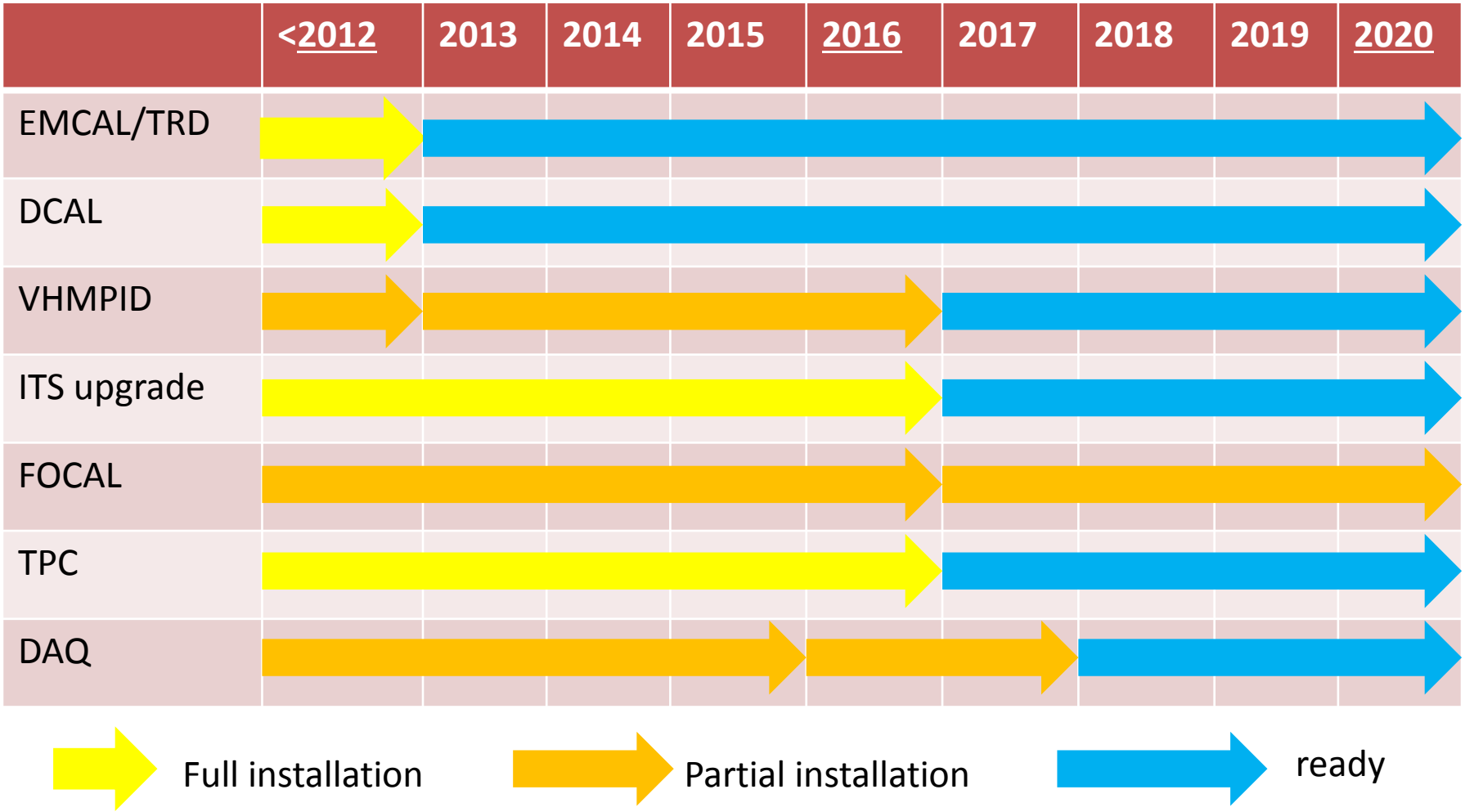
2018 – $\sqrt{s_{NN}}$ = 5.5 TeV high L Pb + Pb for hard probe physics

2019 – $\sqrt{s_{NN}}$ = 5.5 TeV high L Pb + Pb for hard probe physics

2020 – Shutdown – …. upgrades

Timeline for the Upgrade

- *Timeline for the upgrades*
  - *(of course, the schedule could be changed…)*

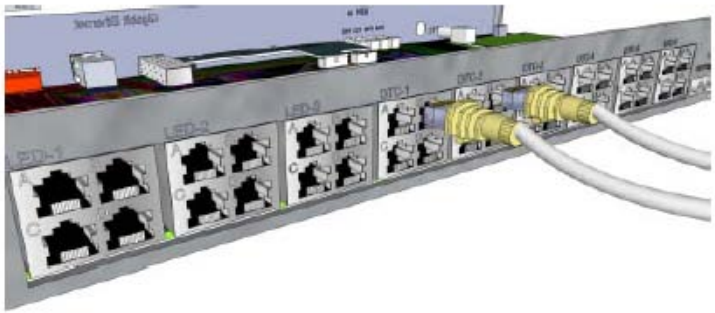


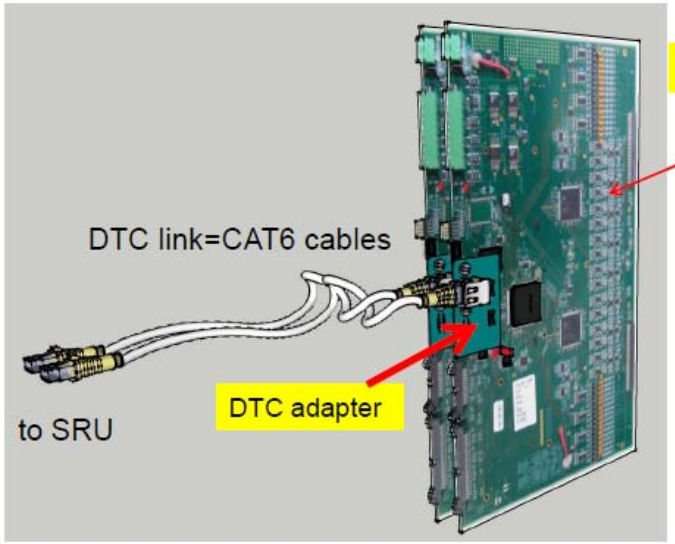
ADC/TDC & FPGA board

- *At least, 10 bit is not enough. More than 12 bit.*
  - *Commercial FADC (TI, AD,,,) with multi-channel/chip, 10-50MSPS, low power consumption*
  - *Roughly speaking, data size in p+A could be:*
    - *0.3(occupancy) x 256 (tower) x 64 x 3 (ch/tower) x 2 (H/L) x 12 (bit) x 20 (# of samples) = 0.9MB/event*
      - *Reference: dN/dy=700, 15MB/evt (TPC), 1.1MB/evt (TRD)*
    - *Need to extrapolate to A+A*
  - *FPGA (Xilinx Virtex series) for zero suppression, feature extraction (online pulse shape analysis, summation), event building, formatting, trigger input handing, output buffering (and send to SUR)*
  - *Similar to TRU in PHOS/EMCAL.*

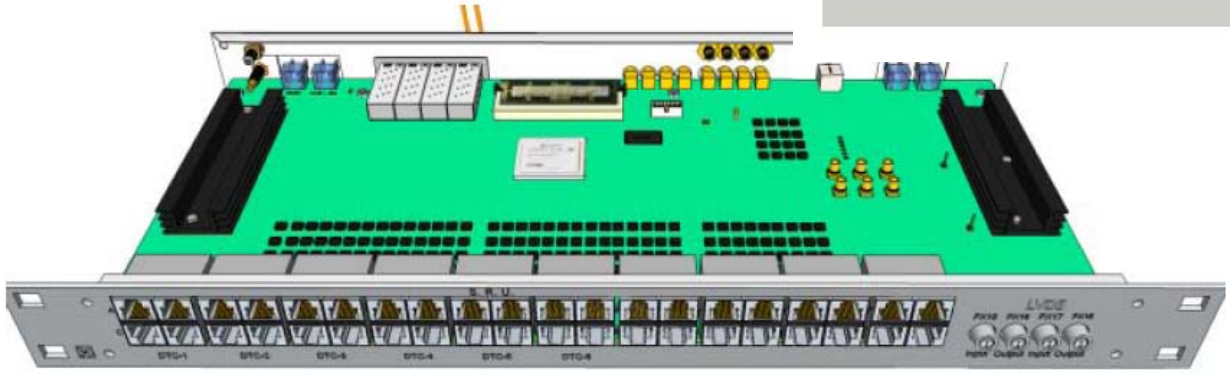
FEE & SRU

- *Use SRU as EMCAL/DCAL/(TPC) will do.*
  - *– developed by RD51+ALICE project*





Scalable readout Unit (SRU)



TTCrx interface for trigger handling
10 GBE, SPF, optical fiber
Master for the slow control of FEEcards

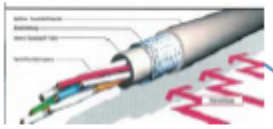
Scheme: FEE and SRU

DTC link protocol

proposed by Fan Zhang , CCNU Wuhan

Coded trigger and Control for dynamic actions.
with 80 MHz clock: Input stream from 40 FEC's @ 80 Mbit/s ~ 3.2 Gbit/s to DATE

CAT6 cable



4 x twisted pairs
CAT6 shielded cable

Clock ← DTC_CLK clock to FEC pin 1-2
Data → DTC_DATA data from FEC pin 4-5
Select ← DTC_TRIG coded trigger to FEC pin 3-6
Return → DTC_RETURN status or local trigger pin 7-8

buffered , terminated LVDS signalling over 15-25 m CAT6

40 x ....

FEE
FEE
FEE
RJ45
Plug in DTC mezzanine
Old Altera FPGA

RJ45
SRU
Virtex-6 FPGA
3.2 Gbps to DATE

- DTC_DATA = Serial data or ACK to SRU
- DTC_TRIG = Serial data or ACK to FEE
- DTC_RETURN = Coded status to SRU (Ready or Error ~)
- Note: for disabling a FEE card , SRU stops CLK for its link

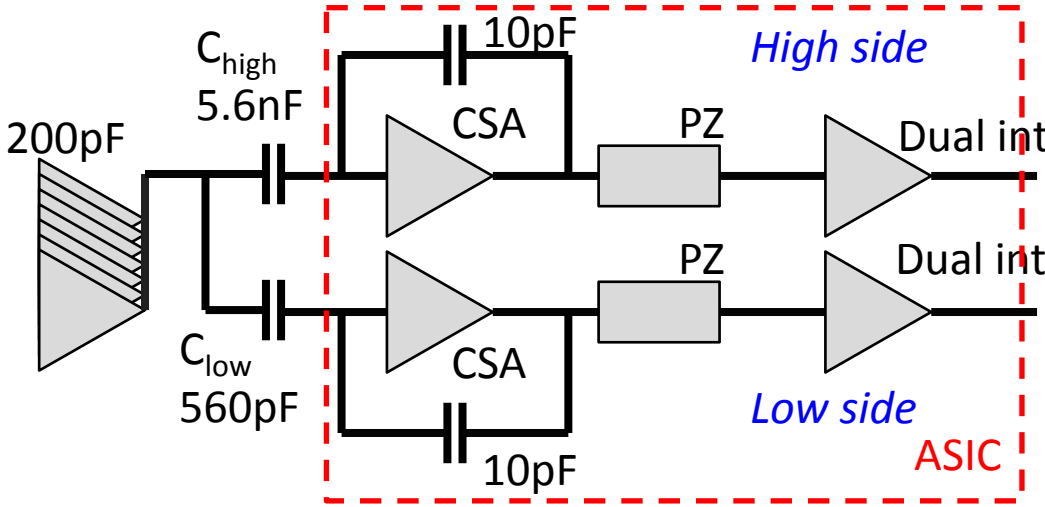
- Mode detection : detect DTC_TRIG pulse
- If (Widths of DTC_TRIG pulse, number of T_{DTC_CLK})
  - 2 : Level-0 trigger
  - 4 : Level-1 trigger
  - 6 : Level-2 trigger = Readout command
  - 8 : Control operation
  - >=9 : Error

Preamplifier

- *Three different types of readout amplifier:*
  - *Charge sensitive amplifier (CSA)*
    - *Pad output current is integrated on the feedback capacitor in CSA. Best in terms of noise…*
  - *Voltage amplifier*
    - *Pad output signal is integrated on the pad capacitance (Cd) and the voltage across the capacitor is amplified. Uniformity of Cd is necessary.*
  - *Current amplifier*
    - *Pad output signal is directly amplified and transformed into a voltage signal. Low input impedance and this limits the use in systems with large capacitive loads…*

Dual charge sensitive preamplifier

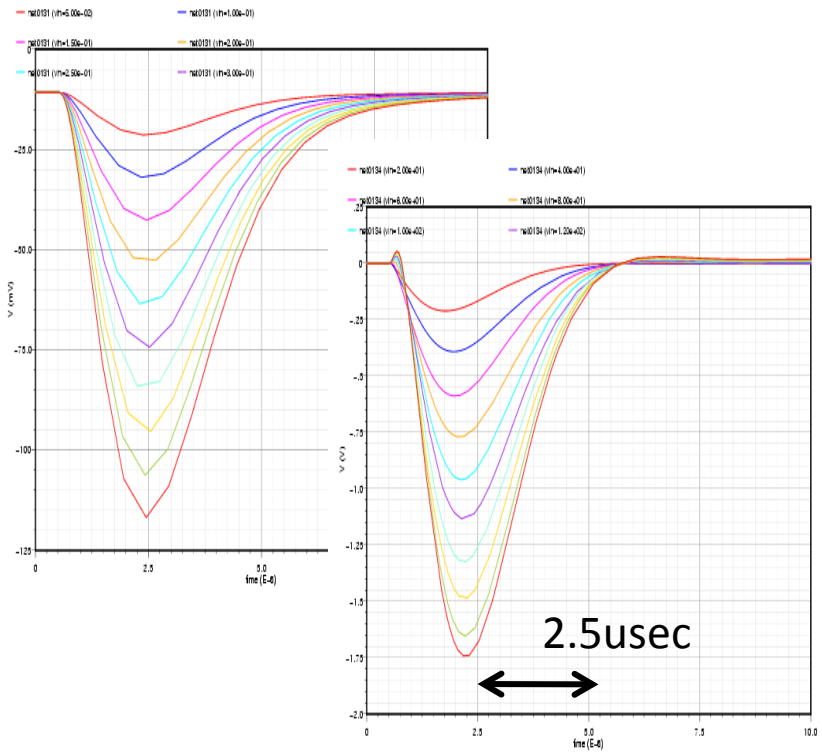
- *Due to the limited output swing of ASIC (5V, 3.3V, 2.5V depending on process), dual input preamplifier with dual gain is designed.*
- *Requirements:*
  - *Open loop gain is sufficiently larger compared to the capacitance ($Z = 1/\omega C + r/A$, $1/\omega C >> r/A$)*
  - *Input impedance (Z) is sufficiently smaller compared to Cd*

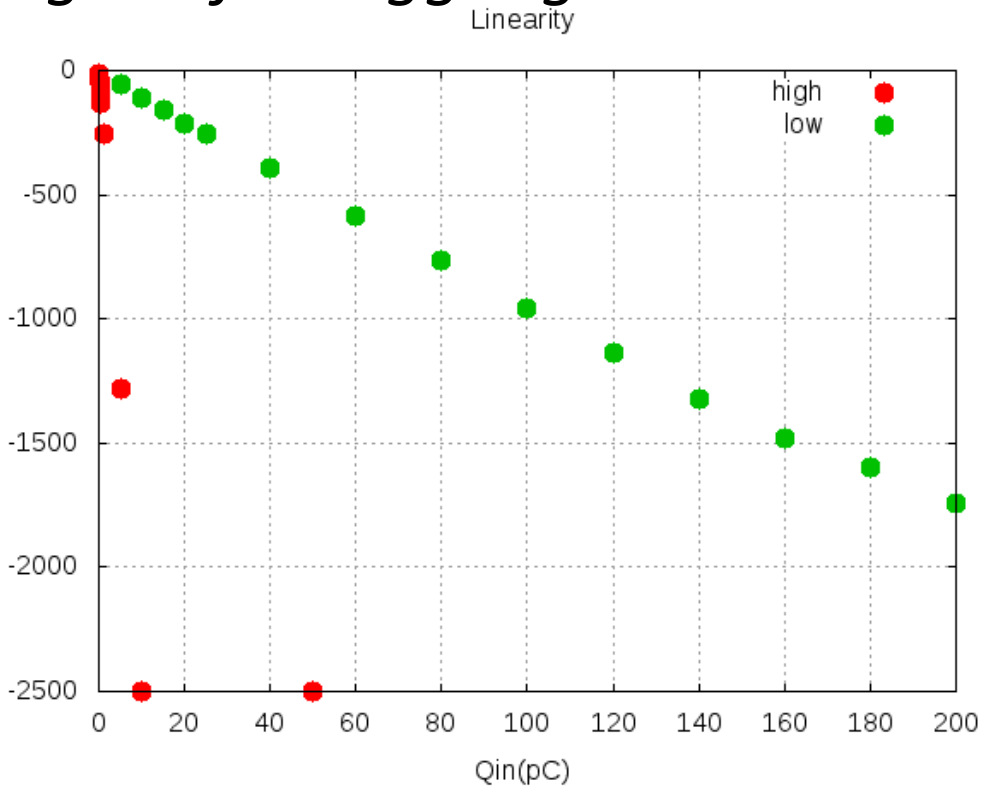


CSA in high gain side has additional saturation avoidance circuit to keep the constant input impedance of high side.

Overall linearity

- *Overall linearity at the end of dual integrator*
  - *Peaking time: τ_{peak} ~ 2usec*
  - *Good linearity up to 200pC*
- *2usec peaking time is not good for trigger generation*



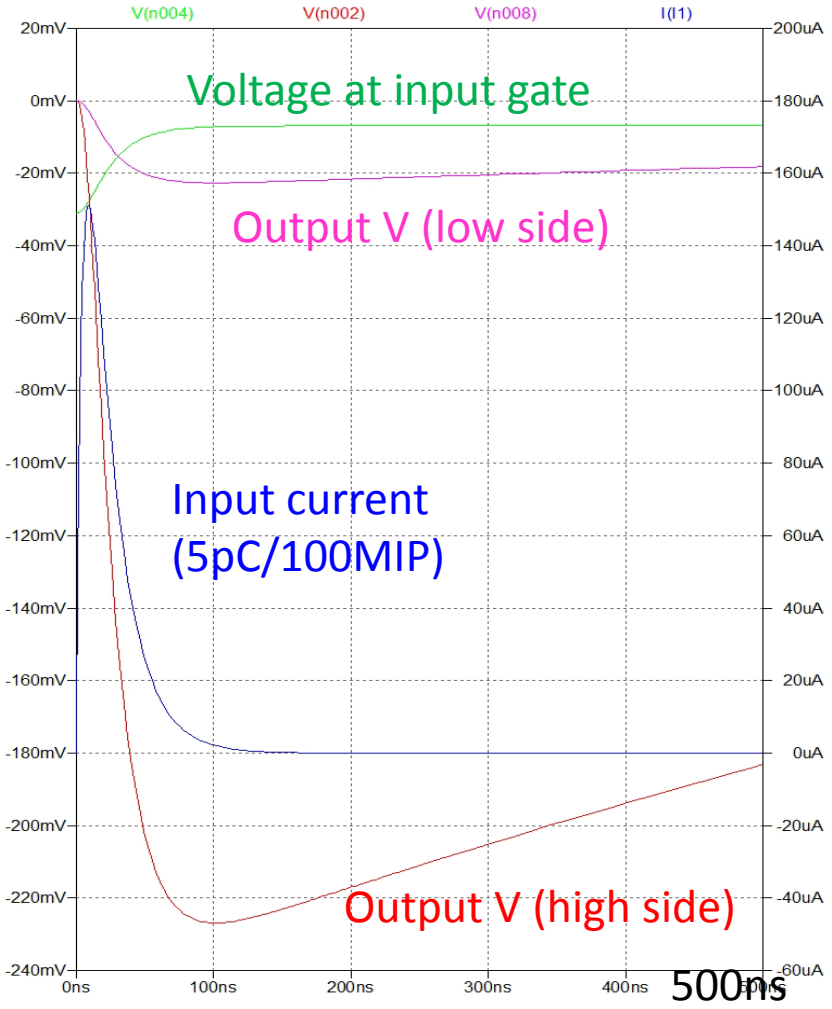


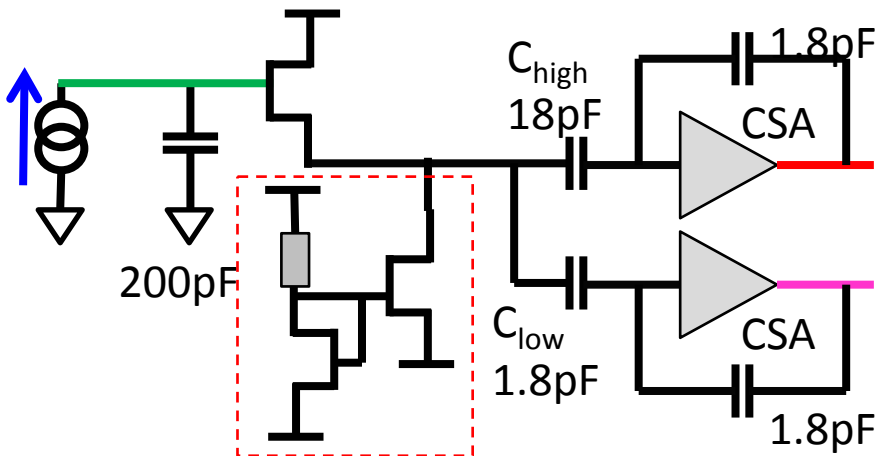
Next plans including trigger capability

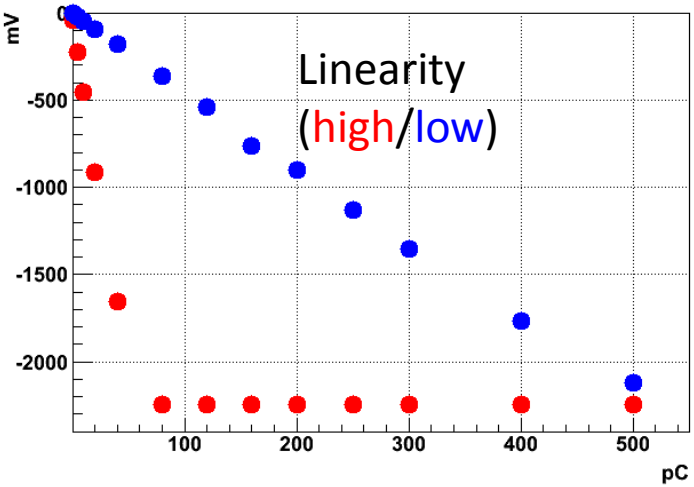
- *Revisit our charge sensitive preamplifier*
  - *To enlarge bandwidth, phase margin, open (closed) loop gain*
- *Another type of QTC without CMOS switches and shaper*
  - *Design is underway.*
- *Another type of preamplifier*
  - *Voltage amplifier proposed by Chuck (ORNL)*
    - *Pad output signal is integrated on the pad capacitance (Cd) and the voltage across the capacitor is amplified.*
    - *Source follower at the 1st stage*
      - *See Chuck and David's slides shown in last week.*
  - *Current amplifier*
    - *Pad output signal is directly amplified and transformed into a voltage signal. Low input impedance and this limits the use in systems with large capacitive loads…*

Voltage amplifier

- *Shown by Chuck & David (ORNL) last week*
  - *Quick simulation using LTSPICE (by Taku)*

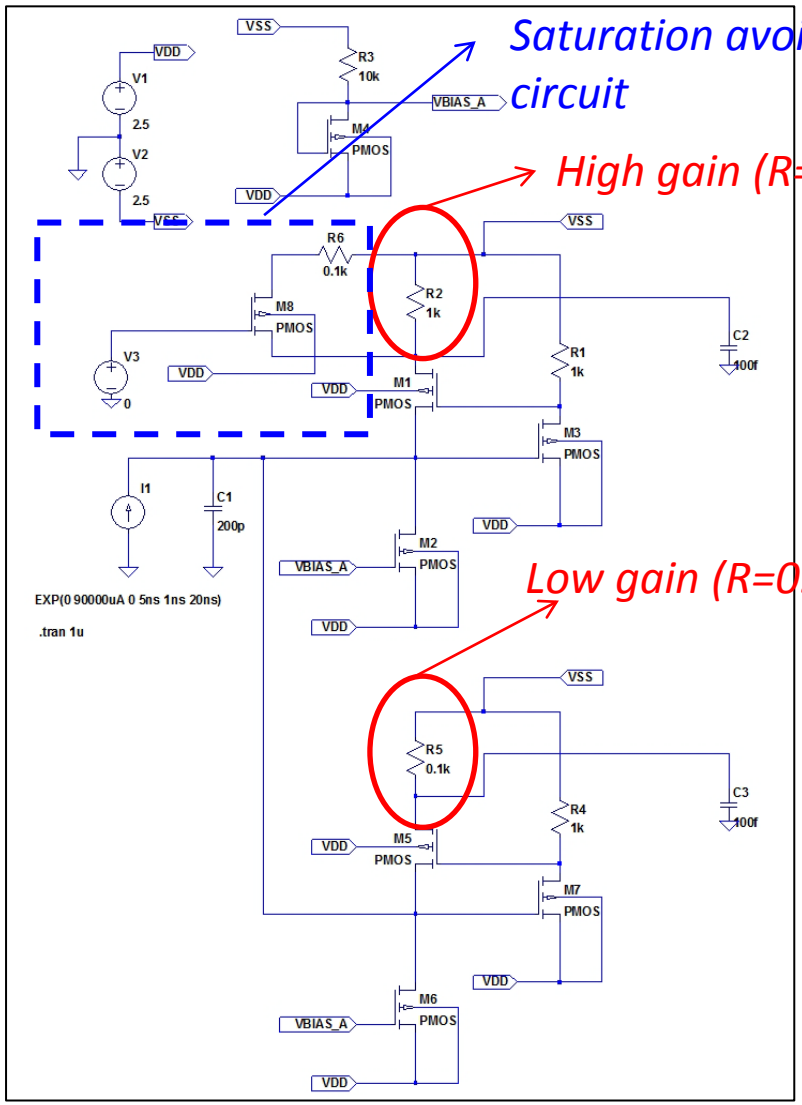


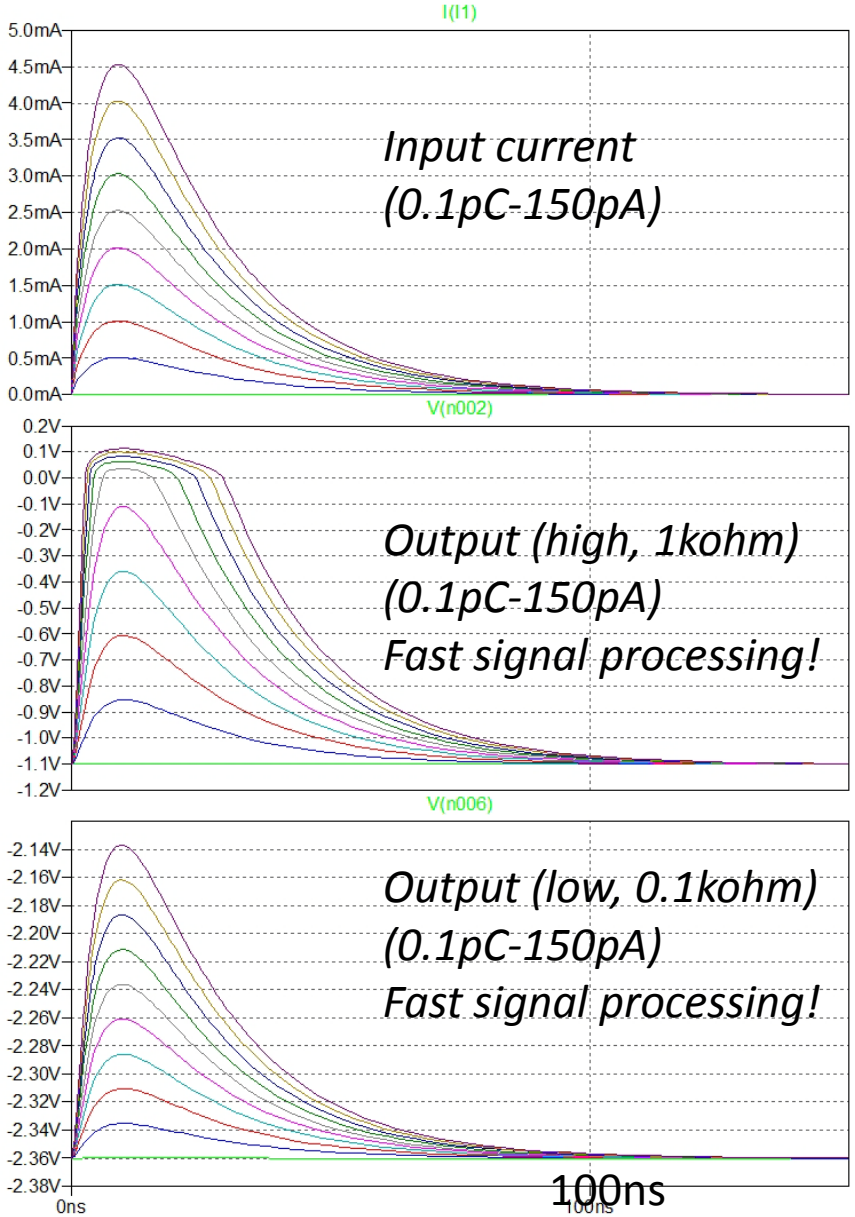




Current preamplifier

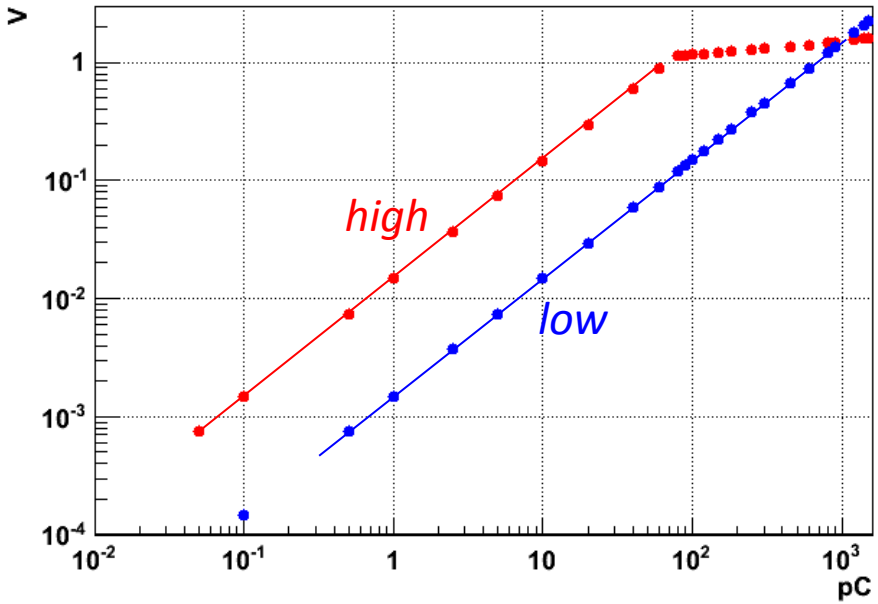
- *LTSPICE simulation (Taku)*





Linearity

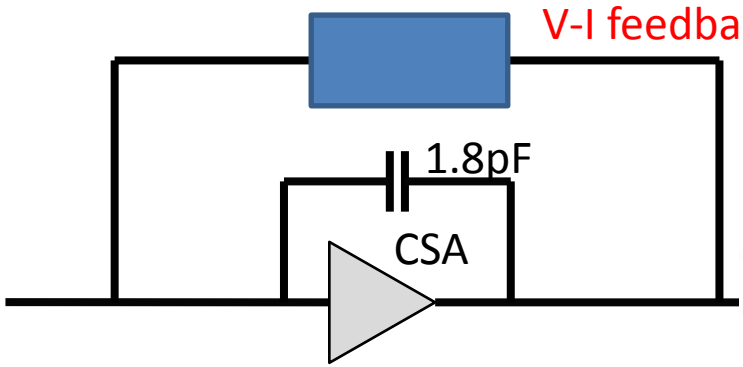
- *Linearity*
  - *V=V(out)-V(baseline)*
  - *Zin=10Ohm*
  - *No gain optimization*
  - *Good linearity is seen.*

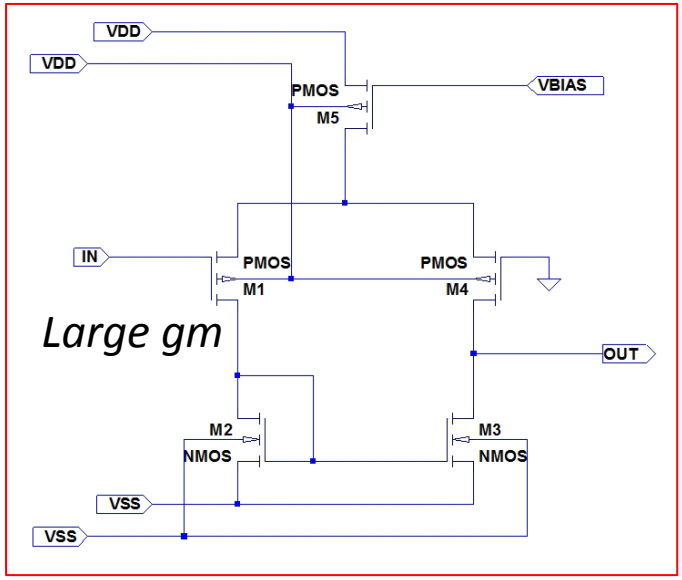


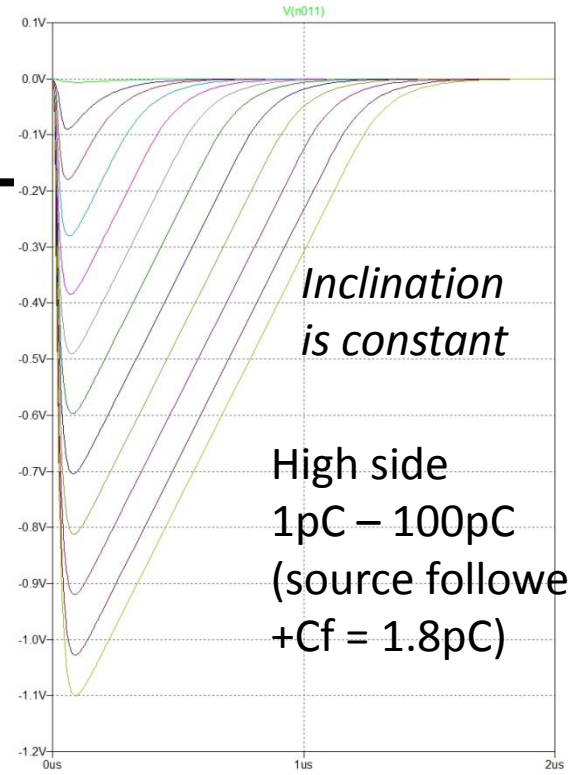
- *Need to optimize CMOS parameters (gm, W/L, I etc) and gain according to realistic conditions.*
  - *One of the crucial issues is how large impedance the transmission line has….*
    - *We are planning to use long line for raw signal driving (10cm).*
    - *Conductance, capacitance, resistance should be carefully evaluated.*

QTCv2

- *QTC without CMOS switches (Taku)*
  - *Constant current feedback by sensing the output voltage.*



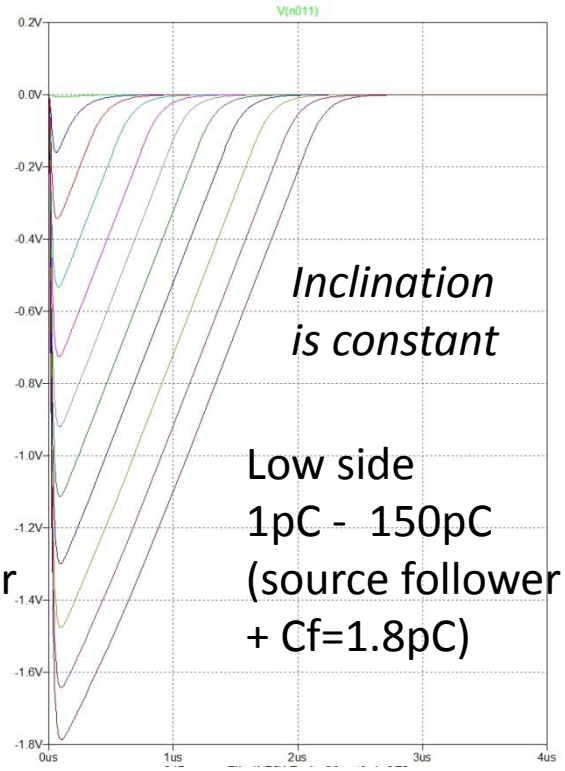




Inclination is constant

High side
1pC – 100pC
(source follower
+Cf = 1.8pC)

2u



Inclination is constant

Low side
1pC - 150pC
(source follower
+ Cf=1.8pC)

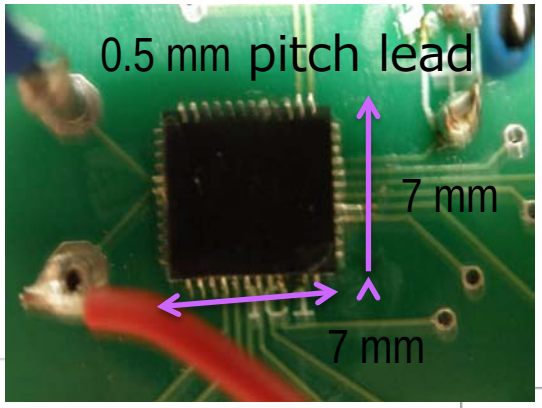
2u 4u

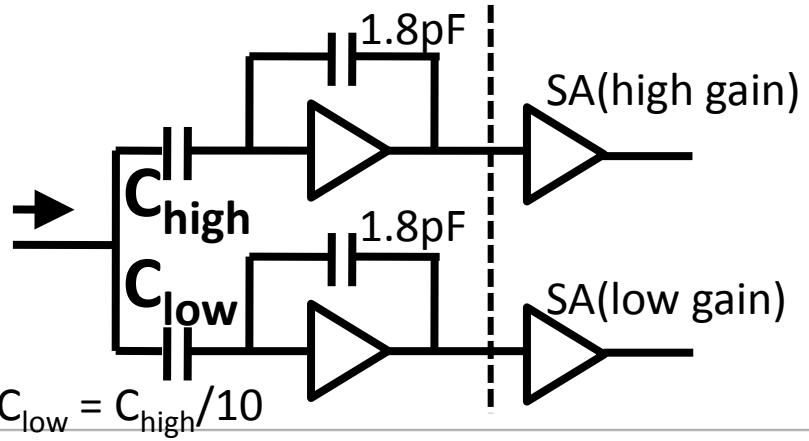
R&D of Dual CSP

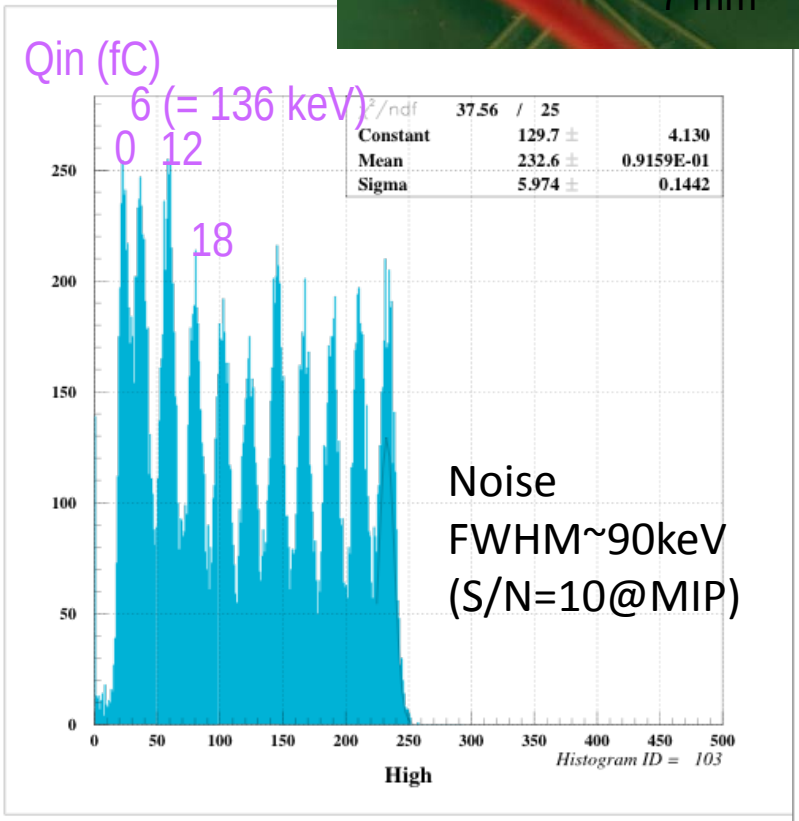
Chip size 1 mm ×2 mm

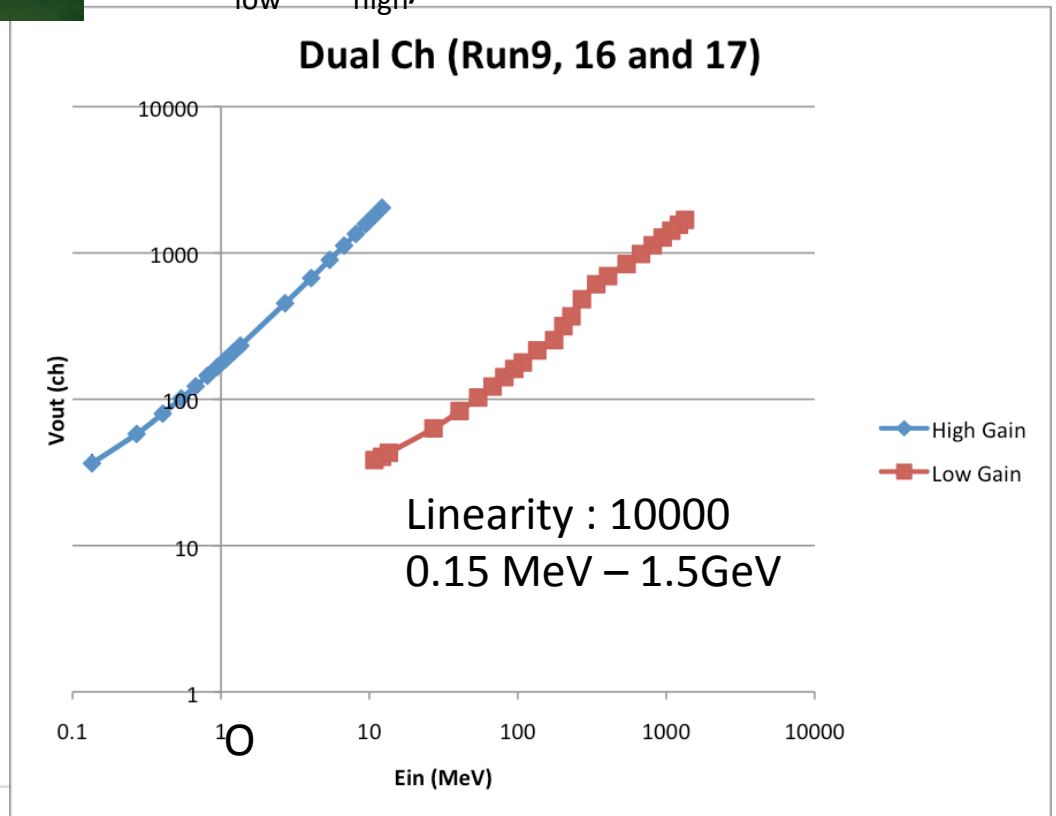
One channel for H/L.

20mW/ch

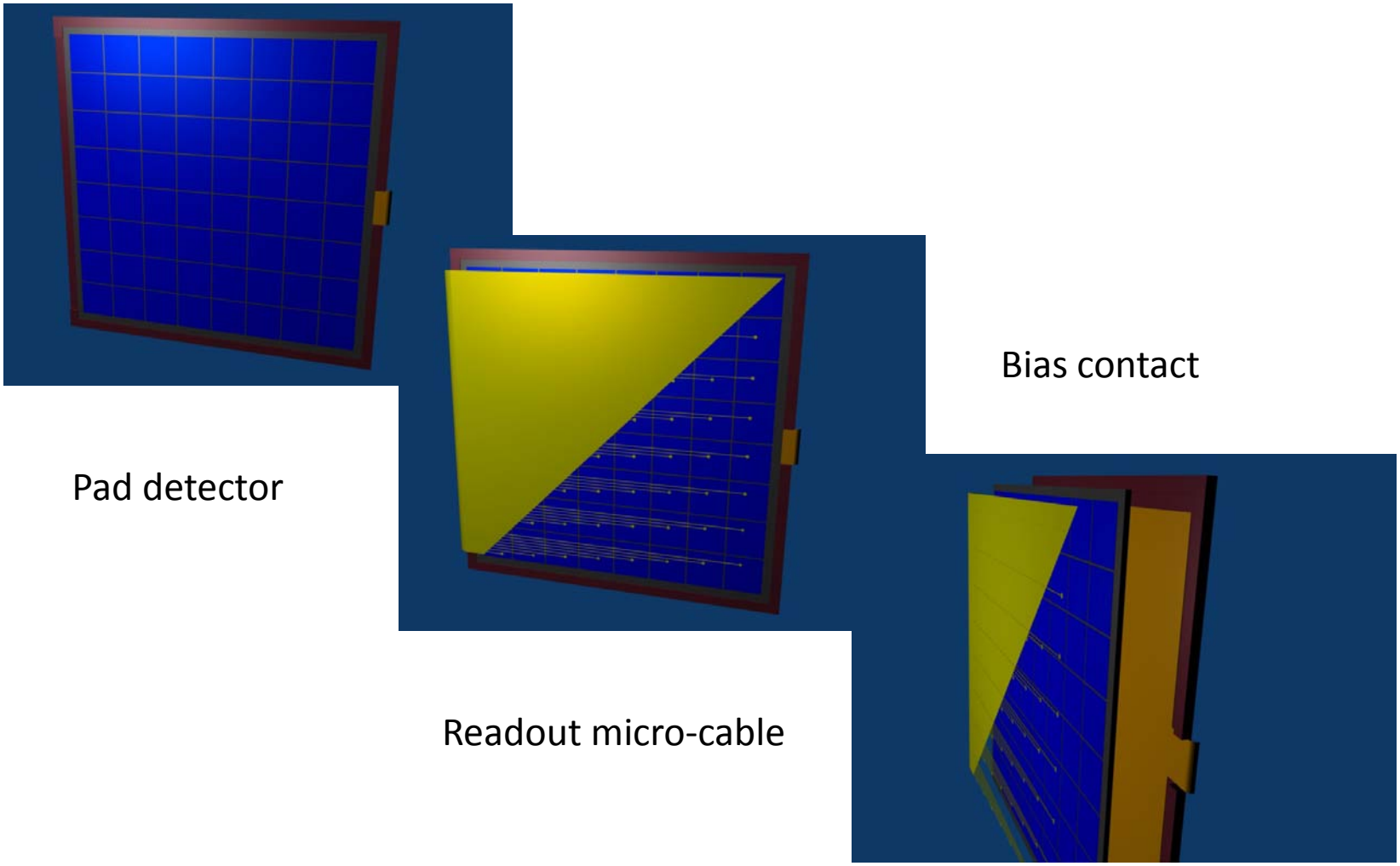






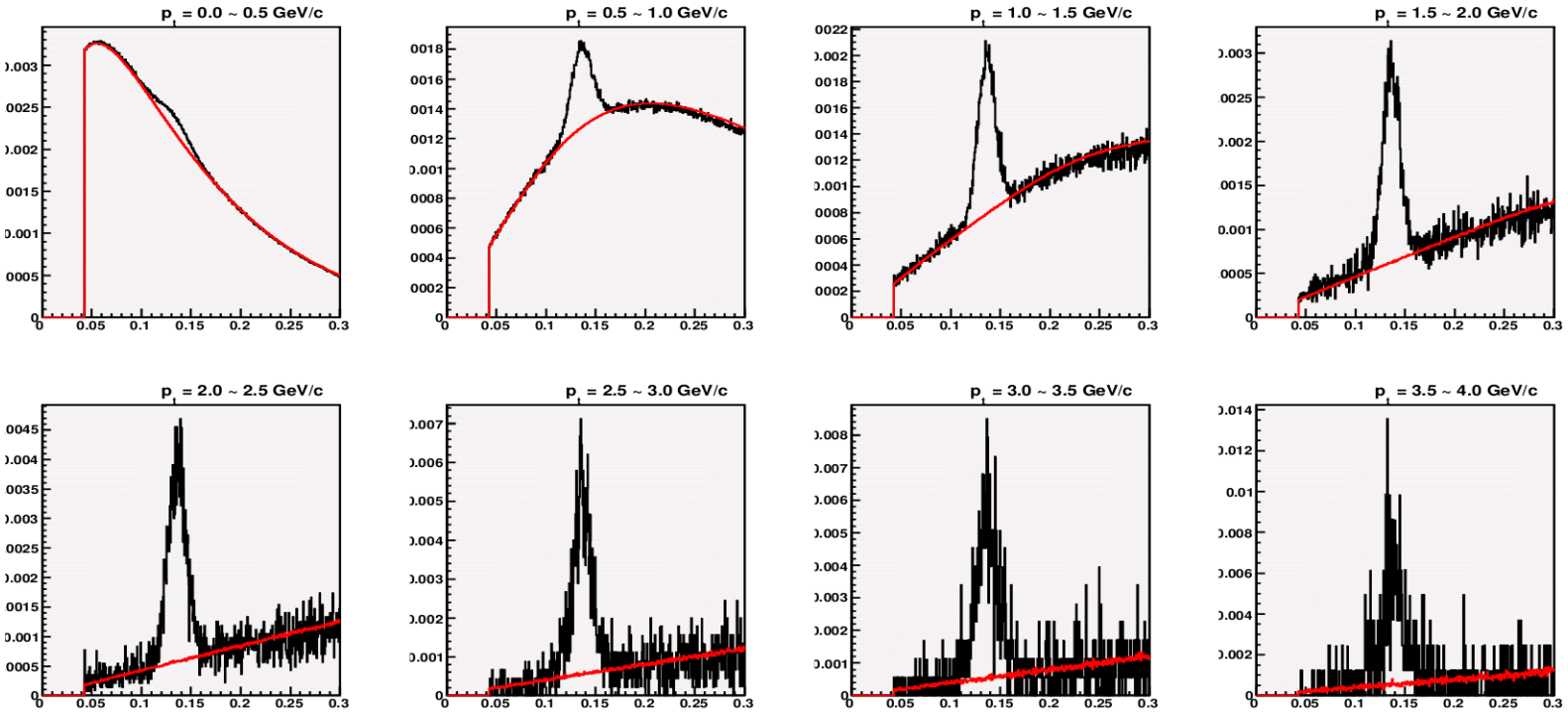


Detector, micro-cable, holder



Inv. Mass in p+A using Si-PADs

- *Two photon invariant mass at 3 < η < 3.5 from HIJING 8.8 TeV p+Pb events*
  - *Energy and position are smeared according to the resolution*

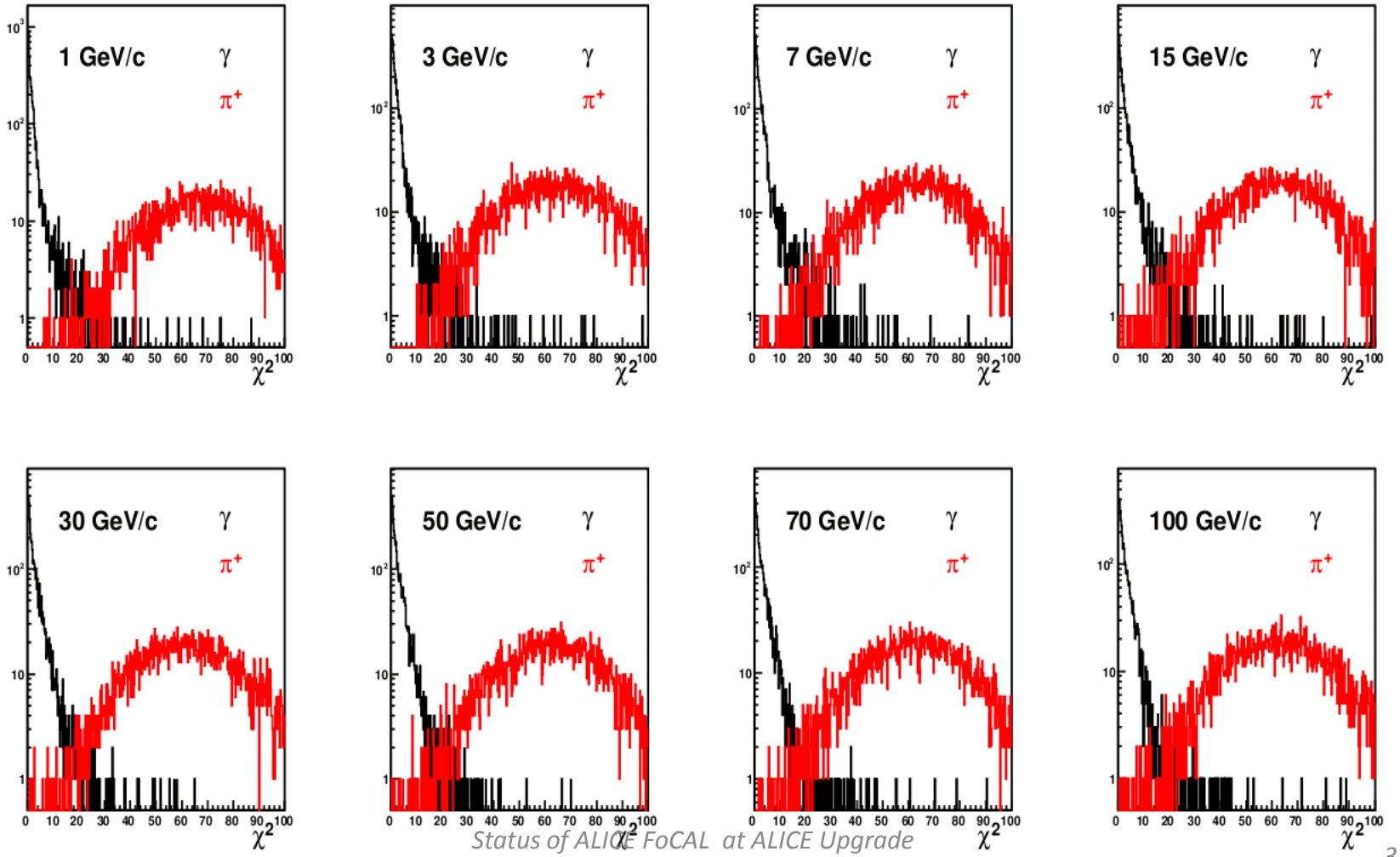


S/N ratio

π^0 p_T (GeV/c)	$0 \sim 0.5$	$0.5 \sim 1$	$1 \sim 1.5$	$1.5 \sim 2$	$2 \sim 2.5$	$2.5 \sim 3$	$3 \sim 3.5$	$3.5 \sim 4$
$\eta = 3.0 \sim 3.5$	0.13	0.41	0.97	1.62	2.45	3.12	3.65	4.03
$\eta = 3.5 \sim 4.0$	0.17	0.48	0.97	1.72	2.20	2.95	3.08	3.15

Rejection of charged particles

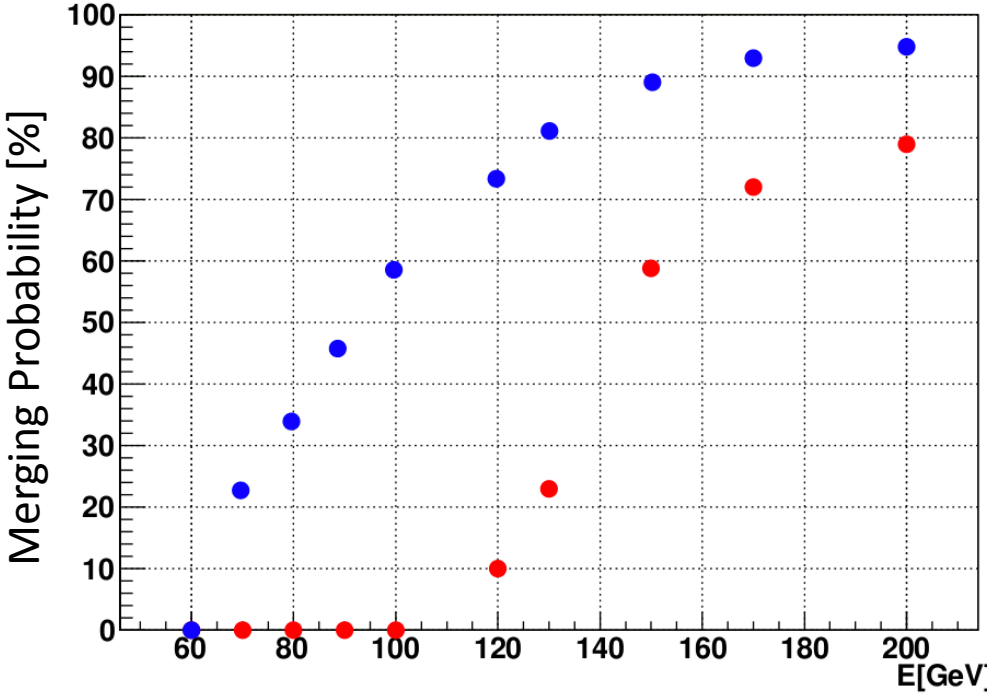
- *Longitudinal shower shape analysis*

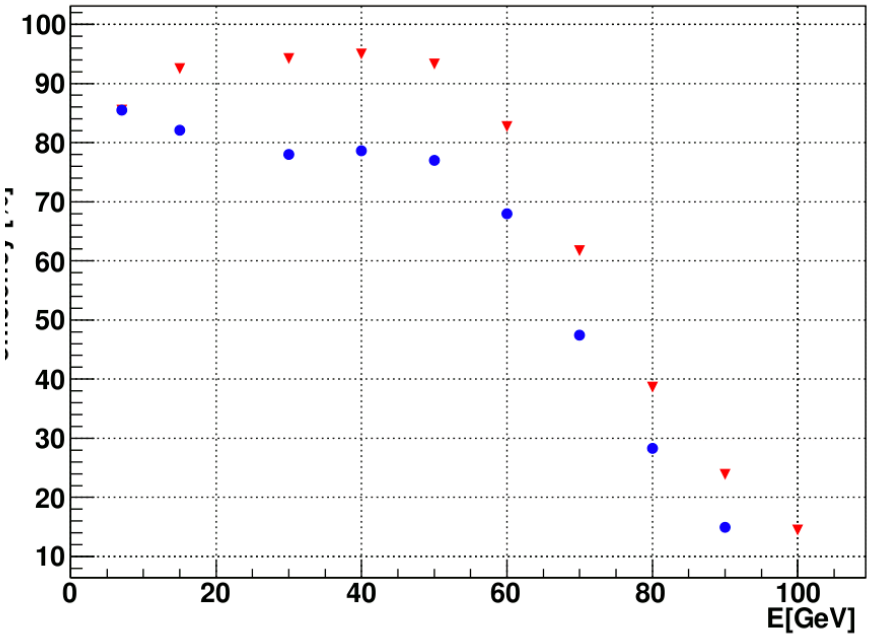


Pi0 Reconstruction using PADs

Two gammas enter the neighboring pads
Two gammas share the same pad

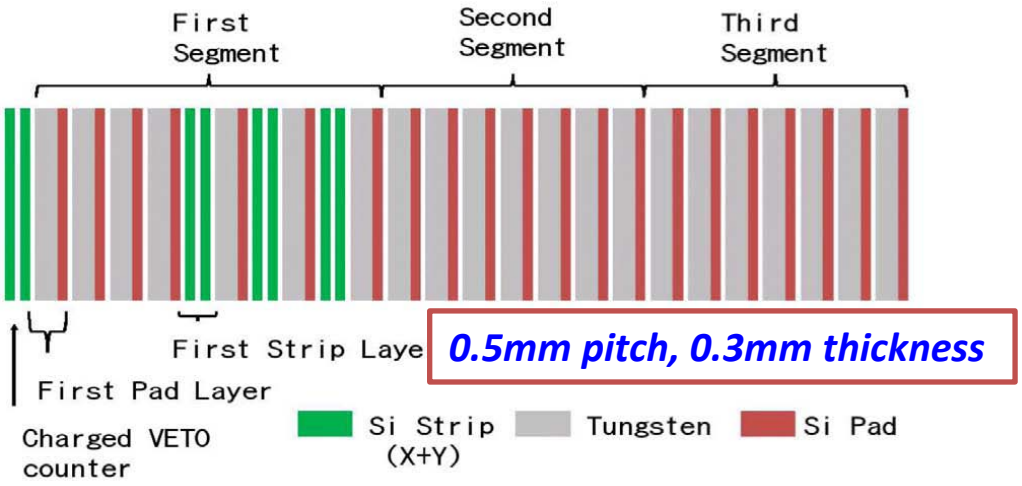
Reconstruction efficiency
Reconstruction efficiency with energy asymmetry cut (< 0.8).





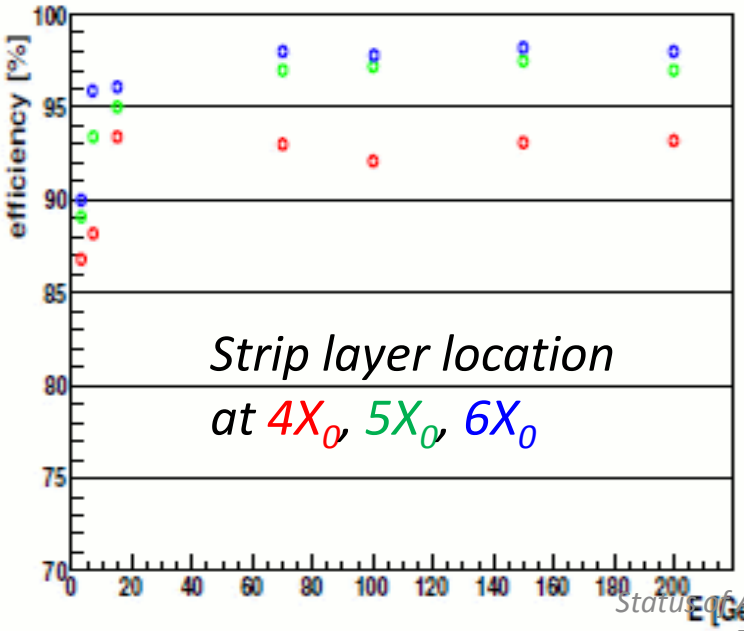
- Pi0 up to 60 GeV (pT = 6 GeV/c at h = 3) can be reconstructed using the Si-pads only.
- For pi0 above 60 GeV, finer hit position information is needed.

Performance of the strips

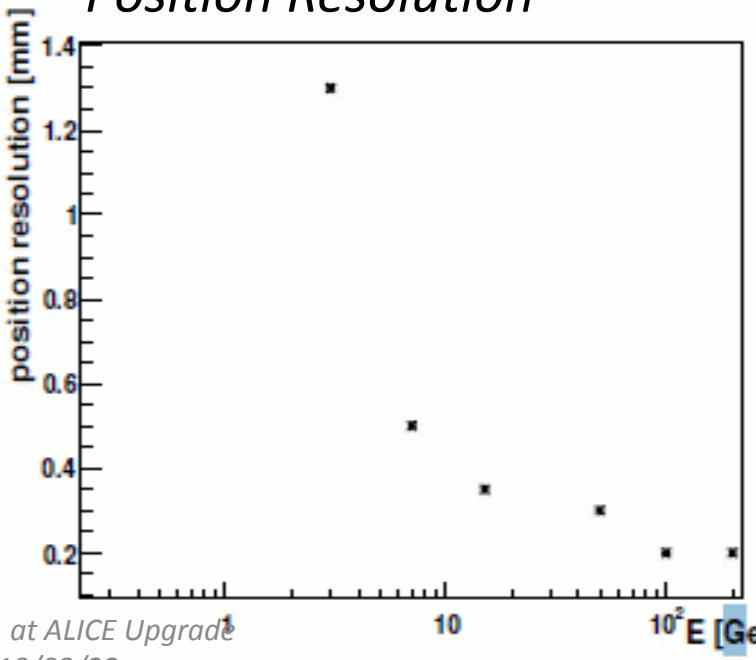


- *Detection efficiency: ~95% for photons with E > 10 GeV*
- *Position resolution: better than ~0.4 mm for photons with E > 10 GeV*

Detection Efficiency

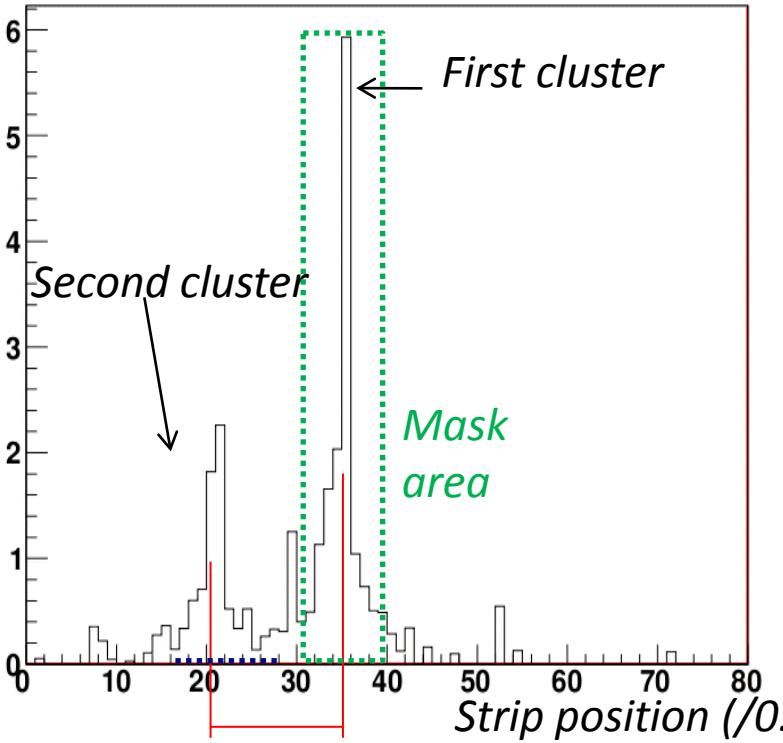


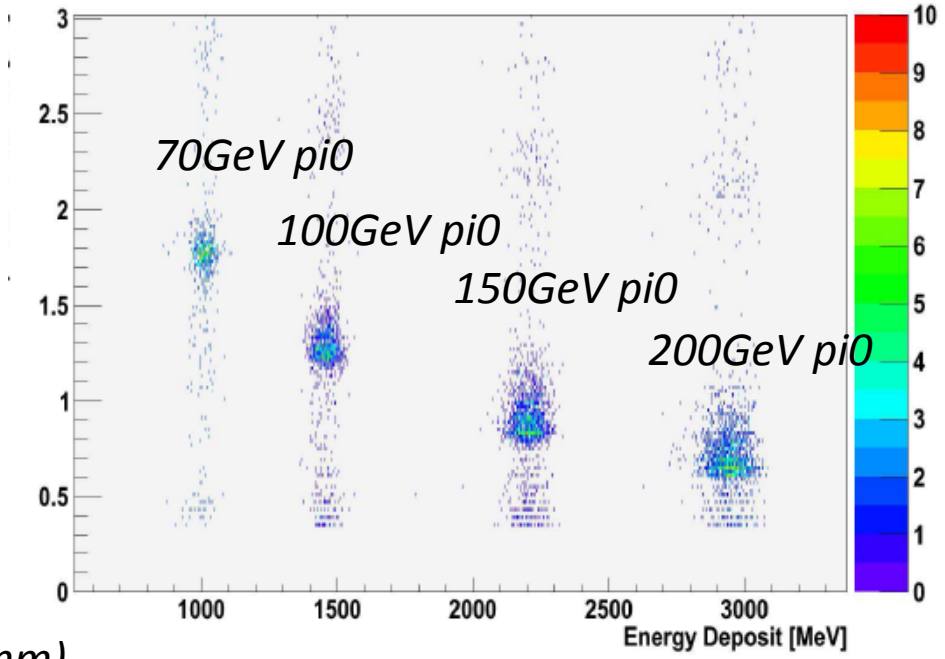
Position Resolution



Pi0 reconstruction using Si-Strips

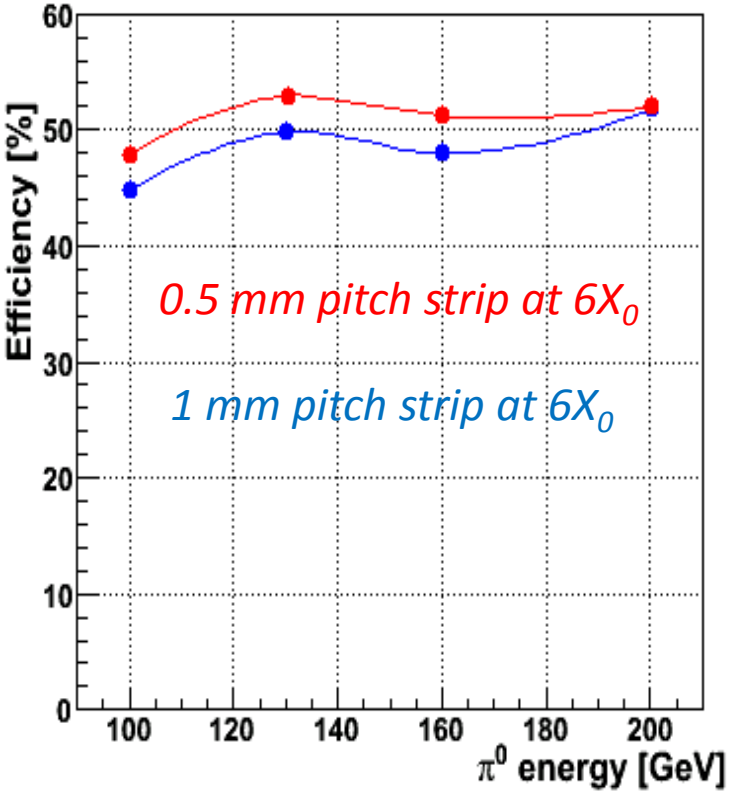
- *Two clusters in the Si-pads starts to merge into one cluster when the two-hit distance is below 2cm (for 1cm x 1cm pads)*
- *Locate a cluster with large energy deposit in the Si-pads & define search region in the Si-strips*
- *Search for two clusters & obtain distance between the clusters*



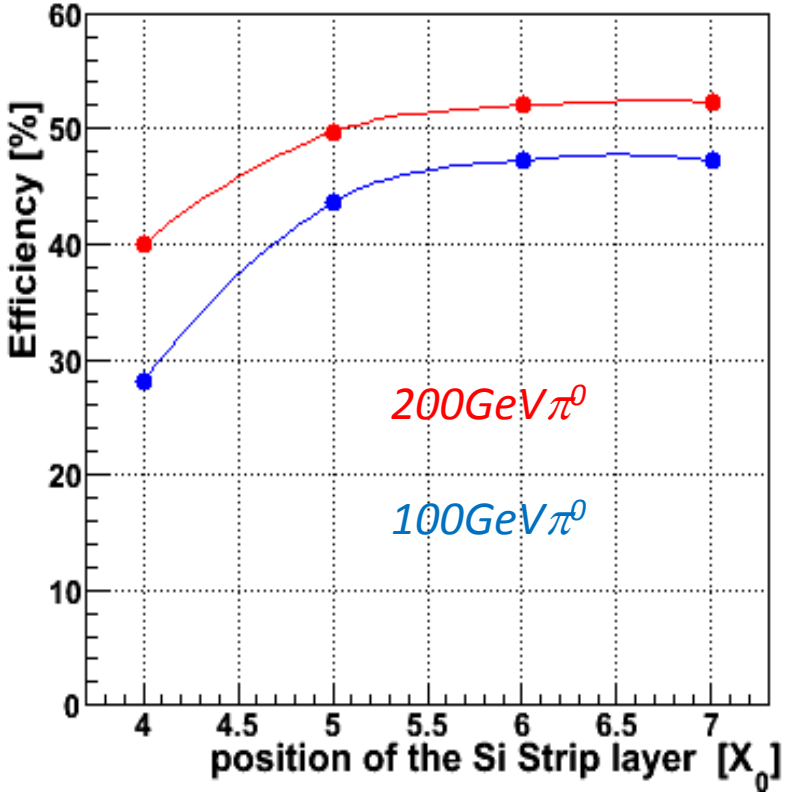


Pi0 reconstruction using Si-strips

Efficiency vs. pi0 energy for 1mm, 0.5mm strip pitch



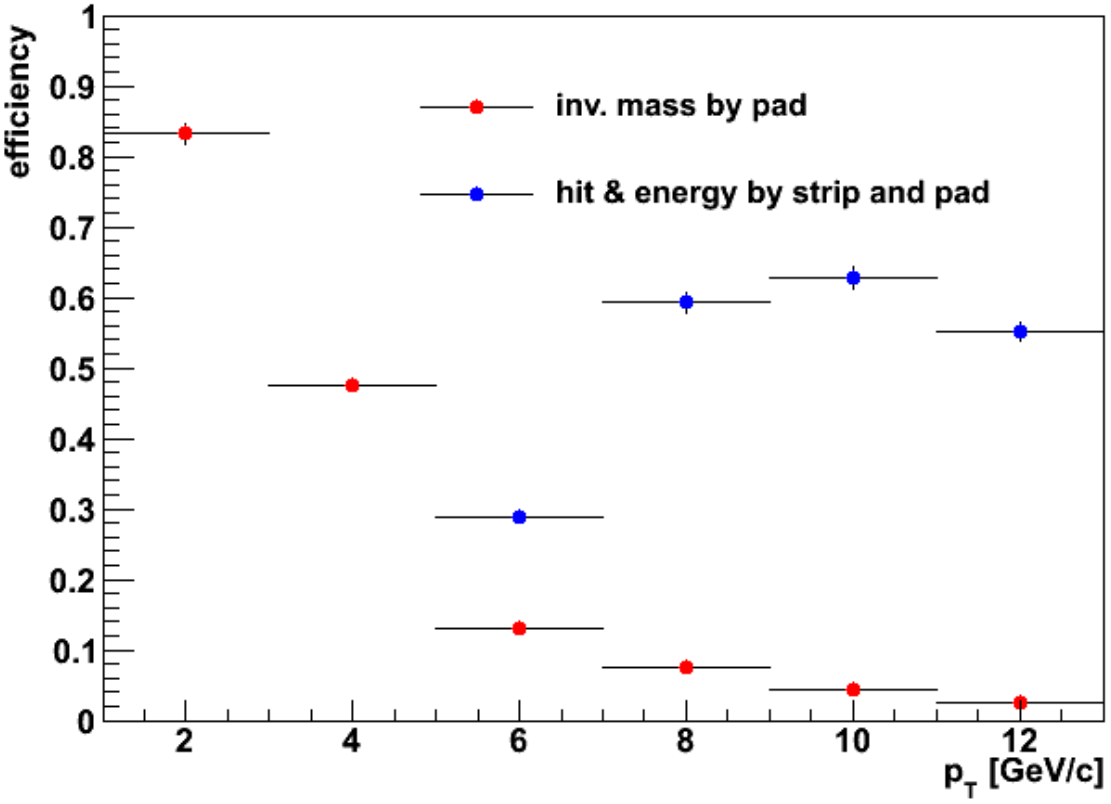
Efficiency vs. position of the strip layer



- *Tentatively obtained efficiency at present is ~50% -- trade-off with fake single photon probability*
- *Further efforts will be made to reconstruction algorithm*

Pi0 simulation by Aliroot

- *Obtained through AliRoot*
- *Input pi0 : 1<p_T<13 GeV (16<E<215 GeV) at η=3.5*



Pi0 identification efficiency using Invariant mass reconstruction with pads

- *effective for low pT*

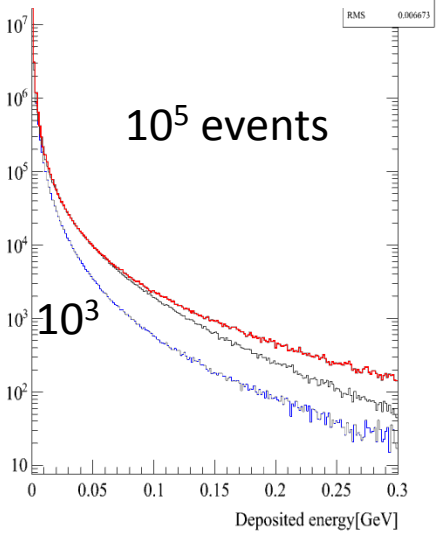
Pi0 identification efficiency using two hit @ strip and merged energy with pad

- *effective for high pT*

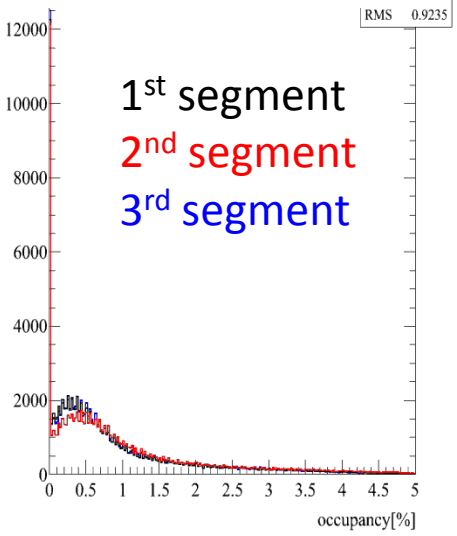
Occupancy

- *Detector occupancy and deposited energy*
  - *Average: 0.9% (MB), 2% (hard process)*
  - *Maximum: ~ 5%*
  - *Event rate is another important issue to see and this will be done.*

Deposited energy

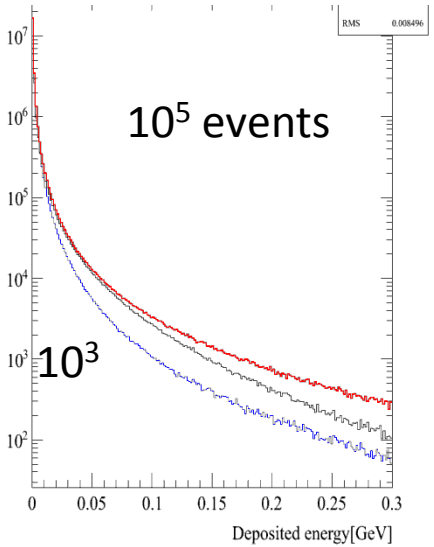


Occupancy

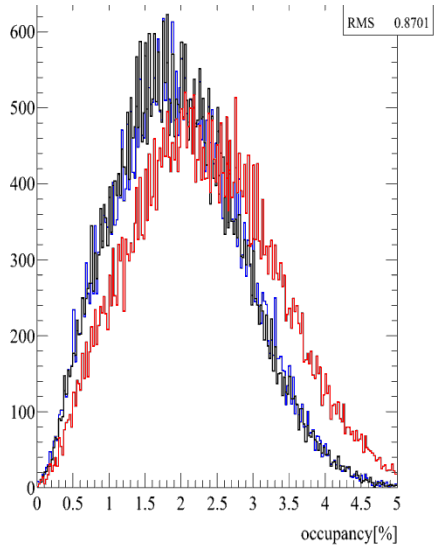


Minimum bias

Deposited energy



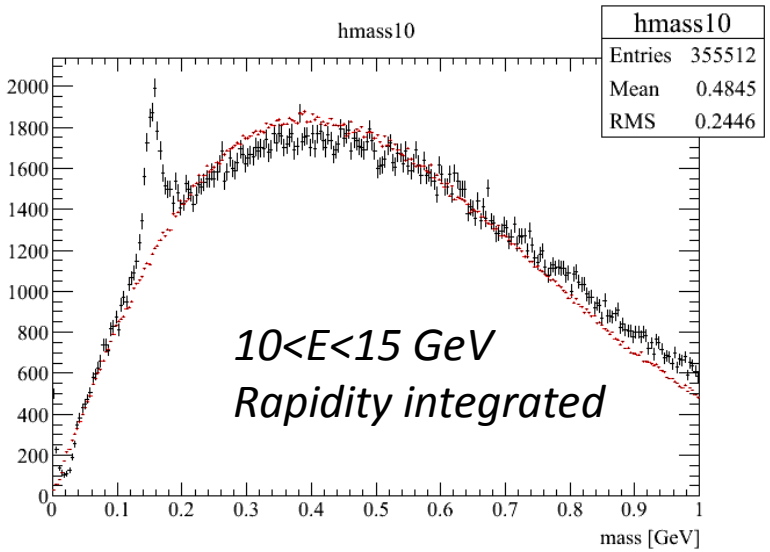
Occupancy

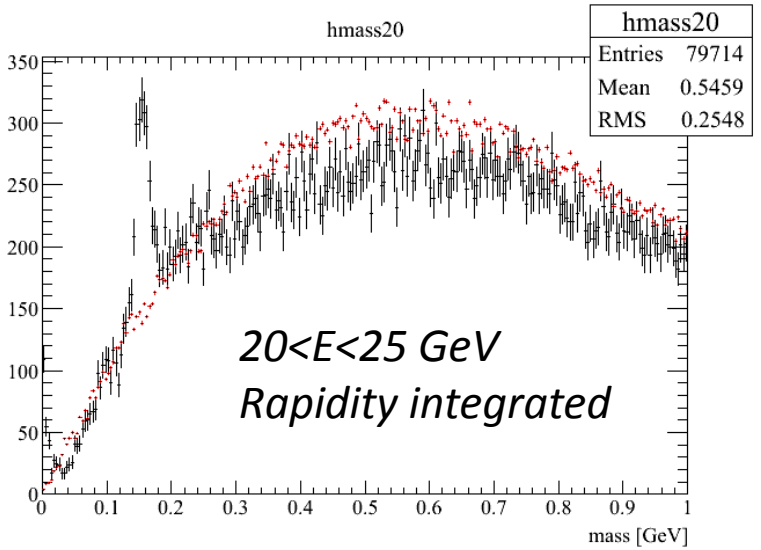


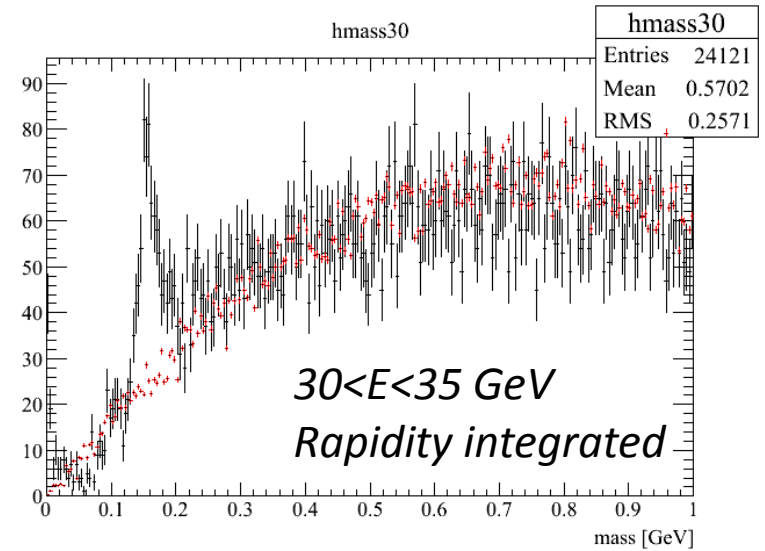
$\hat{p}_T\,(\mathrm{GeV}/c) \in [20,30]$

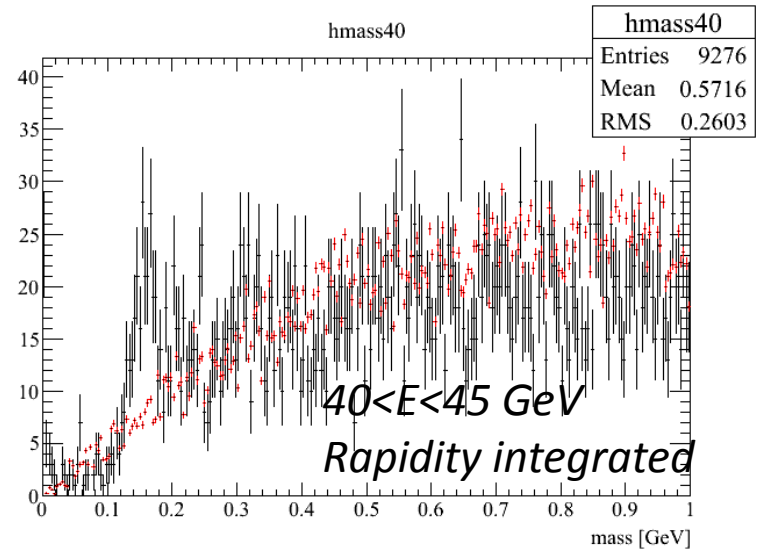
Pi0 in p+p MinimumBias

- *Only pads information is used (no CPV, no strip)*





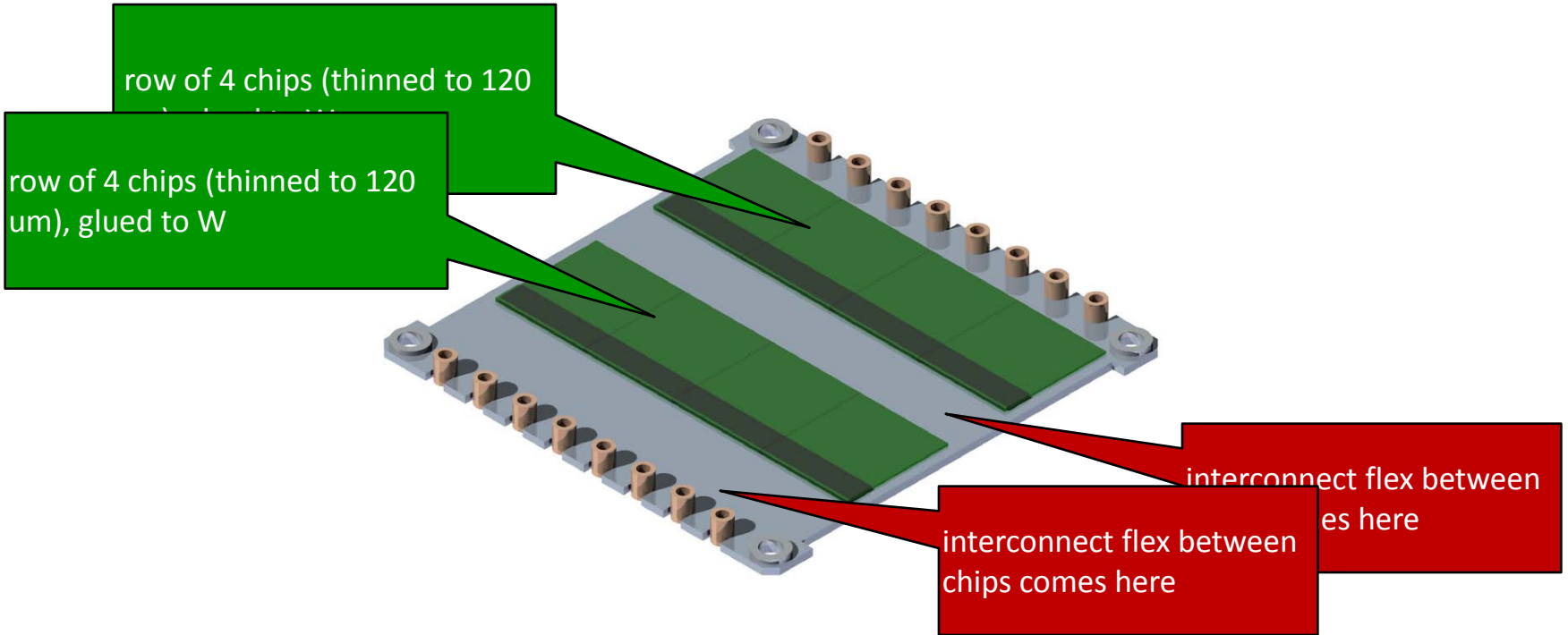




One layer, split in two halflayers

one halflayer

- 1.5 mm W
- W is good heat conductor 170 W/mK (Al 240 W/mK)
- estimated heat resistance ~1 K/W
- no additional interconnect layer/ mounting board



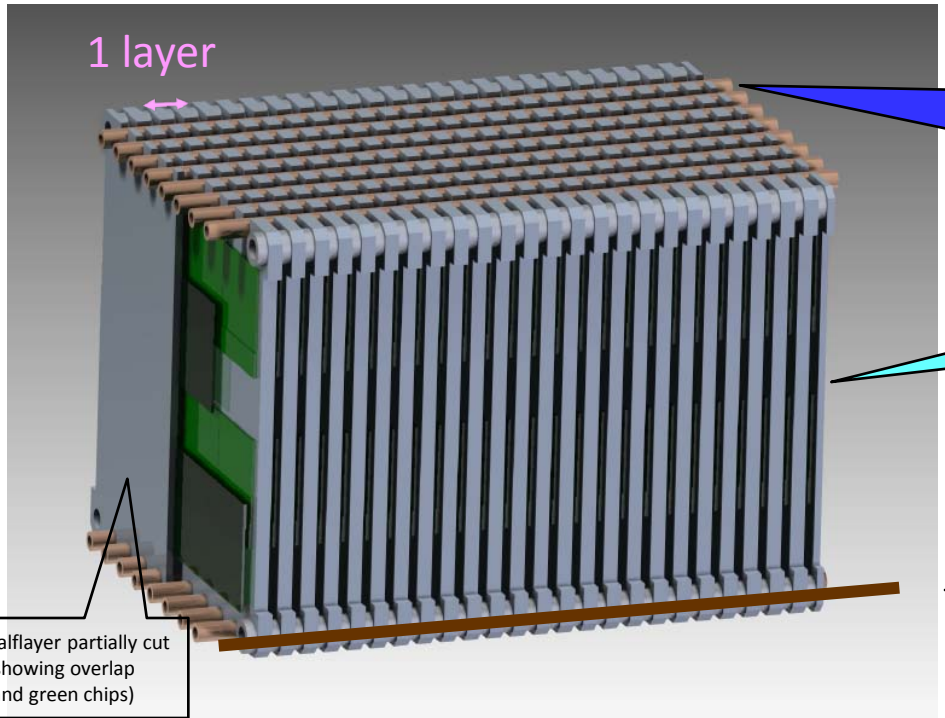
One layer, split in two halflayers

1 layer = two halflayers mounted face to face

- 3 mm W
- 16 chips, their dead zones overlapping
- 4 flextails sticking out
- total thickness 1.5 + 0.5 +0.5 +1.5 mm

  further reduction towards 0.5 mm in total for sensors and cables seems possible,

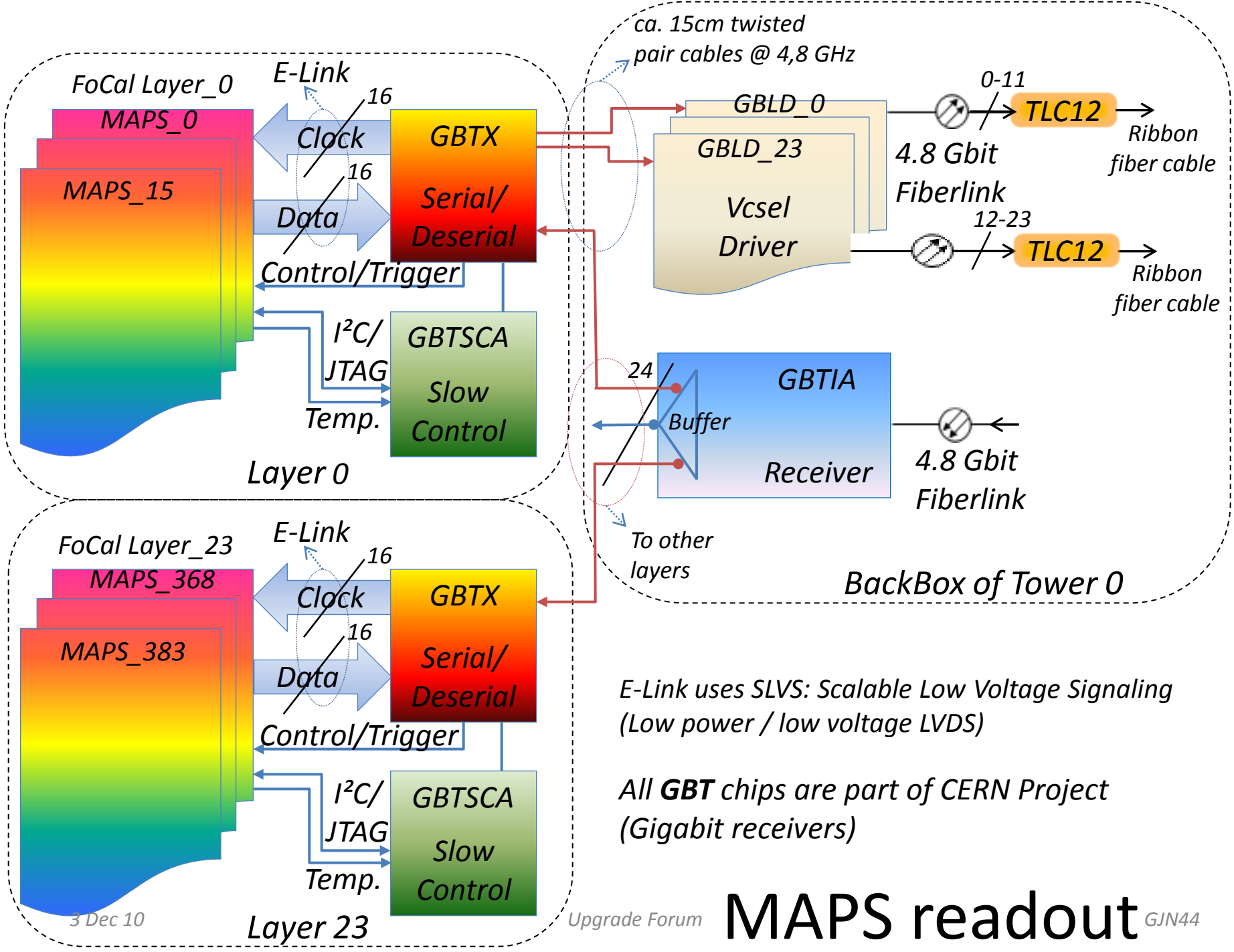
  requires gluing all layers together



cooling pipes at sides will be inserted after assembly of tower

these sides for cables

tension rods keep stack together (prototype)



E-Link uses SLVS: Scalable Low Voltage Signaling (Low power / low voltage LVDS)

*All **GBT** chips are part of CERN Project (Gigabit receivers)*

MAPS readout

Two gamma separation

- *Event display*