Memo: A LabWindows based HV Control System for PHENIX Drift Chamber Operation

summary of design parameters and performance achieved

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A LabWindows based HV Control System for PHENIX Drift Chamber Operation

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design goals:

- software to enable operation and control of the PHENIX drift chamber with its genuine supplies and hardware
- standalone system for laboratory requirements during commissioning of the detector but flexible and handy to be used also in the experimental hall and eventually to be interfaced to other enviroments
- learning phase: What is the essential information to monitor? How can one present it in a comprehensive and clear form?
- user−friendly interface to set and monitor HV parameters in a way related to the detector geometry
- built−in procedures to enable easy recovery from tripped channels

platform:

- LabWindows PC software (C language) under WindowsNT

components:

- 2 LeCroy mainframes model 1458 for operation of one full drift chamber (consisting of 20 "keystones")
- 10 HV modules model 1471 (à 8 ch.): Cathode supplies
- 10 HV modules model 1469 (à 24 ch.): P, G and B supplies
- communication PC ↔ mainfraimes via ARCNET link
- ARCNET driver: ARC20.c code (M. Justice , D.Fong)
- commands structure: CCS header + HEX number string

user interface:

- main control window with several pop−up windows
- HV status display window (main display)
- user−friendly setting of HV parameters (voltages , trip currents, ramp rates), based on the detector geometry (keystones) rather than HV crate slot and channel numbers;
- save/load of mainframe settings
- easy−to−read display of applied voltages, measured currents and channel states: ON, NOT READY, TRIPPED
- automatic procedure for trip recovery
- trace plots of measured parameters + data base access (possible to implement)

trip recovery: initiated by operator, then automatic sequence of "channel disable" and "channel enable" commands, matching the requirements of the individual HV module hardware (e.g. wait time for completion of HV ramping with bulk supplies)

monitor speed: ARCNET+ HV mainframe related. 4 keystones (4 LeCroy HV modules) are read at a time. Information on channel states, voltages and currents is acquired module by module:

- av. time to receive a response to a single HV command: $\leq$ 0.5 sec
- av. time to retrieve all information from 4 keystones: ~ 3.0 sec
- av. time for a monitor cycle over the entire detector: ~ 15 sec

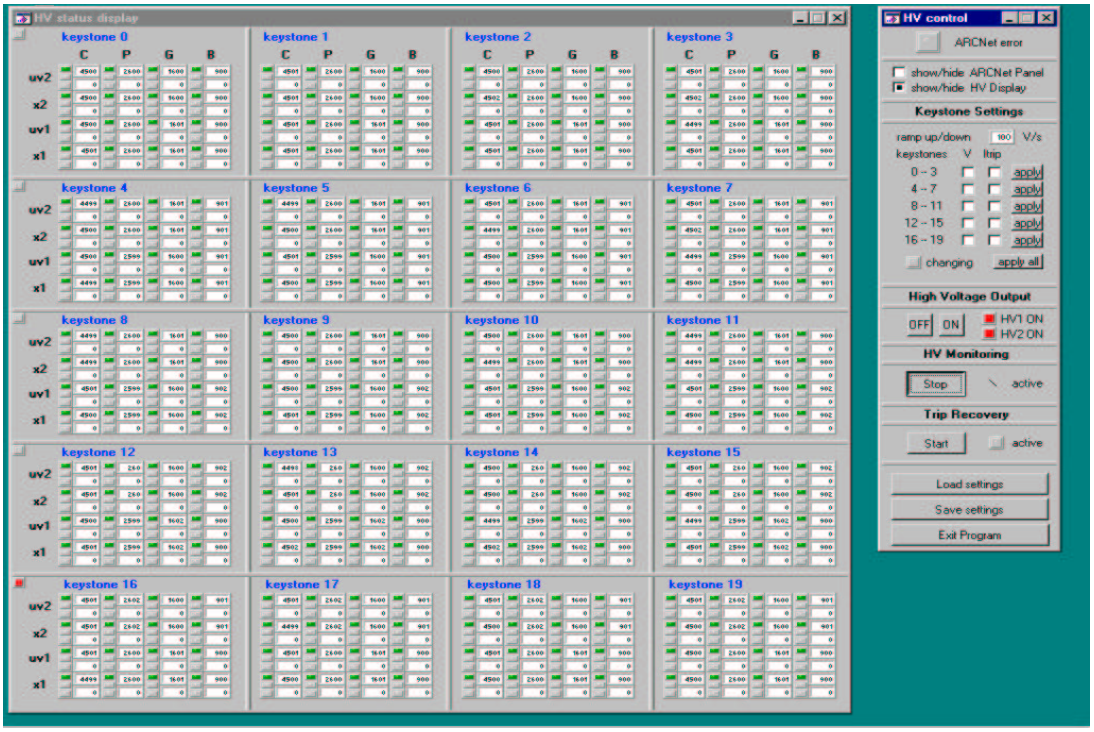

Fig. 1: HV status display for 20 keystones (left). Main control panel (right).

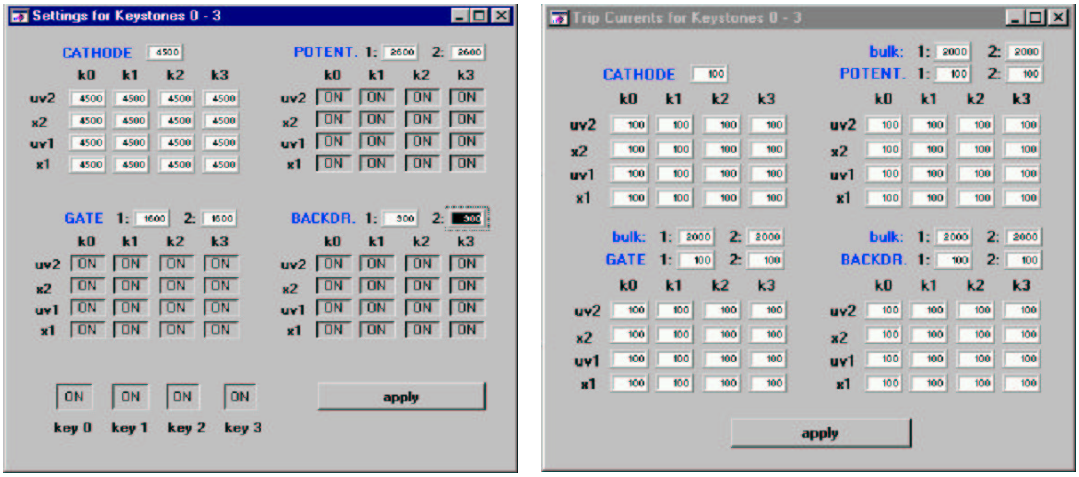

Fig. 2: Panel to enter HV parameters for 4 keystones: Voltage panel (left) and trip current panel (right).

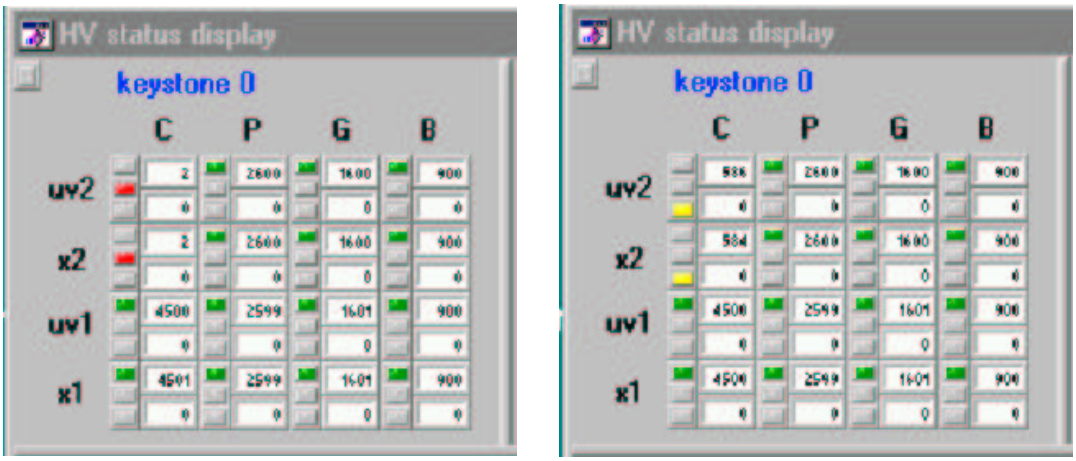

Fig. 3: HV status display for one keystone. The high voltage is supplied for C=Cathode, P=Potential, G=Gate and B=Backdrift wires in four orientations x1,uv1,x2,uv2.
For every supply channel, a display cell shows the measured voltage in Volts (top number), the measured current in μA (bottom number) (here always zero because the drift chamber was not connected to the supplies) and three lights according to the channel status:

- green: OK, voltage matches the desired value
- yellow: NOT READY, voltage does not match the desired value
- red: over−current has occurred, channel has TRIPPED.

Left display: the Cathode supplies x2 and uv2 are tripped.
Right display: after initiating the trip recovery procedure, the trip status is canceled and the channels are ramping up again. The yellow lights indicate NOT READY until full voltage has been reached.

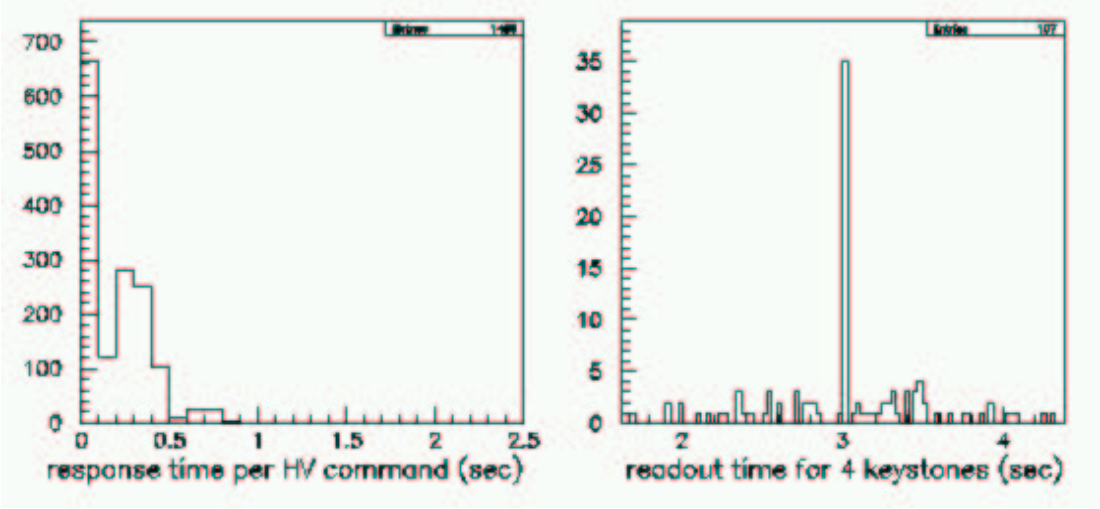

Fig. 4: Monitoring speed: time to receive a response from the mainframe to a single HV command (left histogram), time to retrieve all information from four keystones (right histogram).