Status report of ASIC

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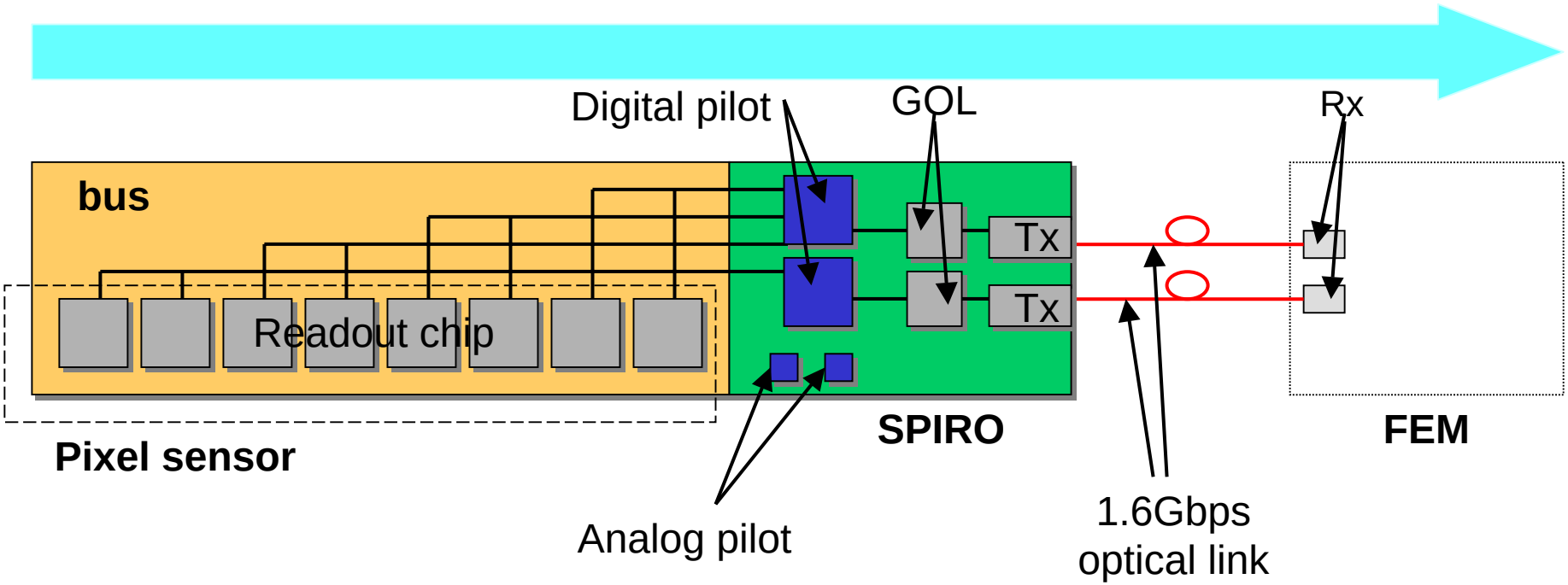
1. Digital pilot ASIC V2
2. Package
3. Test system

Block diagram of the readout part



Digital pilot: Readout chip control and data-readout

Analog pilot: voltage control and thermal monitoring

GOL: parallel to serial converting, 32bit ➡ 1bit stream

Digital pilot ASIC V2

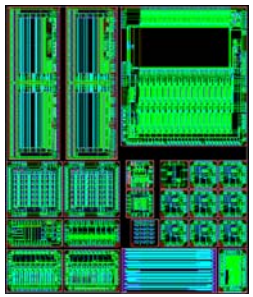
- Adding **Ethernet** control

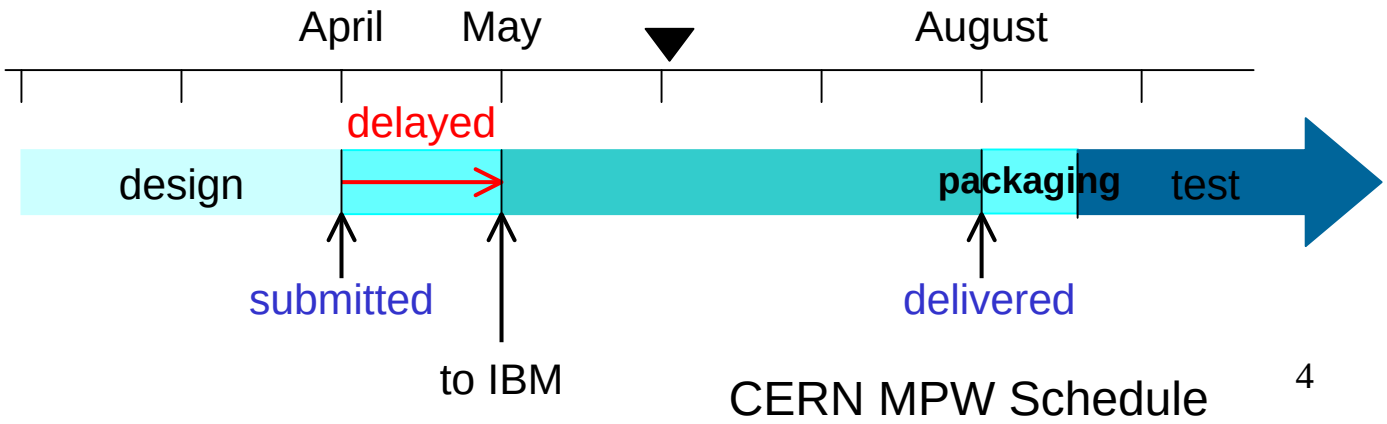
  Previous data-link is **G-link**. There are no receiver in market for our 1.6Gbps G-link.
- Adding data alignment mechanism.
- Adding parity bits to check data parity
- Adding trigger counter.
- Rearrange pin-assignment for optimize to GOL connection and power/GND pin.

Digital pilot ASIC

- V2 design was submitted at 31th March. (Trailer will be sent to IBM at the beginning of May. It is about one month late.)
- V2 chip will be delivered at the beginning of August. It will take about half month to package the chip.

MPW-Trailer





CERN MPW Schedule

Packaging

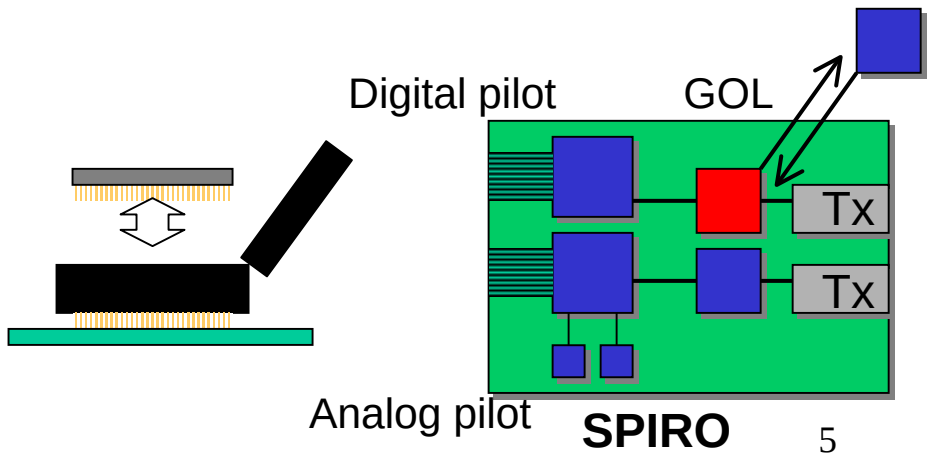
Why we use the packaged chip? (for chip test, board test, and actual board if possible [it depends on board size?])

⇒ easy to handle, easy to change a bad chip

For example, there are 6chips on the SPIRO, if 95% yield per one chip, total yield is $(0.95)^6$=0.74%

- Socket will be delivered in a month for chip test and board test.

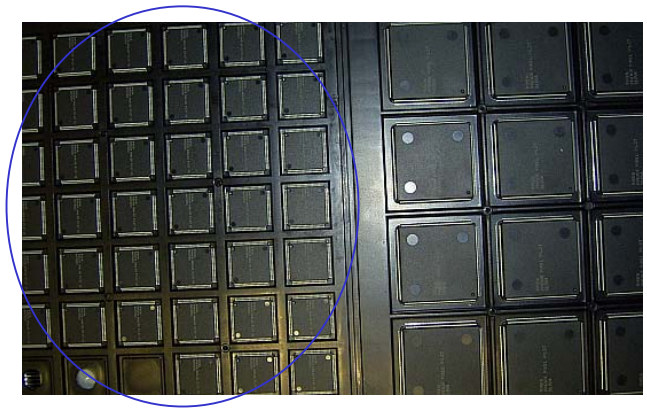
Chip	Size (bare)
Digital pilot	28x28mm (6x8mm)
Analog pilot	14x14mm (3x4mm)
GOL	13x13mm (4x4mm)



Analog pilot chip

- 39chips have been packaged
- Package=14x14mm, 100pins

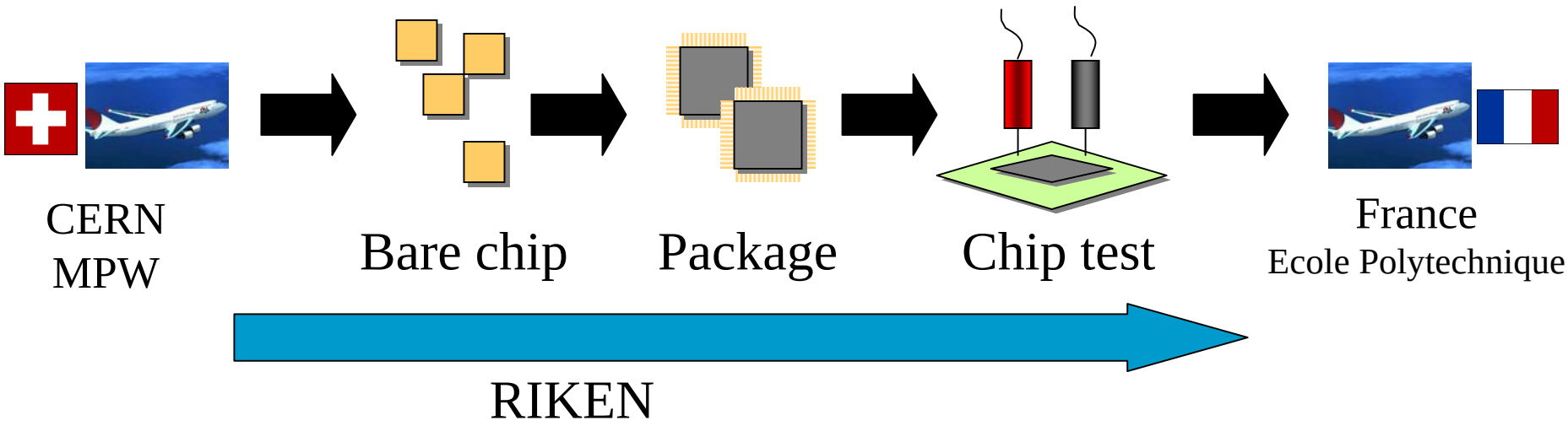
- Chip socket will come in a month. (will come in a month)



Analog pilot digital pilot

Chip test

- We will test chip at RIKEN-Wako.



Now we are developing test system.

ASIC test system

- Digital pilot ASIC
  - V1 test system was completed (H/W and S/W).
  - Minor modification for V2.
    - G-link -> Ethernet
    - Pin assignment
    - Software
    - Socket
- Analog pilot ASIC
  - Logic diagram design was completed.
  - Chip packaging was completed.
  - Socket will come soon.

Summary

- Digital pilot V2 is in process. We can get chip at the end of August.
- Analog pilot is packaged and ready. Socket for Analog and digital pilot will be available in a month
- Test system for all ASIC have been developing in RIKEN.