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**Automated handling of ultra-thin silicon wafers**

A typical target thickness for ultra-thin 200mm and 300mm silicon wafers is about the same thickness as a sheet of paper - ~ 40µm. Thin wafers are the substrates in demand for Smart Cards, MEMS, stacked die, photovoltaic cells, and power devices. Representative business drivers behind these applications include the demand for larger Smart Card die with the same flexibility and strength as smaller die used in early-generation Smart Cards, and the need for more portable memory or more processing capacity in the same package footprint being achieved by stacking thin die [1, 2].

Year	Wafers <150µm (millions)
1999	1.60
2000	3.73
2001	4.35
2002	4.98
2003	7.31
2004	9.79
2005	11.62
2006	13.47

Source: J. Walker, Gartner-Dataquest

According to Gartner-Dataquest, in 2002, production of wafers with a final thickness below 150µm will be about 5 million, growing to more than twice that many by 2005 (Table 1); this trend aligns with forecasts of package thickness decreases.

High production yields with thin (100-250µm) and ultra-thin (<100µm) wafers require new considerations in wafer processing, particularly for automated wafer handling. Wafer yield targets based on experience with thick-wafer processing lines are not relevant; operations managers who target ultra-thin wafer breakage rates at <0.2% will find it difficult to achieve this goal with conventional wafer handling.

**Consider the beast**

You can intuit that ultra-thin wafers are extremely fragile, but also consider that they:

- bow and warp under the stress of device films applied on one side;
- sag under gravity;
- stick to surfaces by surface tension forces of process liquids (i.e., ultra-thin wafers are so light that liquid between a wafer and another solid surface causes the wafer to stick to that surface with a force stronger than gravity);
- flutter in the slightest airflow from air conditioning or even passing people;
- have very thin, razor-sharp edges when ground thin from Semi standard prime wafers, which have gently rounded full-thickness edges; and
- cannot be stored or shipped safely in conventional wafer cassettes.

**The automation challenge**

Single-crystal silicon is a brittle material, subject to instantaneous and catastrophic failure when local stress (usually at a stress-concentrating flaw) exceeds the ultimate strength of the silicon. In general, conventional automation methods for normally thick wafers often apply fatal stresses to thin wafers due to bending, edge contact, and vibration. Common automation requires clever modification or replacement with new approaches to achieve acceptably low wafer-breakage levels (e.g., <0.1%).

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Figure 1. Ultra-thin wafer edge profiles a) after backgrinding and b) after grinding and an etch treatment by atmospheric downstream plasma to blunt the edge.

The edges of ultra-thin wafers are especially fragile (Fig. 1). These can cut into plastic end effectors or storage devices or can be chipped by contact with a hard object. Soft plastic contact surfaces can spread the contact area and minimize decelerations, but then are cut by the razor-like edge.

There are many issues and options to address as a fab moves into thin and ultra-thin wafer processing. The best wafer-thinning process combination is yet to evolve, and the optional procedures listed in Table 2 are at different levels of maturity. Exactly at which thickness level each is needed depends on the product and the available process equipment. Since the geometry (i.e., bow, warp, etc.) of the wafer depends on the applied device film stresses, the free-state shape becomes more dependent on the device film as wafers gets thinner. Comparing the appropriate processes for a ~50 $\mu$ m to a ~250 $\mu$ m wafer in Table 2, you can see that numerous new processes and handling methods will be required for ultra-thin wafer production.

#### "Thin" automation demands

It is important to consider many special automation procedures when handling ultra-thin wafers. For example, ultra-thin wafers are best kept flat against a wafer chuck at all times. They cannot be stored in an unrestrained free state between steps. Vacuum chucks that pull a wafer against a flat surface and special modified Bernoulli chucks that suspend the wafer close to a flat surface are effective in maintaining a wafer essentially flat. Commercially available adaptations of the Bernoulli principle (e.g., from SEZ America and Tru-Si Technologies) facilitate gentle handling of thin wafers without allowing the front device side to contact the chuck surface.

Thin wafers may be mounted on support carriers to avoid severe bending stresses. Several companies offer support concepts. For example, traditional backgrind tapes in various thicknesses are available. Tru-Si Technologies offers a high-temperature tape compatible with plasma etching. Wafer Solutions has a rigid polymer coating solution. Disco has a polyethylene terephthalatetrate tape and a tape-glass substrate.



Figure 2. A hand-held, modified Bernoulli transfer tool from Tru-Si Technologies being used to load wafers into an Achilles Thin-Wafer Pod.

One must also consider minimizing vibration and edge contacts and minimizing thermal stresses across a wafer due to temperature variations. For example, one important factor is to ensure that wafer drying after wet cleaning does not cause any surface tension forces.

It is also important to minimize handoffs from support chuck or end effectors. Tokyo Seimitsu, for example, has developed an integrated grinder-polisher-cleaner so that separate handoffs are not required. This is accomplished by moving the wafer (on the same chuck) from processing station to processing station on an indexing table.

Thin wafers must be cleaned and dried carefully. Cleaning ultra-thin wafers is a challenge; holding these wafers flat while cleaning means only one side is cleaned at a time. Particles can then transfer from the dirty to the clean side, however, during transfer from one holding side to the other. Marangoni-style cleaners are being adapted to address this issue, since wafers are gently cleaned and then do not have to be spun to dry.

Thin wafers must also be stored differently. Buffering between process tools is a problem for ultra-thin wafers unless the buffering storage device holds wafers flat. One common container for buffering or shipping is a "jar," "coin stack," or pod in which wafers are stacked horizontally, one on top of the other, in a round container with plastic or paper separators between each wafer (Fig. 2). So far, however, there is no standard geometry for these pods.

#### Minimizing stress

In addition to minimizing stress during handling, it is obvious that the extent to which thin wafers can be made more robust (i.e., more tolerant to any applied stress), the fewer wafers will be broken. Two important methods that make ultra-thin wafers more robust are minimizing or removing backgrinding damage and minimizing or removing edge chipping.

Removing microcracking under grind lines and gouges under chipped edges eliminates those critical flaws that make a wafer weak (i.e., flaws that result in fatal breaking at lower applied stress levels). For a given applied stress pattern, there is only one critical flaw - the one place that initiates a crack - so the more severe the flaws that are removed, the stronger the wafer.

Careful selection of grinder abrasive wheel grit size and gentle feed rates and rotational speeds, along with other process considerations, can minimize subsurface grinding damage [3]. However, one researcher has reported that x-ray measurements show that deeper subsurface crystalline defects are induced when wafers are ground to ultra-thin levels [4]. Could it be that difficulties in handling ultra-thin wafers before removing damage stressed the wafers and caused the defects to propagate deeper into the wafer surface? This may put additional burden on grind-damage removal methods for ultra-thin wafers.

Opinion differs on the optimum amount of material necessary to remove after grinding and the optimum technique for use in removing subsurface grind damage. Measurement of subsurface damage is sophisticated, and the requirement for full removal depends on the application. Currently, a number of thin die manufacturers are evaluating available alternatives. Most process engineers agree that the gentle action of etching is the superior removal method. Either wet chemical etching (e.g., SEZ America) or dry plasma, fluorine gas etching (e.g., Tru-Si Technologies) is an effective etching technique. Scanning electron microscope (SEM) images of a ground wafer surface before and after dry plasma etching reveals how it improves the silicon surface (Fig. 3). Notice how the rounded pits of the etched surface have fewer sharp microcracks. Wet chemical etching provides similar surface improvement. Post-grinding etching also rounds off wafer edges (see Fig. 1).

Polishing is also proposed as an effective means of removing grind damage. This could involve removing top layers by chemical mechanical polishing (CMP; e.g., technology provided by TSK, Strasbaugh, and others) or by dry polishing (e.g., Disco.) However, the relatively slow polishing removal rate usually limits its application to removal of only a few microns. Higher removal rates are obtained only with relatively high downforce on a delicate wafer, which may induce further penetration of subsurface microcrack damage.

### The role of data

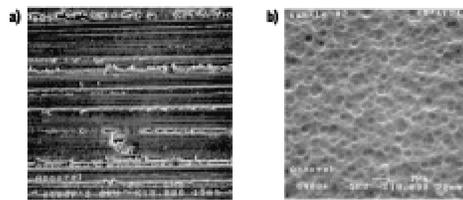
As our knowledge about safe automated handling of thin wafers improves, objective data collection will prove to be extremely valuable. Environmental variables such as temperature, elevation, humidity, shift lengths, operators, etc., could all prove to be significant. Examination and recording of every break will be extremely useful, and archiving broken wafer pieces can be helpful for later examination (similar to saving evidence in a criminal case). Micrographs and SEM images of a break's origin, using fracture mechanics methods, will also provide detailed evidence. To correctly characterize the ~0.1% statistical breakage rate for thin wafers, thousands of wafers must be processed to prove with 90% confidence that this rate is achieved. Overall, data collection will take time, so months of start-up effort should be anticipated to bring a new ultra-thin process line to target yield levels.

The corollary is that you should beware of wafer-breakage data from just a few wafers that show a wafer-thinning process stream as robust enough to produce high yields. With special care, most processing tools can be made to process a few thin wafers with no breakage. But when several tools are linked together, not only do the processes interact (i.e., upstream stresses cause more downstream breaks), but also the handling of fragile, ultra-thin wafers between process steps can limit yield unless special care is given to integration-handling issues.

### Integration options

Typical process steps used today to thin wafers include: applying device-protecting backgrind tape to a wafer's front side; backgrinding to near the final thickness; removing the tape plus an adhesive clean; and removing surface and subsurface grind damage to the final thickness. This is followed by conventional mounting to a tape frame and sawing. So far, there is no consensus on whether a closely integrated set of some or all of the above processes is superior to flexible integration (a term recommended by Tru-Si Technologies in 1999).

With a closely integrated process (i.e., either several process steps combined within one tool or multiple tools "bolted" together, such as from TSK), the integration tool supplier has the burden of solving automated handling between steps. Further, throughput is limited by the slowest process step in the tool.



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Figure 3. Scanning electron microscope (SEM) images of a silicon surface a) after grinding and b) after grinding and etching to remove surface and subsurface damage.

With flexible integration, each process tool is "stand-alone." Wafers are buffered between process steps to balance throughput. In addition, parallel processing with multiple copies of slower tools can optimize throughput.

**Future challenges**

The introduction of special processes to create ultra-thin wafers will likely introduce challenges other than handling. These could include problems with electrostatic discharge, contamination, corrosion, galvanic actions, cleaning difficulties, waste disposal, gas stream scrubbing, dicing, difficulty placing wafers on tape frames, and handling of ultra-thin die.

Consider, for example, conventional dicing operations in semiconductor assembly. Transferring and holding an ultra-thin wafer onto adhesive tape is not a trivial exercise. The Takatori system for mounting onto tape frames with wafers from a pod is one commercial solution available. Such mounting requires special robotic end effectors to facilitate pick-and-place from various pods and to enable the precise placement of thin wafers onto the tape.

Most existing semiconductor industry standards did not anticipate manufacturing thin die <200µm thick. Semiconductor Equipment and Materials International (Semi) recently held exploratory sessions to gather a consensus on the need for special thin or ultra-thin wafer standards for material handling.

Many official Semi and de facto material-handling standards are in use for all common wafer sizes up to 200mm. The best example is the 25-slot cassette. This cassette, however, was designed for full-thickness wafers, and it will not handle ultra-thin wafers safely. Further, many handling techniques, such as edge gripping or pushing wafers against a stop to definitively locate them, are not recommended for ultra-thin wafers. Accordingly, Semi is addressing the growing recognition that no adequate standards exist for handling thin or ultra-thin wafers, with an ongoing list of meetings at Semicon exhibitions and other focus groups [5].

A segment of the semiconductor industry is paying increasing attention to special needs for the production of thin device wafers. In addition to Semi meetings, several technical meetings have been held and more are envisioned to address the problems of reliable production of thin wafers and die.

**Acknowledgments**

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Wafer thickness (µm)	Feasibility unknown		Capability foreseen '04		Developing capability '03			'02 production capability		
	0	25	50	75	100	125	150	175	200	225
Die handling					Standard die pick-and-place methods					
Dicing					Advanced thin die handling Special low-aspect-ratio dicing					
Placement on tape frame						Standard die separation				
SSD removal <1µm					Manual placement Automated placement on tape frame					
Bulk Si removal						Dry (plasma) etching Wet (chemical) etching Polishing (CMP or dry)				
Etching (wet or dry)						Etching (wet or dry) Backgrinding with coarse + fine wheels				
Handling between steps					All steps integrated to eliminate handoffs Flexible integration with robotic automation					
Backgrind method						Tapeless backgrinding Advanced grind tools Standard backgrinding tools				
Grind tape					No tape Enhanced-release tape Standard backgrind tape					
Rigid wafer carrier					Alumina, polymer, or tape, etc.					
End effector					No-touch Bernoulli type Vacuum type end effector					
Storage or shipping					Separated die on tape frame Whole wafers in pods Whole wafers in cassettes					

Table 2. Probable handling processes for a range of wafer thicknesses

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