

RICH LVL-1 Trigger Study

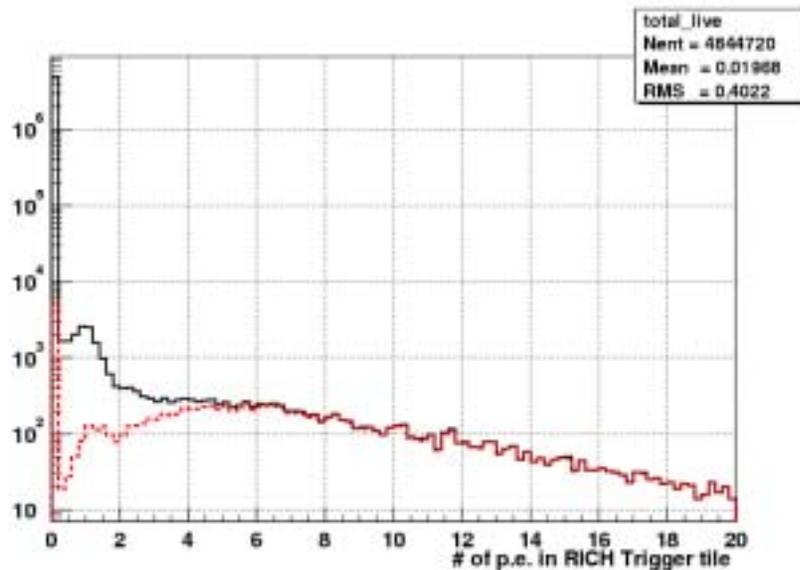
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Score board for RICH LVL-1 in Year-2 proton run (Over 50 point is success each)

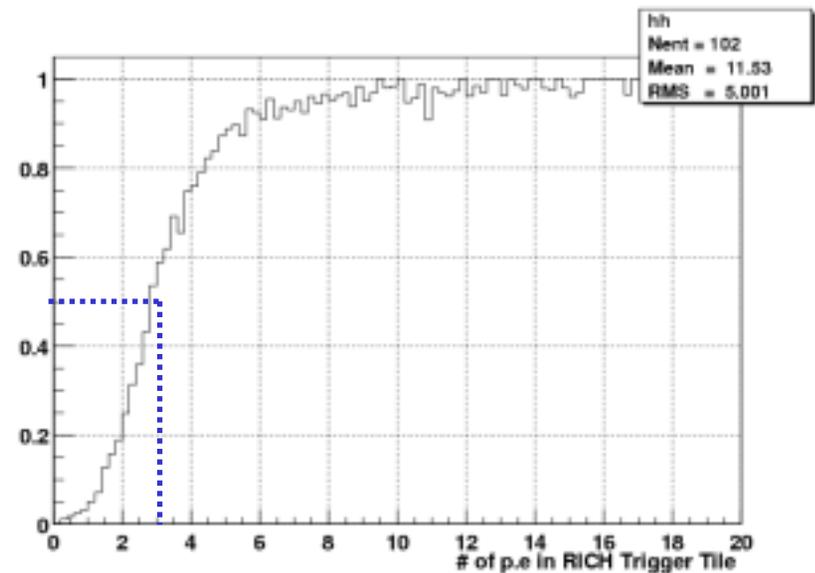
- **16 RICH LVL1 Modules were installed : 100 Point!**
 - Modules were tested in Japan
 - But the test using real RICH FEE in BNL couldn't performed in this time
- **Configurations for RICH LVL1 Modules were tuned: 70 Point!**
 - ADC Timing and threshold
- **Got following performance at last: 25 Point....**
 - Working Tile : 38 tile (14.8%)
 - Hot Tiles (Trigger bits are high too frequently) : 74 tile (28.9%)
 - Dead (No trigger signal at all) : 144 tile (56.3%)
- **Started to investigate the problems: 40 Point!**
 - One of the problem is the bad Int_R chip which produce the LVL1 trigger sum signals?
 - Also, several bias voltages of AMU/ADC Board are investigated

Performance for good channels

- **Photo-electron distribution in a RICH trigger tile**
 - Accumulate good channels
 - Black : Total p.e. distribution
 - **Red** : require the trigger bits



- **Efficiency curve**
 - **Red** / Black in left figure
 - Efficiency \sim 50% @ 3 p.e
 - Need to set lower threshold?



Updated Status of Progress

- Shooting Hot and Dead tiles: Reaching to the End!
 - No correlation was found with oscillation problem
 - Chips used in the experiment have been passed once before and Now too!
 - A part of them are tested again recently, and are found correctly working.
 - It was same both for Hot and Dead tiles.
 - Hot tiles (29%) had close correlation with miss-resetting analog trigger signals from Int-R Chips
 - Signal must be reset every B.C, but corresponding channels were not.
 - Critical voltage of ECL Bias was the reason of miss-reset of trigger signal.
 - The ECL Bias voltage on Chip test board and AMU/ADC were different.
 - After adjusting ECL bias on AMU/ADC modules, the noise has gone!
 - ECL bias adjustable by replacing some resistors
 - Dead tiles (56%) are still investigated
 - No current sum signal is seen for several corresponding channels (at BNL).
 - Reason may also exist on some of the bias voltages.

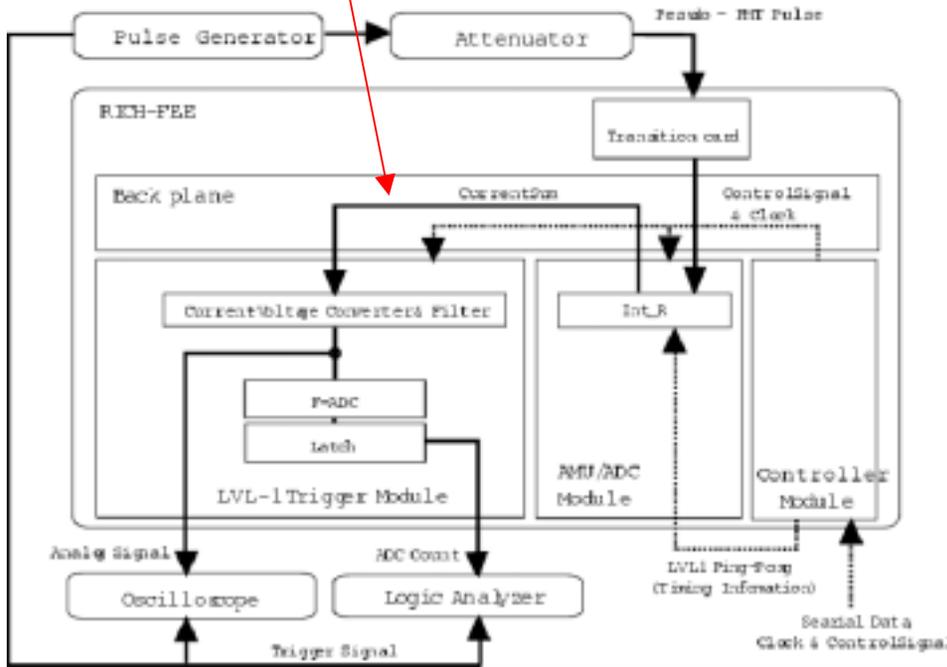
Plan for Year-3

- Work advanced in very good time manner
 - Work planned by the end of April are almost achieved
 - Shoot Hot tile, and Started Chip test for the case of breakage.
- Between May and September
 - Figure out the reason of the LVL-1 “Dead tile” problem.
 - Replace the resistors for ECL Bias on the AMU/ADC modules, and the module will again be tested with LVL1 Module.
 - Check all the trigger sum outputs
 - Perform the complete chain test from input of the AMU/ADC Module through output of the LVL1 Module (That was not done by last year)
 - Selecting spare “good chip” for further runs.
 - Ship two crates each to Japan and receive another two crates from Japan.
- By the end of September
 - Ship all the crates/modules back to BNL

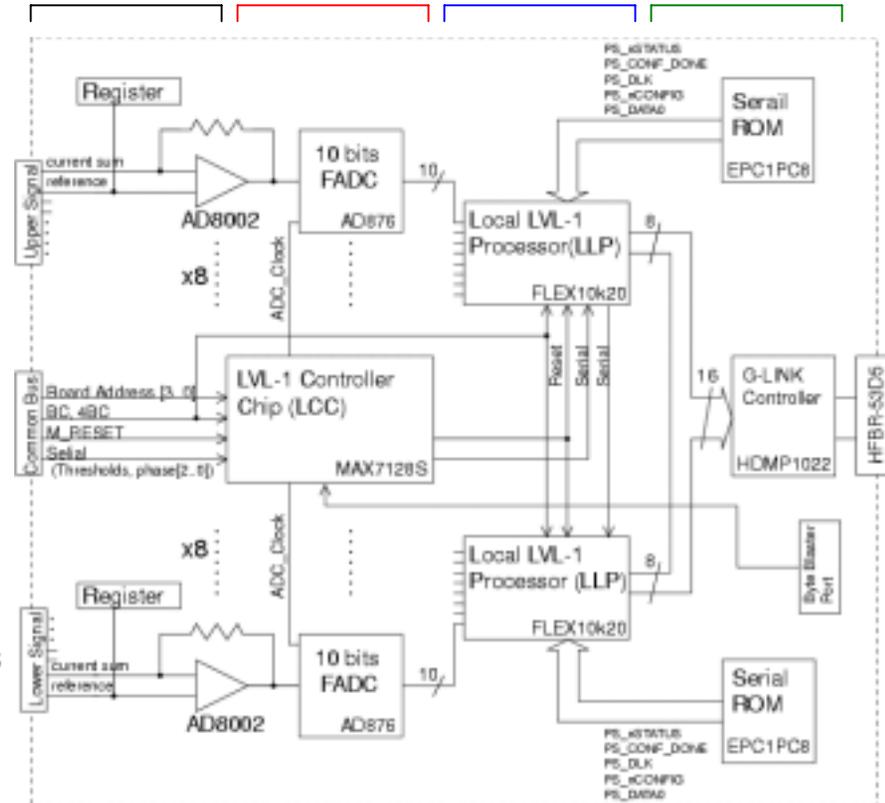
Other Figures

Block diagrams

Here is the problem?



Current to voltage **AD conversion** **Threshold** **output**



- RICH FEE**

- This is the block diagram used for the test in Japan
- Int_R chips on AMU/ADC Module

- RICH LVL1 Module**

- Functions after “AD conversion” works well even in bad channel