

# RICH Trigger performance

- Summary of the RICH LVL1 for last proton run
- Performance of good channels
- Possible problem of bad channels
- Block diagrams – where we have problem?
- Plans for next run

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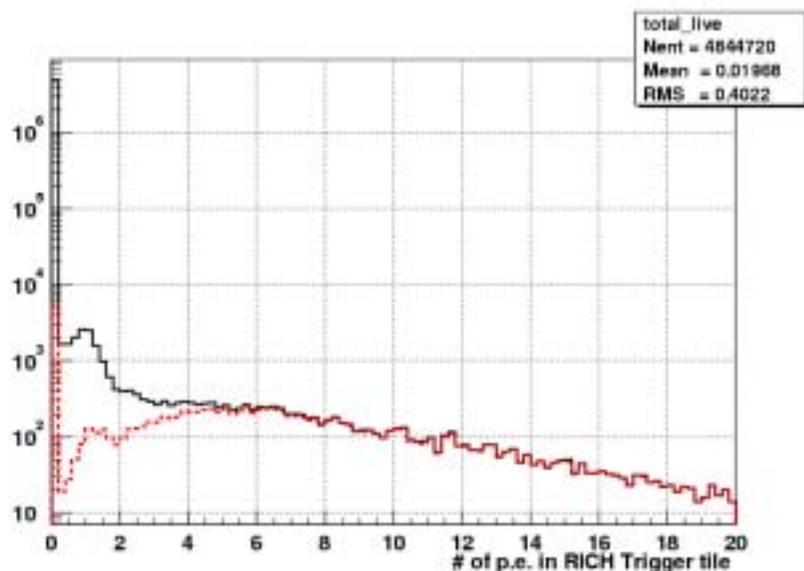
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# Summary of RICH LVL1 for the last proton run

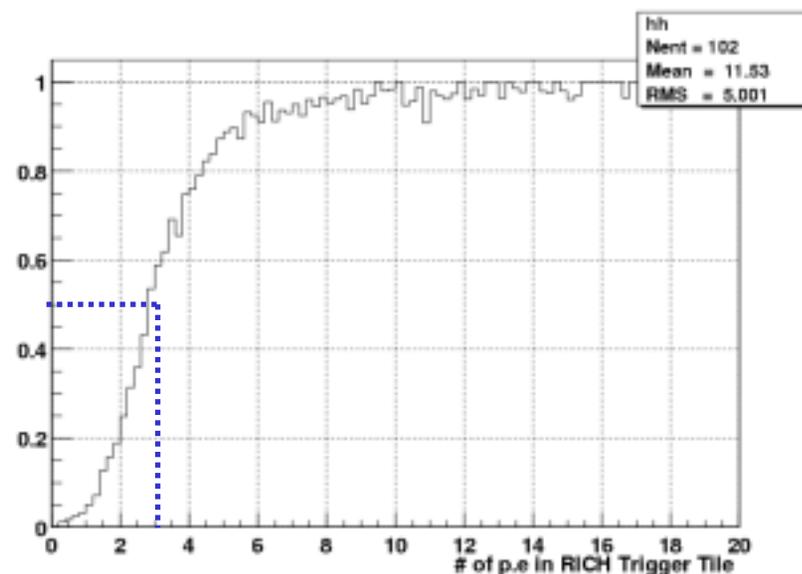
- **16 RICH LVL1 Modules were installed**
  - Modules were tested in Japan
  - But the test using real RICH FEE in BNL couldn't performed in this time
- **Configurations for RICH LVL1 Modules were tuned**
  - ADC Timing and threshold
- **Got following performance at last**
  - Working Tile : 38 tile (14.8%)
  - Masked (noisy) : 74 tile (28.9%)
  - Dead (no signal) : 144 tile (56.3%)
- **We started to investigate the problems**
  - One of the problem is the bad Int\_R chip which produce the LVL1 trigger sum signals

# Performance for good channels

- **Photo-electron distribution in a RICH trigger tile**
  - Accumulate good channels
  - Black : Total p.e. distribution
  - **Red** : require the trigger bits



- **Efficiency curve**
  - **Red** / Black in left figure
  - Efficiency ~ 50% @ 3 p.e
  - Need to set lower threshold?



# Possible problem for bad channels

- **Dead channels**

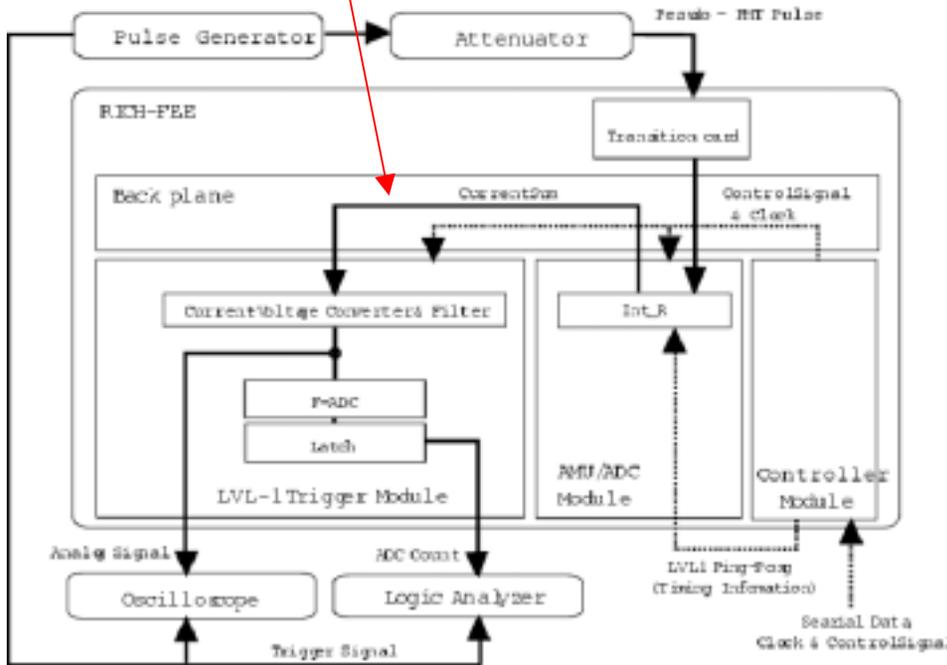
- Int\_R Chip produce the LVL1 trigger sum signal
- We checked some of dead channels after the run and found that Int\_R chip does not output the signal

- **Noisy channels**

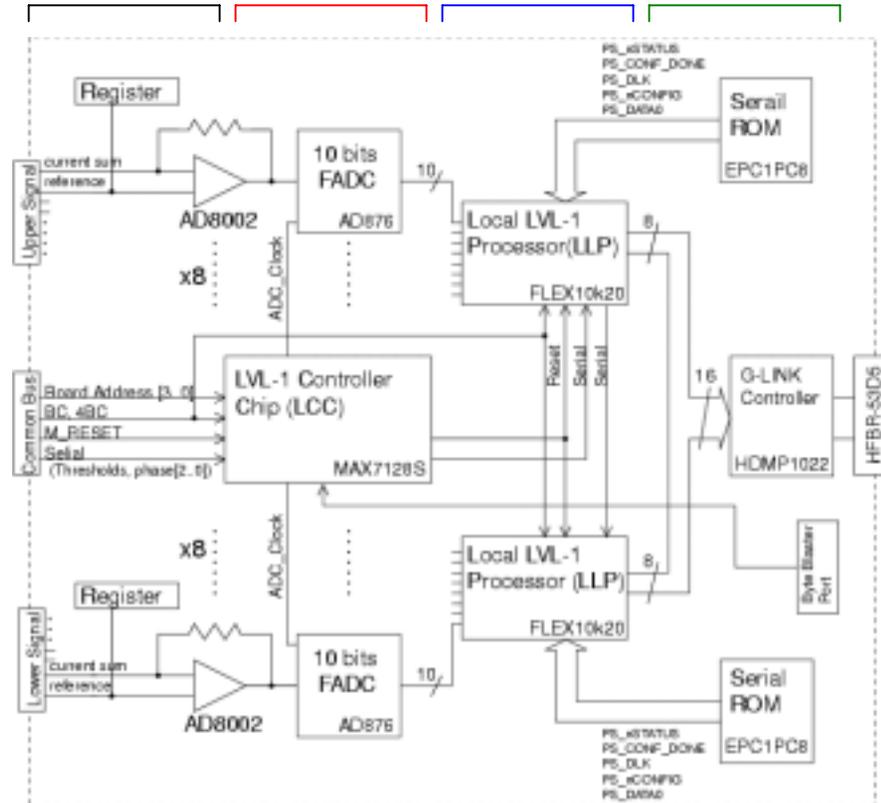
- Oscillation problem
  - Which happens only in BNL so far
  - We would like to reproduce the situation in Japan to debug
- Temporary solution was reconfiguration of Int\_R chip
- We couldn't understand the origin yet

# Block diagrams

Here is the problem?



Current to voltage    **AD conversion**    **Threshold**    **output**



- **RICH FEE**

- This is the block diagram used for the test in Japan
- Int\_R chips on AMU/ADC Module

- **RICH LVL1 Module**

- Functions after “AD conversion” works well even in bad channel

# Plan for next run

- **We are planning to ship RICH FEE crate to Japan on March**
  - Test LVL1 Trigger Sum output of all Int\_R chip
  - Replace them to good one if the chip doesn't output the correct signal
  - Perform the complete chain test from input of the AMU/ADC Module through output of the LVL1 Module