

PHENIX TEC - FLASH ADC

INTRODUCTION

A custom analog-to-digital converter (ADC) has been designed for the Front End Electronics (FEE) chain of the PHENIX Time Expansion Chamber (TEC) at RHIC. The chip consists of two individual flash ADCs having a common digital encoder that produces a single 5-bit output (fig.1). This unusual architecture is chosen because signals from the TEC are divided into two ranges of interest:

- 1) dE/dX range – low level signals due to ionization tracks produced as charged particles lose energy within the detector volume.
- 2) TR range – high level signals due to ionization *globs* produced when transition radiation (TR) photons are absorbed within the detector volume.

As shown in fig. 1, the ADC requires a Preamp/Shaper circuit with two outputs. The high gain output (x5) drives the dE/dX input of the ADC while the low gain output (x1) drives the TR input of the ADC. In this way, signal ranges are set to match the dynamic ranges of the ADC inputs. Optimum resolution is, therefore, maintained over a large dynamic range without the need for many high precision comparators. In addition, the ADC for the dE/dX input is nonlinear, further increasing dynamic range.

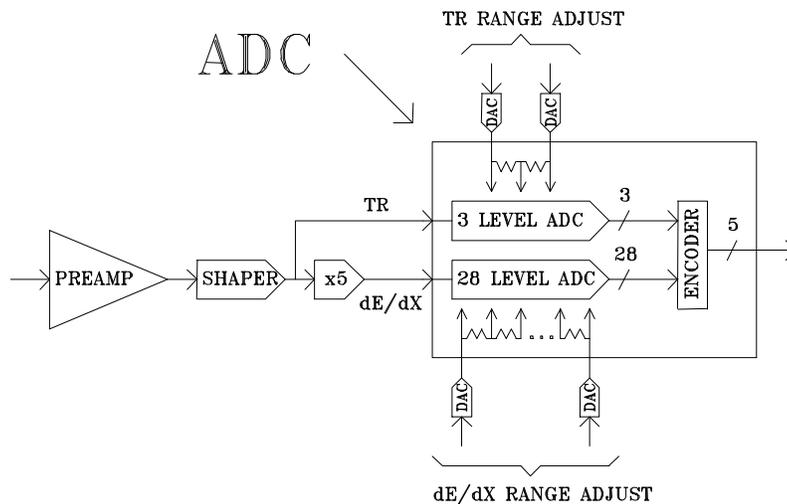


FIG. 1 Optimum resolution is maintained over a large dynamic range without the need for many high precision comparators by using two internal ADCs to cover two signal ranges (dE/dX and TR). The final FADC output word is formed by encoding the results from both internal ADCs.

FEATURES

- Two Internal ADCs

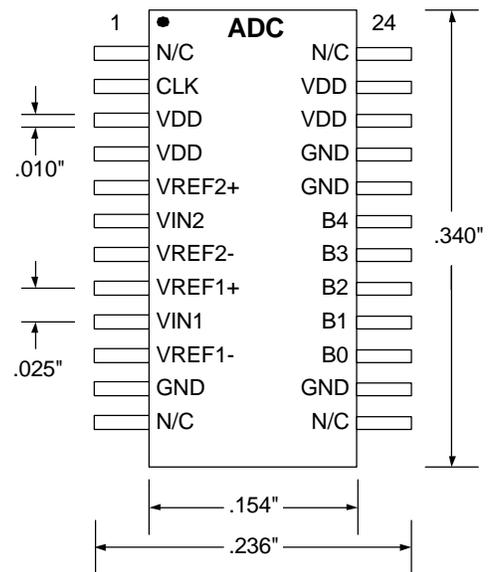
1.) dE/dX ADC

Output Codes	Input Voltage Range (adjustable)	Corresponding Detector Charge Range (example)
1-10	40 - 400 mV	2 - 20 fC
11-28	480 - 1840 mV	24 - 92 fC

2.) TR ADC

Output Codes	Input Voltage Range (adjustable)	Corresponding Detector Charge Range (example)
29 - 31	800 - 1600 mV	200 -400 fC

- 5-bit output (both ADCs combined)
- 40 Ms/s sample rate
- 20 MHz input bandwidth
- 0 - 2V input range
- +/- 10 mV accuracy
- Integral Nonlinearity (INL)
 - +/- 1/ 8 LSB max
 - +/- 1/32 LSB typical (rms)
- Differential Nonlinearity (DNL)
 - +/- 1/16 LSB max
 - +/- 1/64 LSB typical (rms)
- +5V supply voltage
- 27 mA supply current
- 150 mW power dissipation
- 0 - 80°C operating range (ambient)
- 1.2u CMOS process (ORBIT)
- 1.6 x 2.0 mm die size
- 24 pin SSOP package



PIN DESCRIPTIONS

INPUTS

- (9) VIN1: Signal input for the dE/dX ADC (0 - 2V)
- (6) VIN2: Signal input for the TR ADC (0-2V)
 - * The signal sources driving these inputs should each have an impedance of 100 ohms or less to maintain high frequency operation.
- (2) CLK: Clock input (5V CMOS, 50% duty cycle)

OUTPUTS

- (15-19) B0-B4 Five bit binary coded output (B0=LSB, B4=MSB). Codes 1-31 correspond to comparator thresholds 1-31. Outputs will drive 30 pF loads to 5V CMOS logic levels in less than 5 ns. Output impedance is 75 ohms, thus minimizing transmission line effects.

REFERENCE PINS

Each internal ADC contains a resistor chain that generates the voltage levels at which corresponding comparators switch (fig.1). Both ends of the chains are brought out to pins so that their endpoint voltages may be adjusted by external sources such as programmable digital-to-analog converters (DACs). This permits the user to set the transfer function of each ADC. Tables in the previous section give typical examples.

- (8) VREF1+ Positive end of the resistor chain for the dE/dX ADC
- (10)VREF1- Negative end of the resistor chain for the dE/dX ADC.
- (5) VREF2+ same as VREF1+ for the TR ADC.
- (7) VREF2- same as VREF1- for the TR ADC.

Each reference pin must be driven by a low impedance source in order to minimize the loading effects of the ADC resistor chains. Therefore, a buffer amplifier should be placed between each pin and the DAC that drives it. The dE/dX resistor chain is 200 ohms and the TR resistor chain is 770 ohms. Therefore, to reduce the loading effect to less than 1%, the VREF1 pins should be driven by a buffer amplifier with an output impedance of 2 ohms or less and the VREF2 pins should be driven by a buffer amplifier with an output impedance of 7.7 ohms or less. Many ADCs may be driven by a single buffer providing that the impedance and current characteristics of that buffer are adequate. In addition, bypass capacitors should be placed as close to the reference pins as possible (.01-.1 uF chip types).

GND

- (11,14,20,21) All ground pins should be soldered directly to a common ground plane.

SUPPLY

- (3,4,22,23) +5V (+/- .25V). Bypass the supply pins to a ground plane with .01- .1 uF chip capacitors.

NO CONNECTION

- (1,12,13,24)

TIMING (simplified)

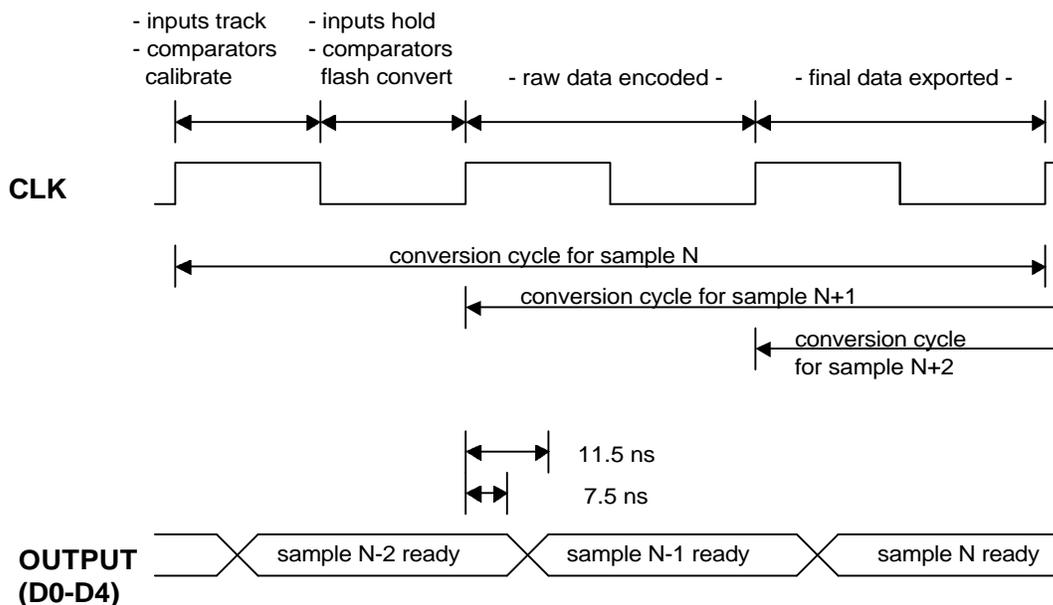


Fig. 2 Basic ADC operation is illustrated in the timing diagram above. During the first half of each clock period, input signals are tracked while internal comparators are calibrated. During the second half of each clock period, input signal voltages are held on internal capacitors and applied to a bank of comparators. Flash conversion occurs during this time and raw digital data is latched at the end of the period. The ADC is immediately ready to start a new conversion cycle. The conversion rate is, therefore, equal to the clock rate. While the second conversion cycle occurs, raw data from the first cycle is encoded into a binary format. During the third conversion cycle, final data corresponding to the first conversion cycle is applied to the output pins of the chip. As shown, output data is valid 11.5ns after the rising edge of the clock and remains valid until 7.5ns after the rising edge of the next clock. There is a short period between conversions (~ 4ns) where data is changing and is unavailable for export. The pipelined architecture of this ADC permits high speed operation at the expense of a latency time of slightly more than 1 clock period.

MEASURED CHARACTERISTICS

Ten prototype chips were fabricated, packaged, and tested. One of the chips was nonfunctional while the remaining nine had nearly identical performance characteristics that met the design goals listed in the 'FEATURES' section. Test results obtained from one of these chips are presented here and are typical of the lot.

LOT ID: adcx1_5bit_10_2_95 (Orbit Semiconductor Inc.)
 DICE RECEIVED: 4/3/96 (Orbit Semiconductor Inc.)
 DICE PACKAGED: 4/10/96 (Emanuel Equipment Corp.)
 PARTS TESTED: 4/12/96 - 6/12/96 (Brookhaven National Laboratory)

TESTING CONDITIONS

- TEMP 20°C
- VDD 5V
- VREF1+ 1.840V
- VREF1- 0.040V
- VREF2+ 1.800V
- VREF2- 0.500V
- CLK 40 MHz square wave (CMOS logic levels)
- VIN1, VIN2 Connected to signal sources through 4' of 50 ohm coaxial cable. Source impedance is 100 ohms.
- B0 - B4 Connected to data acquisition system.

TRANSFER FUNCTIONS

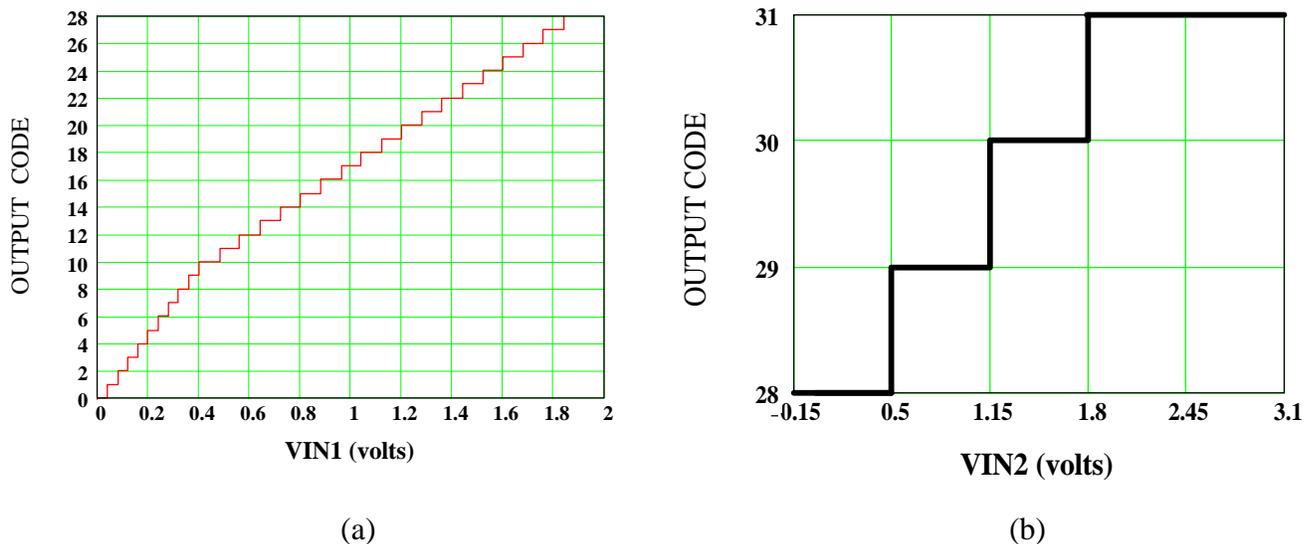


Fig 3. Graph (a) shows the transfer function of the ADC with respect to the dE/dX input (VIN1). The digital output is plotted against input voltage and is seen to have two linear segments. The first segment extends from code 0 to code 10 and has a slope of 1 LSB per 40 mV. The second segment extends from code 10 to code 28 and has a slope of 1 LSB per 80 mV. Resolution is highest for small signals because this is the region where the best discrimination between electrons and pions is realized. Graph (b) shows the transfer function of the ADC with respect to the TR input (VIN2). In a typical application, $VIN2 = 1/5 VIN1$, and only large input signals are capable of generating the codes 29-31. These large signals are expected to be produced by TR photons. The slope in this graph is 1 LSB per 650 mV.

INTEGRAL NONLINEARITY (INL)

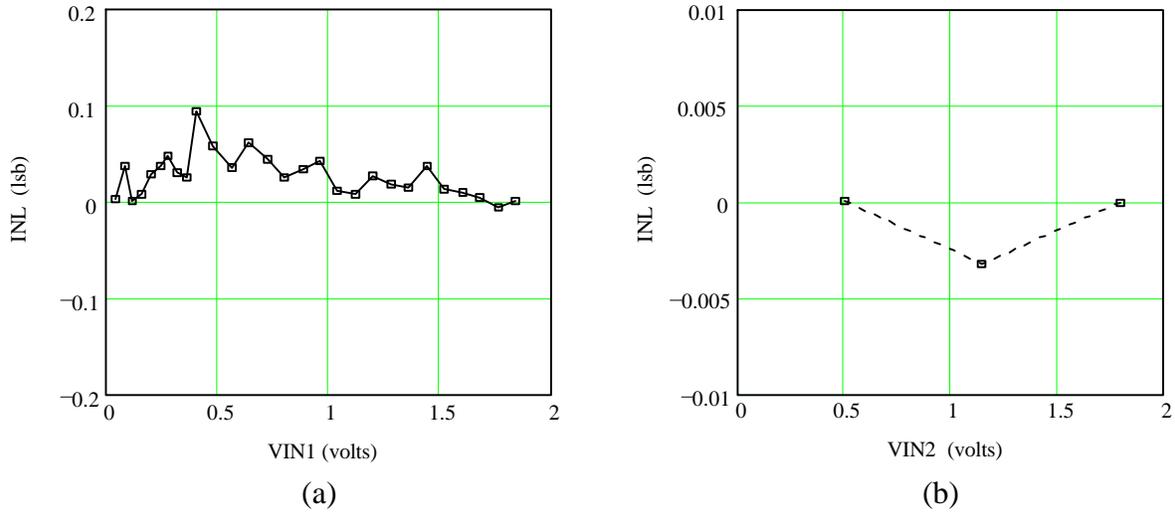


Fig. 4. Integral nonlinearity (INL) is plotted as a function of input voltage and is expressed in least significant bits (LSB). Graph (a) depicts INL with respect to the dE/dX input (VIN1) and graph (b) depicts INL with respect to the TR input (VIN2). For codes 1-28 (graph a), INL is typically +0.03 LSB with a peak value of 0.1 LSB at code 10. This peak occurs because the transfer function changes abruptly at this point. For codes 29-31 (graph b), INL is negligible. Note that both INL functions are zero at their end points. This is achieved by fine adjustment of the voltages at the reference pins of the resistor ladders (VREF1+, VREF1-, VREF2+, VREF2-).

DIFFERENTIAL NONLINEARITY (DNL)

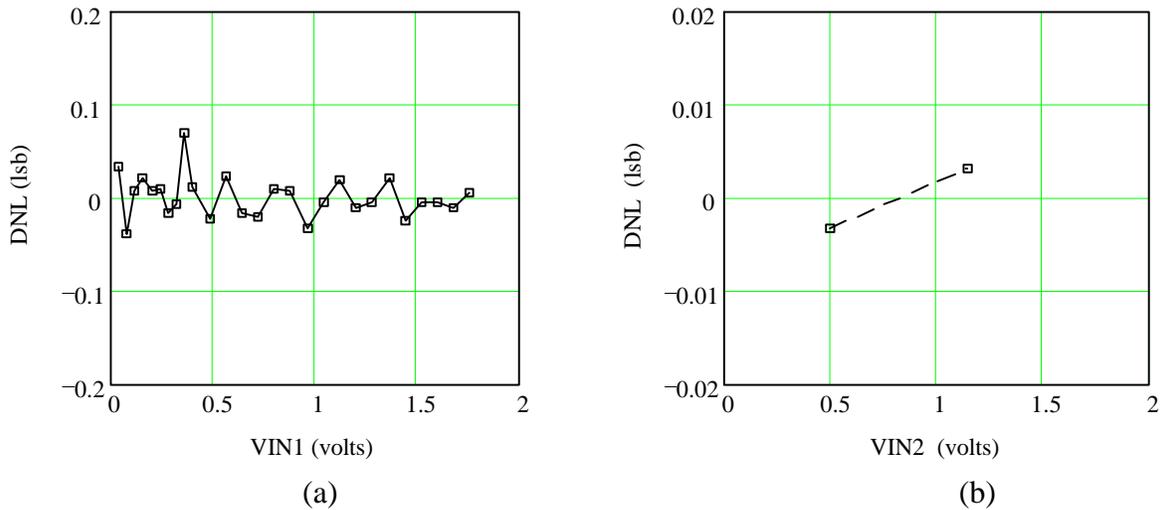
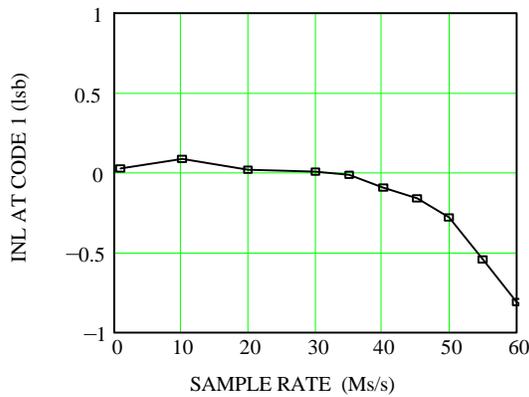
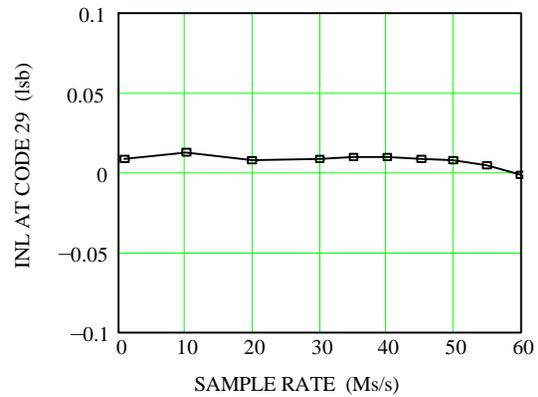


Fig. 5. Differential nonlinearity (DNL) is plotted as a function of input voltage and is expressed in least significant bits (LSB). Graph (a) depicts DNL with respect to the dE/dX input (VIN1) and graph (b) depicts DNL with respect to the TR input (VIN2). For codes 1-28 (graph a), INL is typically ± 0.02 LSB with a peak value of +0.07 LSB at code 10. This peak occurs because the transfer function changes abruptly at this point. For codes 29-31 (graph b), DNL is negligible. In these graphs, the DNL function is defined at each data point to be the difference of a measured LSB from its ideal value.

SAMPLE RATE LIMITATIONS



(a) dE/dX ADC



(b) TR ADC

Fig. 6. INL for the internal dE/dX ADC is measured at code 1 for a range of sampling rates. This data is plotted in (a). For rates below 40 Ms/s, INL is small and relatively constant. As rates exceed 50 Ms/s, INL increases rapidly. This effect is due to timing limitations of the ADC circuitry. Operation of the ADC is, therefore, not recommended above 50 Ms/s. Graphs have been made for values of the INL function measured at various codes. The results are very similar and code 1 was chosen arbitrarily. INL for the internal TR ADC is measured at code 29 and is plotted in (b). While higher rate operation is possible with the internal TR ADC alone, overall operation is limited by the internal dE/dX ADC.

ANALOG BANDWIDTH

Fig. 7. -- GREATER THAN 50 MHz (Specific data to follow)

POWER DISSIPATION

Fig. 8. Power dissipation is plotted as a function of sample rate. The specified sample rate for this ADC in the TEC Detector System is 40 Ms/s. At this rate, power dissipation is approximately 150 mW.

