PHENIX Barrel Vertex Tracker (VTX)

Front End Electronics for the Strip Layers

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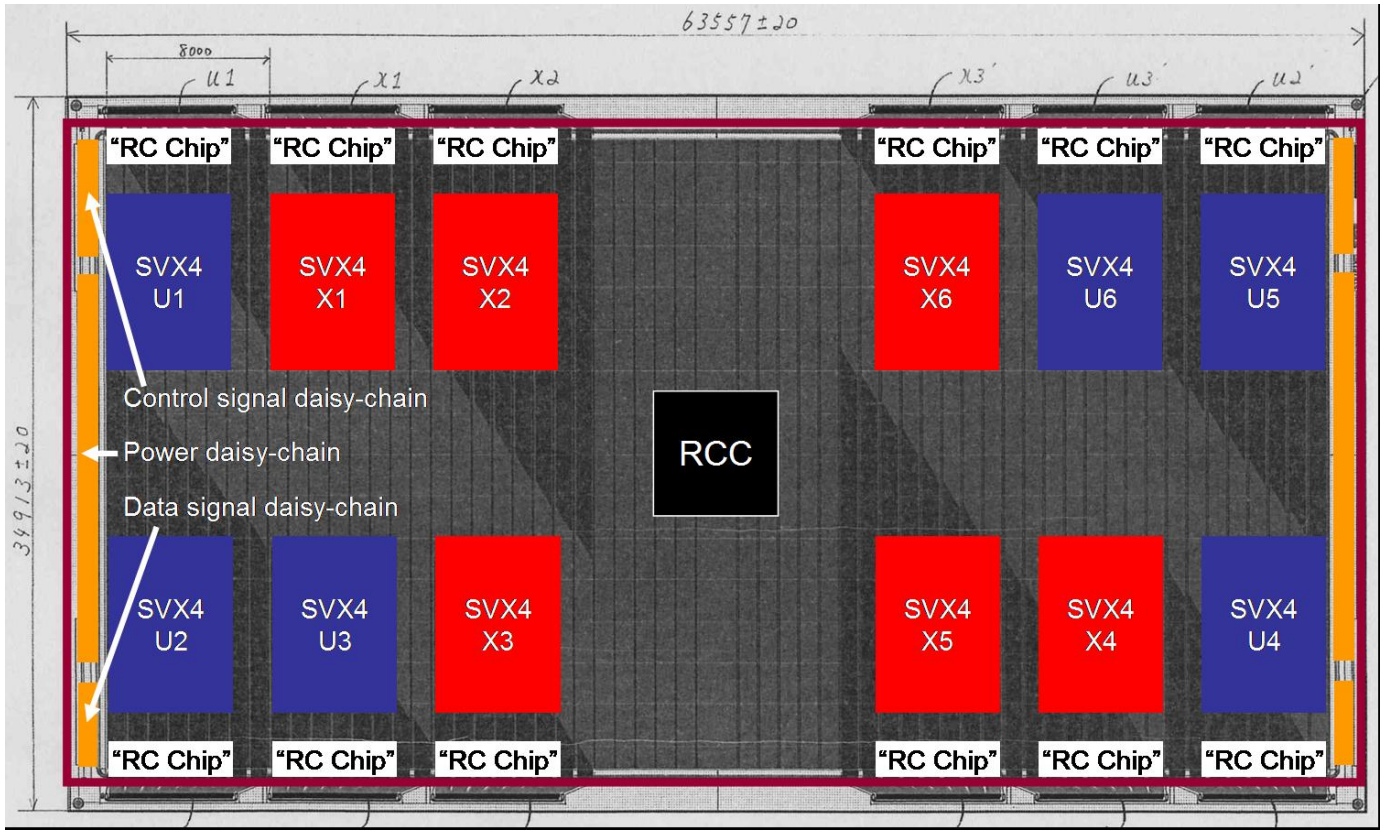
Project Readiness Review 01/19/2005

Outline

- System Overview
  - Readout Cards (ROCs)
  - Front End Modules (FEMs)
- Some Details
  - SVX4
  - ROC Control Chip (RCC)
  - Space/Trace Analysis
  - Thickness Considerations
  - Bandwidth Considerations
- Current R&D Status
- Cost & Schedule Determination

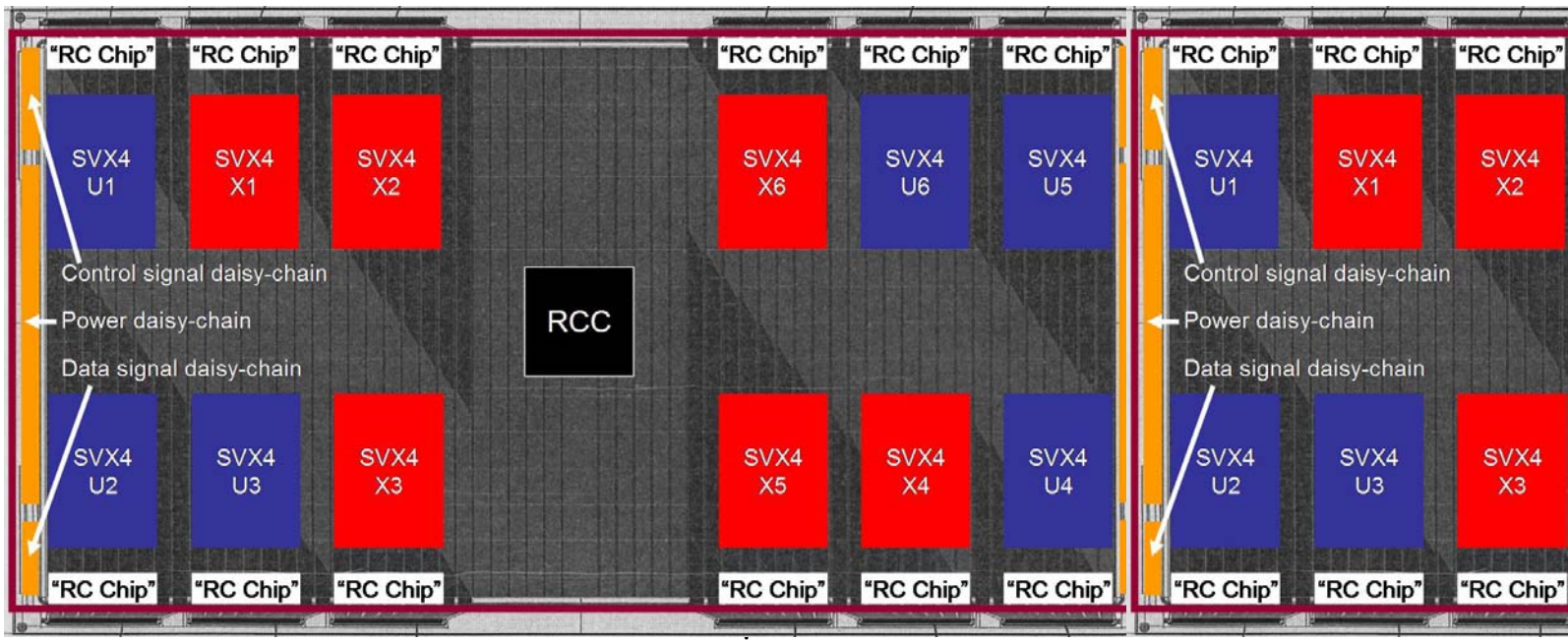
Readout Cards (ROCs)



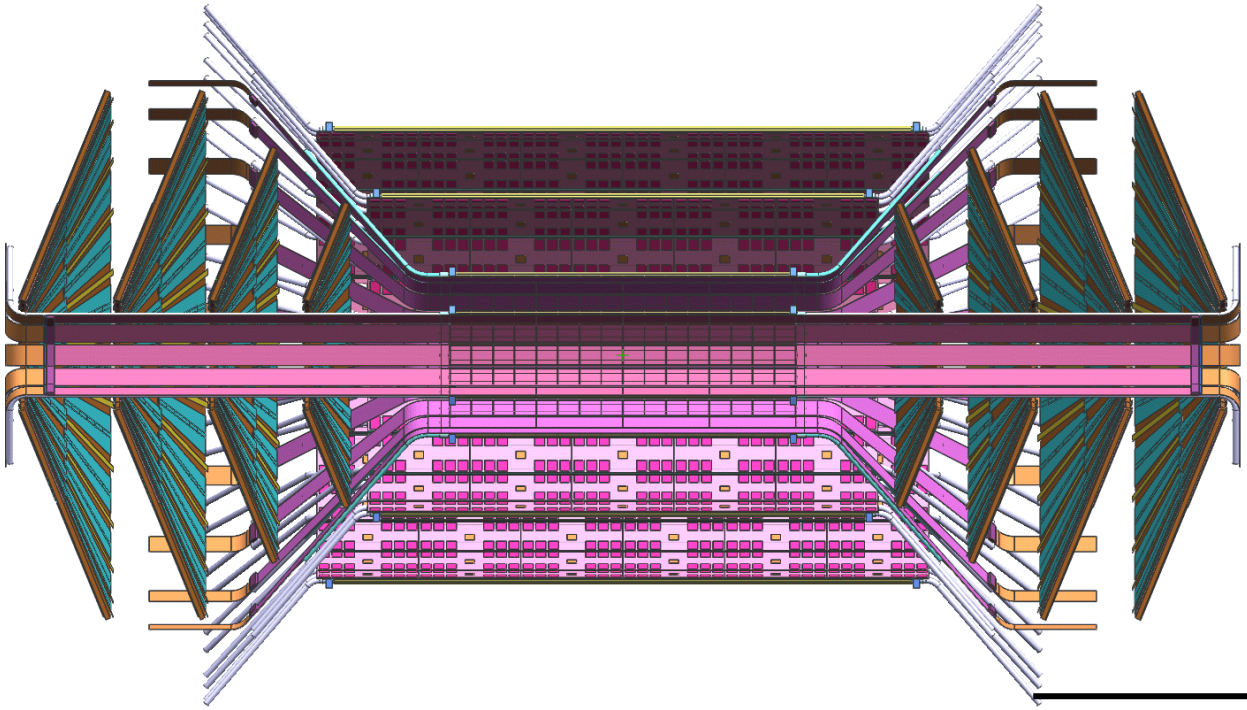
- Each 3x6cm sensor has 1536 channels, 1 ROC.
  - Implemented as a small aluminum/kapton flex cable.
  - Each requires 12 SVX4 chips and 1 ROC Control Chip (RCC, details later).

Ladders

- Signal traces and power layers (already inherent in ROC) connected at ROC edges to form one signal and power bus per ladder w/o extra material.
- 5 or 6 ROCs per ladder forms one detector azimuthal segment.

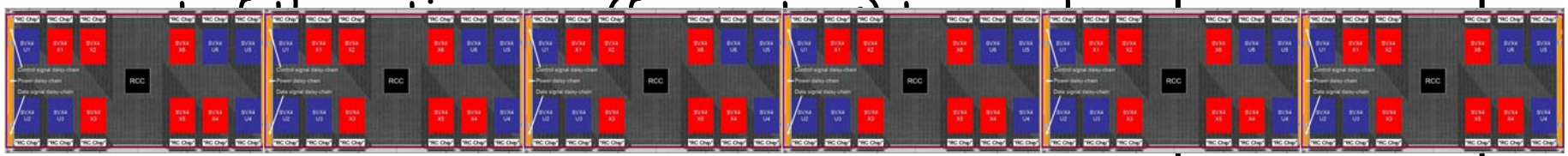


Front End Modules



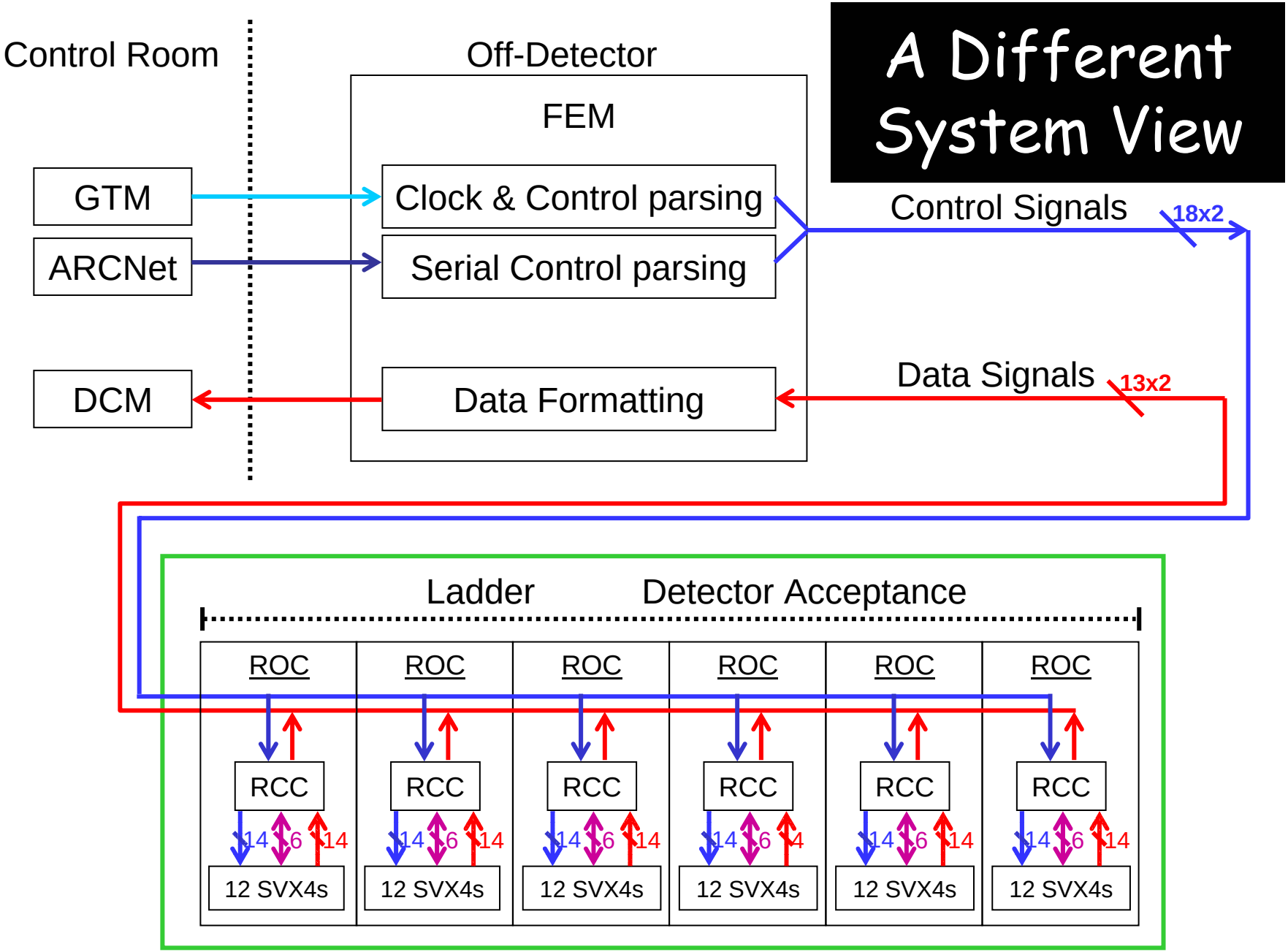
FEM Rack

- RCCs drive/receive LVDS signals across a bus



  - Clock and Fast Control.
  - Data Collection Modules.
  - Slow Controls.

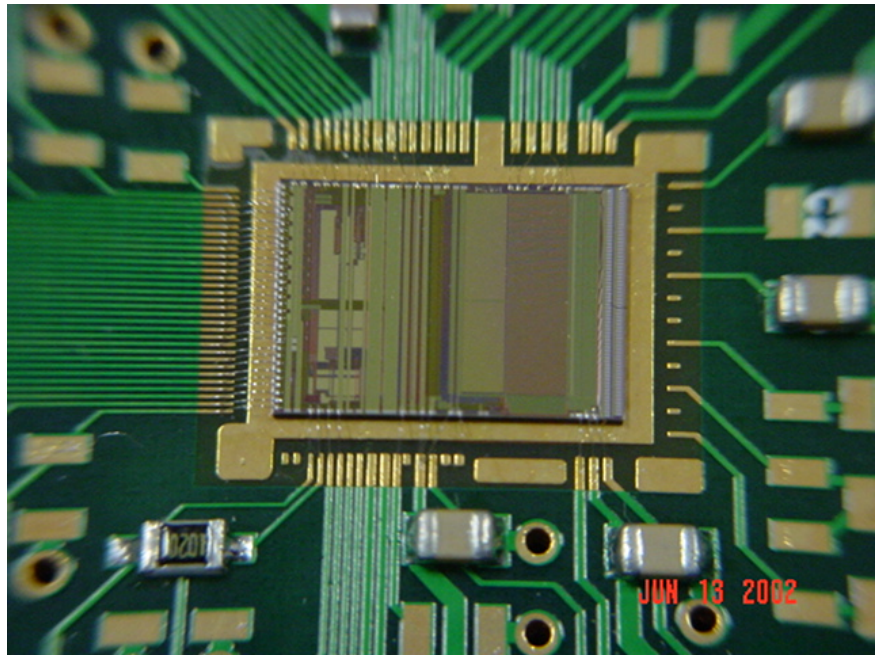
A Different System View



Some Numbers

Strip Layers	Layer 3	Layer 4	Sum
Ladders	18	26	44
Sensors/Ladder	5	6	
Sensors, ROCs, RCCs	90	156	246
SVX4s	1,080	1,872	2,952
Channels	138,240	239,616	377,856

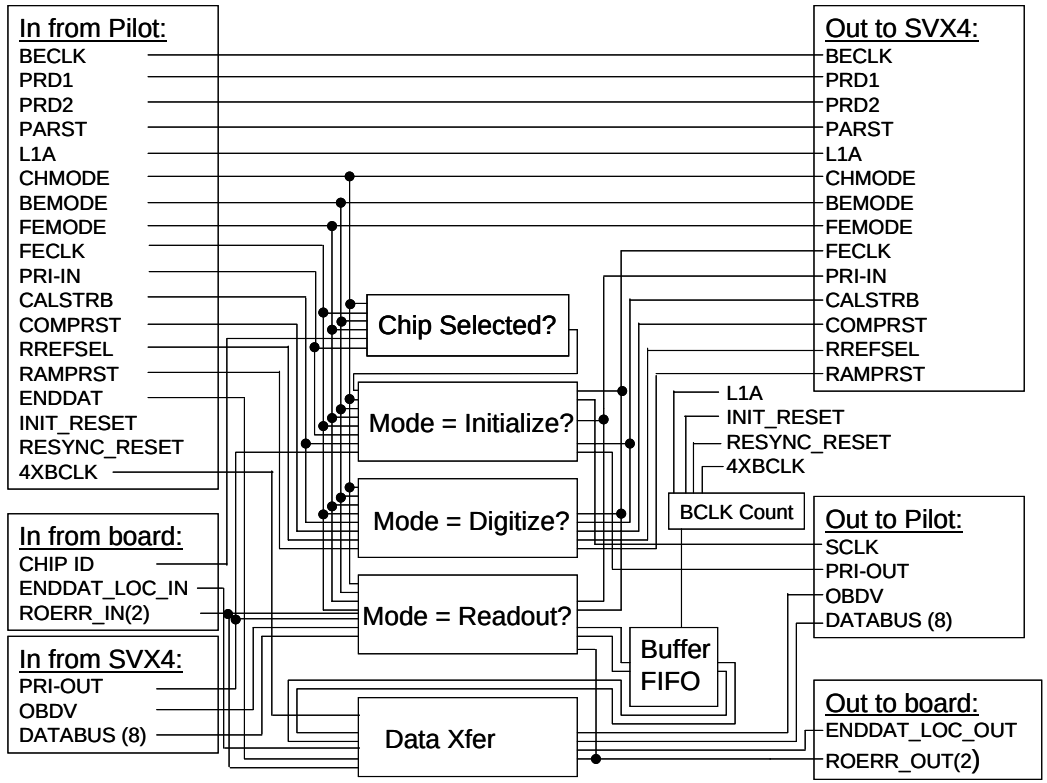
SVX4



- 128 channel chip.
- 5000 tested chips being purchased by RIKEN from FNAL.
- 0.25 μm TSMC process (inherently rad hard).
- Compatible with PHENIX DAQ:
  - Sufficient L1 latency (w/ analog pipeline).
  - Multi-event buffering (4 events).
  - Simultaneous digitization/readout and acquisition.
  - 106 ns RHIC clock sufficiently close to 132 ns Tevatron clock.
- Designed for $C_{detector}$ = 10-35pF:
  - Noise 0.22-0.25 fC
  - S/N 15-17 for 625μm sensors
- Power consumption ~ 3mW/channel.
- Designed for AC-coupled sensors:
  - Strip-pixel sensors are DC-coupled.
  - Dark current considerations strongly suggest using RC-chips (Hamamatsu) to provide AC coupling.
- Provide selectable on-chip 0-suppression w/ robust common-mode noise rejection:
  - Double correlated sampling (store difference between samples separated by ¾ of a clock cycle).
  - Write-amplifier pedestal subtraction.
  - Dynamical pedestal subtraction (if there's an offset present on a majority of channels due to common mode noise, this can be subtracted before 0-suppression).
- Latch-up probability greatly reduced (requires 200 mA) due to SVX4 epitaxial layer/low-resistance substrate fabrication process.

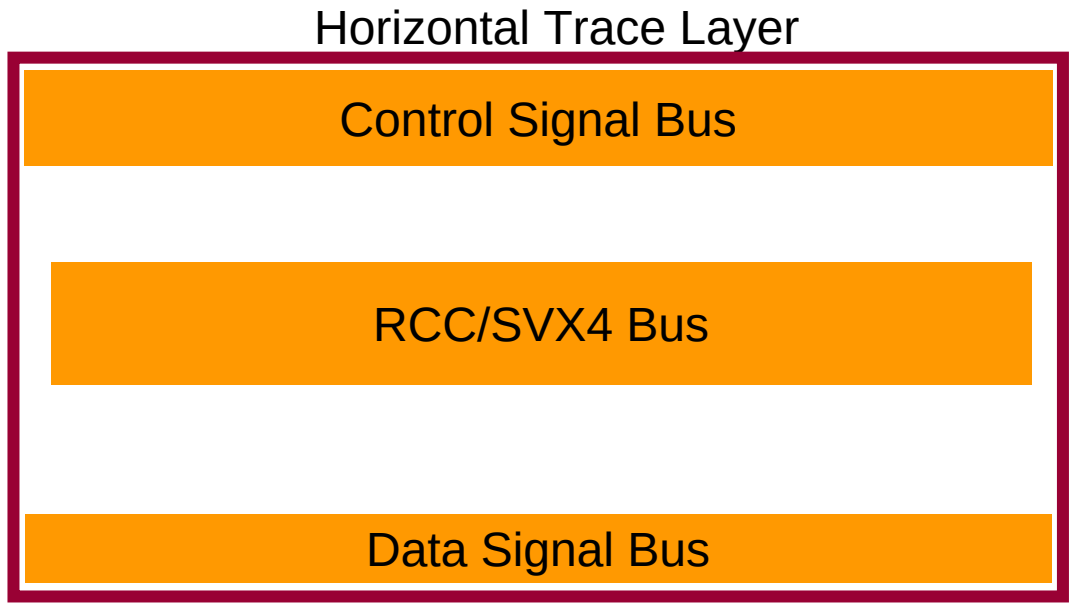
ROC Control Chips (RCCs)

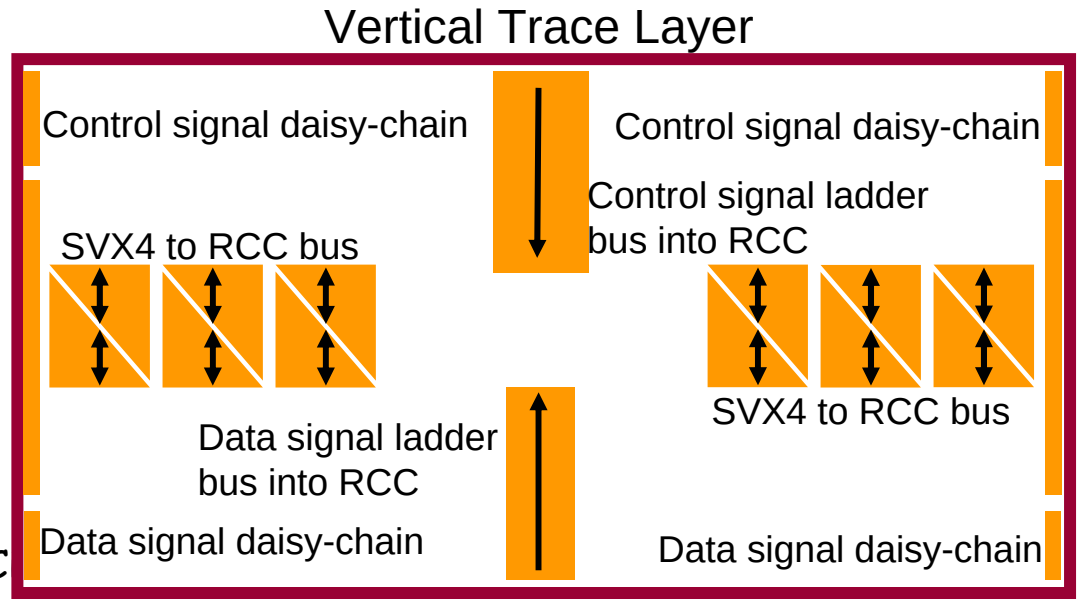
- RCC functionality:
  - State machine to direct serial control and data transfer.
  - Dual FIFO to allow simultaneous conversion (digitization + SVX4 readout) and data transfer to FEM, each in < 40 μsec.
  - Reduces # clock lines on bus.
  - Isolates effects of single-point failures.
  - Simplicity allows full FPGA prototyping, postponement of technology decision.
- ASIC vs. FPGA choice driven by:
  - Radiation tolerance.
  - Size, thickness.



Is There Room?

- ROC trace count almost entirely accounted for in connections from the RCC to/from the ladder bus and the SVX4s.
  - This number is reasonably well fixed by the SVX4.
- Figures to the right show a sketch of a possible trace layout to scale (100μm space/trace) showing that two trace layers is likely sufficient.
- Sufficient space also exists for edge connections.

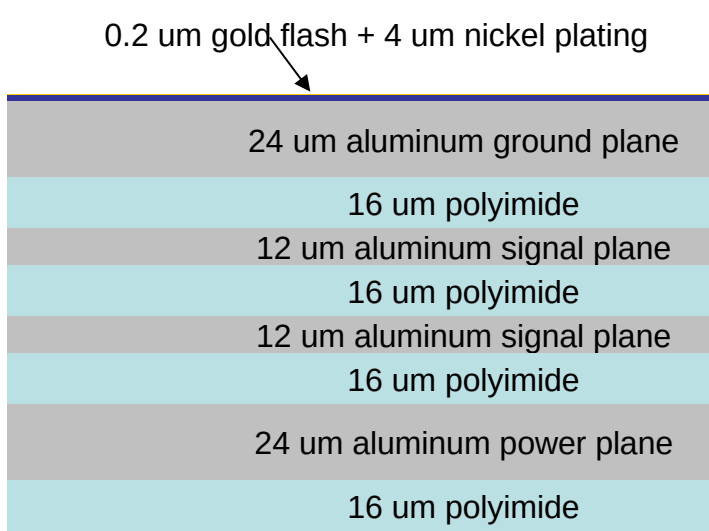




V. C

How Thick Is It?

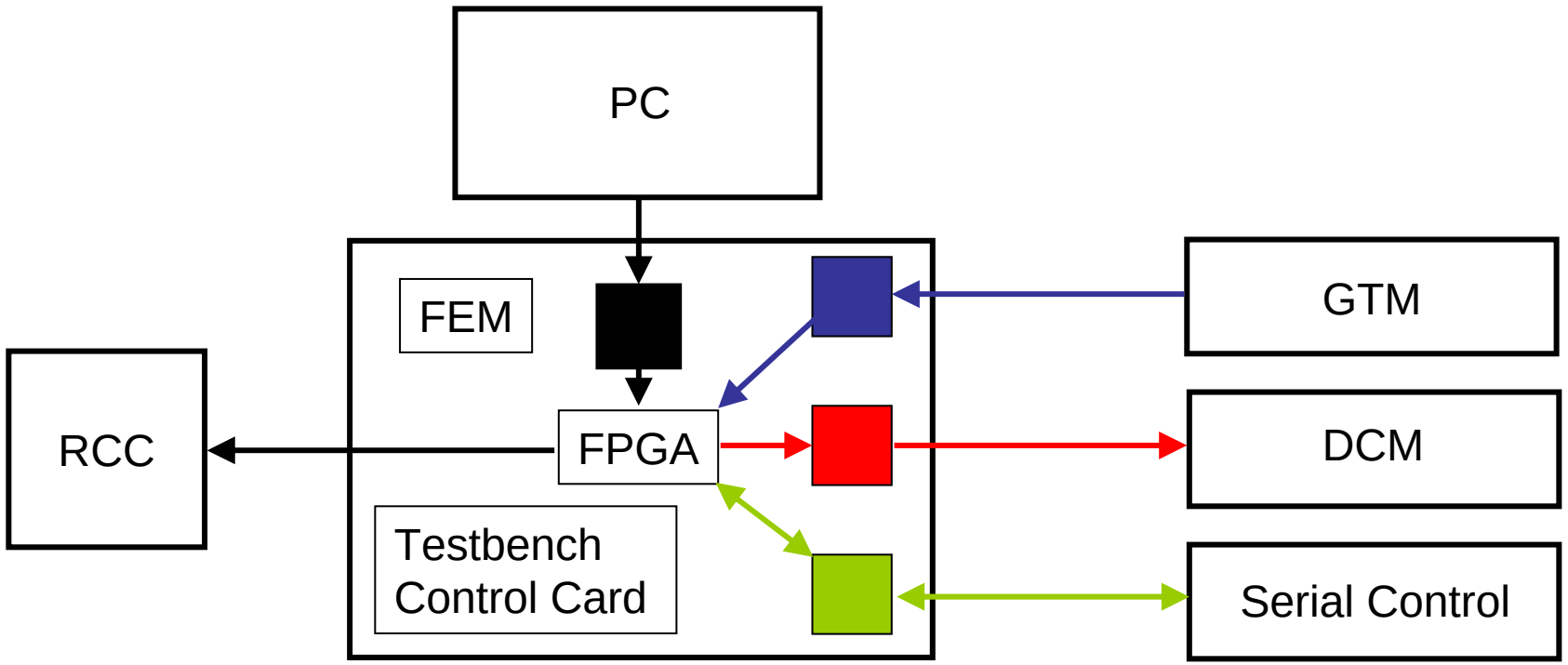
- Assumed bus structure shown at right.
- ATLAS-style (conductor/polyimide) ROC much thinner than CDF-style (BeO).
  - Crucial for PHENIX because ROCs cover entire area of strip layers.
- Material summary shown below.
- Reductions from proposal:
  - Eliminate substrate (small cards self-supporting).
  - Cu → Al (hope to capitalize on pixel-layer R&D).



Component	Material	X0 (mm)	Length (mm)	Width (mm)	Scale Factor	Height (um)	Qty	%X0
Ground/Power planes	Al	89	60	30	1	20.0	2	0.045
Capacitors, resistors, epoxy, wire-bond encapsulation	Estimate based on CDF hybrid							0.147
SVX4	Silicon	93.6	9.11	6.4	1	300.0	12	0.125
Throughhole plating	Al	89	60	30	0.6	13.0	2	0.018
Trace planes	Al	89	60	30	0.4	12.0	2	0.011
Polyimide		357.5	60	30	1	22.0	4	0.025
Adhesive		357.5	60	30	1	20.8	3	0.017
RCC	Silicon	93.6	7	7	1	300.0	1	0.009
Gold flash	Gold	3.35	60	30	0.5	0.4	1	0.006
Nickel plating	Nickel	14.7	60	30	0.5	2.0	1	0.007
Photoresist		357.5	60	30	0.5	20.0	1	0.003
Total								**0.411**

Front End Modules (FEMs)

- FEM serves as interface between RCC and the PHENIX DAQ (GTM, DCM, Serial Control).
  - Functionally similar to PHENIX FEMs developed at ORNL.
  - Different physical interfaces.
- Testbench designed to incorporate much of the required FPGA code but with USB/PC interface.



Data Format

Data Sent by RCC to FEM

Word Type	Bits 15-8	Bits 7-0	Note
0	1000, 4-bit RCC Address	0	Once per ROC
1	BCLK 15-8	BCLK 7-0	Once per ROC (value sampled on receipt of LVL1)
2	1001, 4-bit SVX4 Address	L1 Sample	Once per SVX4
3	0, 7-bit Channel Address	ADC	Potentially multiple values per SVX4
4	FF	FF	If this is missing there is a conversion error: a) PRI_OUT is high when ENDDAT_FEM arrives, b) Data exceeds RCC FIFO depth.

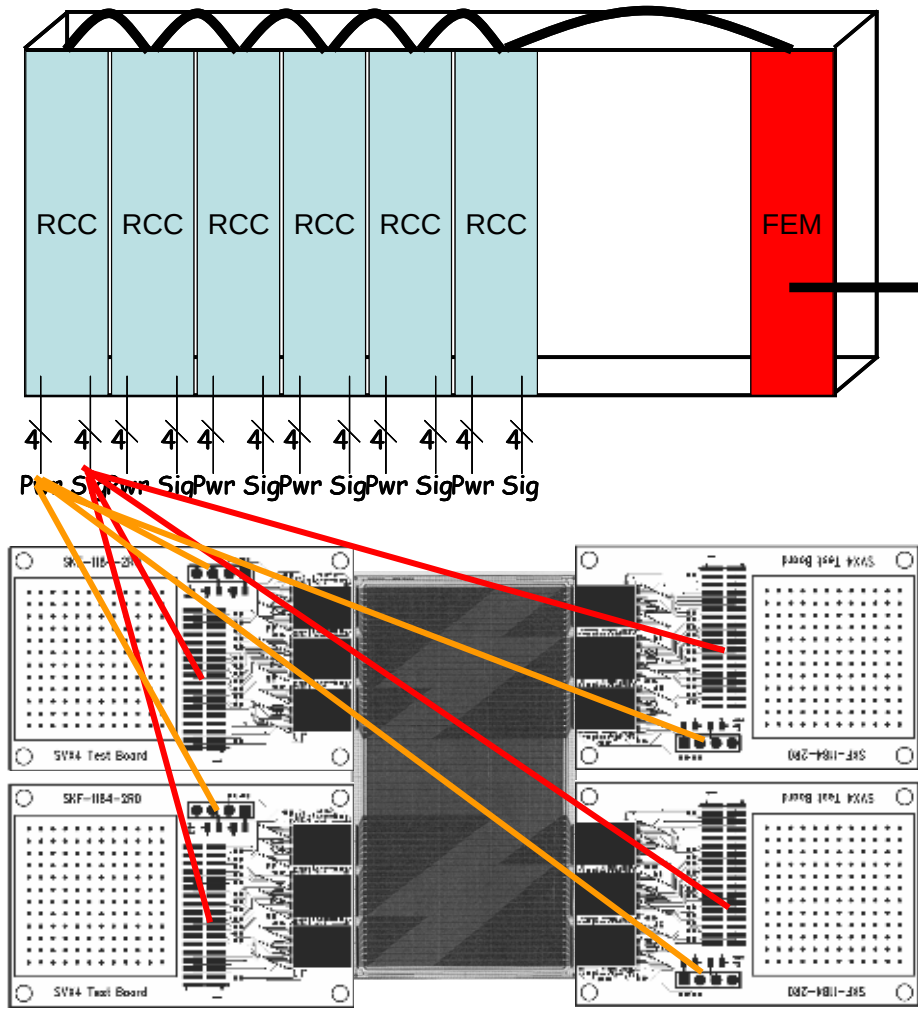
Data Sent by FEM to DCM

Word Type	Bits 16-0	Note
0	FFFF	DCM-required header word
1	Strip Barrel ID	Fixed # unique to strips.
2	Event #	
3	Module ID	A unique # for each ladder
4	Flag Word	0-suppression on/off
5	FEM BCLK Value	
6 -- 9	Data	Copies of RCC/FEM word types 0-3 (drop empty SVX4, RCC addresses)
10	Error Word	Bit 15: 5th Level-1, Bits 13-8 RCC/FEM BCLK match (1 bit per RCC), Bit 7: Data Transmission incomplete, Bits 5:0 Conversion Errors
11	FEM Serial #	Hard-coded on FEM Boards
12	FEM Firmware Version #	Encoded in FEM FPGAs
13	Parity Word	Bit-wise XOR of word types 1-12
14	0	DCM-required trailer word

Data format not important at this point except as a demonstration that testbench development should be directly portable to the FEMs.

Current R&D Status

- ROC implemented as four "hybrid boards" plus one "RCC board".
  - Large form factor allows for easier probing and debugging.
- Boards fabbed.
- Firmware and control GUI far along:
  - Correct signal pattern for serial control, digitization, readout seen at hybrid header (as determined by previous work w/ CDF hybrid).
- Goal is to complete debugging and start testing with sensors in March.



Budget Estimation Procedure

- Different components broken out into four categories.
  - R&D
  - Design
  - Prototype
  - Fab
- Further subdivided to give WBS elements which are defined by:
  - WBS dictionary page
  - Systematic contingency calculation
  - Cost sheet

Strip ROC Budget

ID	WBS	Task Name	Generic R&D Fy05	Manpower	Material (loc. overhead +tax)	Additional Overhead	DOE Contingency	TPC DOE (with contingency)	RIKEN	RIKEN Contingency	RIKEN Total
13	**1.1.1.1.1**	**ROC R&D**	**145338**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
14	1.1.1.1.1.1	ROC Design 0th Round	0	0	0	0	0	0	0	0	0
15	1.1.1.1.1.2	ROC Prototype 0th Round	0	0	0	0	0	0	0	0	0
16	1.1.1.1.1.3	ROC Design 1st Round	0	0	0	0	0	0	0	0	0
17	1.1.1.1.1.4	ROC Prototype 1st Round	0	0	0	0	0	0	0	0	0
18	1.1.1.1.1.9	ROC Design 2nd Round	145338	0	0	0	0	0	0	0	0
19	**1.1.1.1.2**	**ROC Design**	**0**	**34,605**	**0**	**3,114**	**13,202**	**50,921**	**0**	**0**	**0**
20	1.1.1.1.2.1	ROC Design Pre-production	0	34,605	0	3,114	13,202	50,921	0	0	0
21	**1.1.1.1.3**	**ROC Prototype**	**0**	**74,507**	**307890**	**34,416**	**129,212**	**546,025**	**0**	**0**	**0**
22	1.1.1.1.3.1	ROC Prototype 2nd Round	0	45,260	119311	14,811	55,609	234,991	0	0	0
23	1.1.1.1.3.2	ROC Prototype Pre-productic	0	29,247	188579	19,604	73,603	311,034	0	0	0
24	**1.1.1.1.4**	**ROC Fabrication**	**0**	**43,871**	**83984**	**3,948**	**43,303**	**175,106**	**160,000**	**0**	**160000**
25	1.1.1.1.4.1	ROC Fabrication - Boards	0	0	30550	0	11,915	42,465	0	0	0
26	1.1.1.1.4.5	ROC Fabrication - SVX4s	0	0	0	0	0	0	160,000	0	160000
27	1.1.1.1.4.6	ROC Fabrication - Other Part	0	0	15246	0	4,726	19,972	0	0	0
28	1.1.1.1.4.7	ROC Fabrication - Assembly	0	0	38188	0	11,838	50,026	0	0	0
29	1.1.1.1.4.8	ROC Fabrication - Test	0	43,871	0	3,948	14,824	62,643	0	0	0

Strip FEM Budget

ID	WBS	Task Name	Generic R&D Fy05	Manpower	Material (loc. overhead +tax)	Additional Overhead	DOE Contingency	TPC DOE (with contingency)	RIKEN	RIKEN Contingency	RIKEN Total
31	**1.1.1.1.5**	**FEM Design**	**0**	**80,037**	**0**	**7,203**	**27,045**	**114,285**	**0**	**0**	**0**
32	1.1.1.1.5.1	FEM Design - 1st Round	0	49,749	0	4,477	16,810	71,036	0	0	0
33	1.1.1.1.5.5	FEM Design - Pre-production	0	30,288	0	2,726	10,234	43,249	0	0	0
34	**1.1.1.1.6**	**FEM Prototype**	**0**	**76,963**	**18534**	**8,595**	**32,268**	**136,360**	**0**	**0**	**0**
35	1.1.1.1.6.1	FEM Prototype - 1st Round	0	48,212	9267	5,173	19,422	82,074	0	0	0
36	1.1.1.1.6.5	FEM Prototype - Pre-producti	0	28,751	9267	3,422	12,846	54,286	0	0	0
37		MILESTONE - Strip FEM Fabricat	0	0	0	0	0	0	0	0	0
38	**1.1.1.1.7**	**FEM Fabrication**	**0**	**43,871**	**64097**	**3,948**	**33,841**	**145,757**	**0**	**0**	**0**
39	1.1.1.1.7.1	FEM Fabrication - Boards	0	0	7755	0	1,551	9,306	0	0	0
40	1.1.1.1.7.2	FEM Fabrication - Parts	0	0	49879	0	15,463	65,342	0	0	0
41	1.1.1.1.7.3	FEM Fabrication - Assembly	0	0	6463	0	2,004	8,467	0	0	0
42	1.1.1.1.7.4	FEM Fabrication - Test	0	43,871	0	3,948	14,824	62,643	0	0	0
43	**1.1.1.1.8**	**ROC/FEE Testbench developme**	0	0	10980	988	5,984	17,952	0	0	0

Key Budget Assumptions

- Prototyping rounds:
  - ROC: four (including two at nominal size, thickness).
  - FEM: two (doesn't take credit for testbench control card development).
  - RCC: one (as an ASIC, after thorough debugging as an FPGA).
- Spares:
  - Require 10% *working* spares.
  - Assume 80% ROC yield, 90% FEM yield.
- Estimate total 3000 engineering hours.
- Physicist hours not included in project costs.
- All institutional overheads included.

Sample Dictionary Page

WBS #: 1.1.1.1.1.4 **Rev. 0 Date 12/23/04**
Title: ROC Prototype – 1st Round

DESCRIPTION (Scope, Number of Items, Method of Accomplishment, and Special Requirements)

Prototyping tasks consist of part ordering, parts, assembly and testing/debugging the board and firmware. Sometimes specialized equipment and/or development of a testbench is required. Part ordering, testing/debugging and development of test benches requires engineering and physicist resources – only engineering requirements are estimated. Assembly requires technician resources. Physicist resources are also required but not called out in the cost estimate.

The first round prototype ROC will be a functional equivalent of the final ROC (not thinned, non-ASIC implementation of the RCC). Generic R&D is needed to determine appropriateness of sensor selection. With forethought the work required to make that determination can accomplish this round of prototyping.

Costs include assembly of a testbench based on one built for SVX4.

Production quantities allow for a full ladder system test.

Costs are dominated by testing and debugging, the estimate for which is always difficult to estimate. Therefore costs are deemed to be based on engineering judgment.

Contingency Calculation

Technical, cost, and schedule risk factors

Technical	Cost	Schedule	Risk factor
Existing design and off-the-shelf hardware	Off-the-shelf or catalog item		1%
Minor modifications to an existing design	Vendor quote from established drawings	No schedule impact on any other item	2%
Extensive modifications to an existing design	Vendor quote with some design sketches		3%
New design, nothing exotic	In-house estimate based on previous similar experience	Delays completion of non-critical path subsystem item	4%
New design, different from established designs or existing technology	In-house estimate for item with minimal experience but related to existing capabilities		6%
New design, requires some R&D but does not advance the state-of-the-art	In-house estimate for item with minimal experience and minimal in-house capability	Delays completion of critical path subsystem item	8%
New design, development of new technology which advances state-of-the-art	Top-down estimate from analogous programs		10%
New design, way beyond the current state-of-the-art	Engineering judgment		15%

Technical, cost, and schedule risk weights

Technical	Cost	Schedule	Risk weight
	Material cost OR labor rate	Same for all	1
Design OR manufacturing	Material cost AND labor rate		2
Design AND manufacturing			4

- Each item in the WBS is assigned three risk factors (F) and three risk weights (W).
  - State of design
  - Basis of cost estimate
  - Schedule criticality
- $C = F_i W_i$, where repeated indices imply summation.

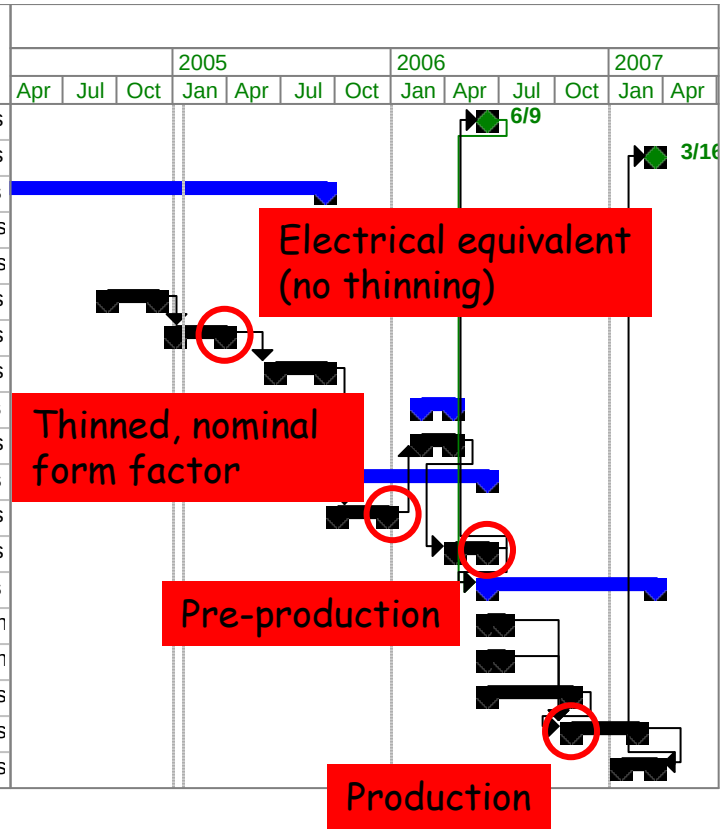
$C = 4x6\% + 2x15\% + 1x8\% = 62\%$

Sample Cost Sheet

WBS: 1.1.1.1.1.4			Quantities By/Date	TVC						
Activity: ROC Prototype - 1st Round			Costing By/Date	22-Dec-04						
PHENIX Silicon Vertex Detector			MATERIAL / CAPITAL EQUIPMENT		LABOR				MAT/LABOR	
NO	DESCRIPTION	QTY	UNITS	$ / UNIT	TOTAL-$	HRS/UNIT	WAGE	TOTAL HRS	TOTAL-$	OVERHEAD	TOTAL
1	Hybrid Boards	7		$ 250.00	$ 1,750		$ -	0	$ -	613	$ 2,363
2	Hybrid Parts	7		$ 100.00	$ 700		$ -	0	$ -	245	$ 945
3	Hybrid Assembly	7		$ 250.00	$ 1,750		$ -	0	$ -	613	$ 2,363
4	RCC Boards	5		$ 350.00	$ 1,750		$ -	0	$ -	613	$ 2,363
5	RCC Parts	5		$ 200.00	$ 1,000		$ -	0	$ -	350	$ 1,350
6	RCC Assembly	5			$ -		$ 38.65	30	$ 1,160	2,096	$ 3,256
	Testbench equipment:										
1	Control boards	2		$ 900.00	$ 1,800		$ -	0	$ -	630	$ 2,430
2	Control parts	2		$ 500.00	$ 1,000		$ -	0	$ -	350	$ 1,350
3	Control assembly	2			$ -		$ 38.65	30	$ 1,160	2,096	$ 3,256
4	Computer	1		$ 2,000.00	$ 2,000		$ -	0	$ -	700	$ 2,700
5	Crate	1		$ 1,000.00	$ 1,000		$ -	0	$ -	350	$ 1,350
6	Power supplies	1		$ 200.00	$ 200		$ -	0	$ -	70	$ 270
7	Cables	1		$ 300.00	$ 300		$ -	0	$ -	105	$ 405
8	Power supply, cable assembly	1			$ -		$ 38.65	20	$ 773	1,398	$ 2,171
9	Testing/Debugging	1			$ -		$ 76.03	240	$ 18,247	20,673	$ 38,921
TOTAL					$ 13,250			320	$ 21,339	$ 30,901	$ 65,490
			BNL Overhead	9.00%	$ 1,309				$ 1,921	$ 2,781	$ 6,011
			Sales Tax	9.800%	$ 1,299						$ 1,299
			Sub Total		$ 15,858				$ 23,260	$ 33,682	$ 72,800
Contingency Technical Risk Factor 0-15%		4%									
Contingency Technical Risk Weight 2 or 4		2									
Contingency Technical Risk Total Percent/Cost		8%	Sub Total		$ 1,269				$ 1,861	$ 2,695	$ 5,824
Contingency Cost Risk Factor 0-15%		15%									
Contingency Cost Risk Weight 1 or 2		1									
Contingency Cost Risk Total Percent/Cost		15%	Sub Total		$ 2,379				$ 3,489	$ 5,052	$ 10,920
Contingency Schedule Risk Factor 0-15%		8%									
Contingency Schedule Risk Weight = 1		1									
Contingency Schedule Risk Total Percent/Cost		8%	Sub Total		$ 1,269				$ 1,861	$ 2,695	$ 5,824
Total Percentage		31%	Total Contingency		$ 4,916				$ 7,211	$ 10,442	$ 22,568
			TOTAL		$ 20,774				$ 30,470	$ 44,124	$ 95,368

Strip ROC

ID	WBS	Task Name	Start	Duration
11		MILESTONE - Strip ROC Card Re	Fri 6/9/06	0 days
12		MILESTONE - Strip ROC Card Fa	Fri 3/16/07	0 days
13	**1.1.1.1.1**	**ROC R&D**	**Tue 4/1/03**	**640 days**
14	1.1.1.1.1.1	ROC Design 0th Round	Tue 4/1/03	4 mons
15	1.1.1.1.1.2	ROC Prototype 0th Round	Tue 7/22/03	4 mons
16	1.1.1.1.1.3	ROC Design 1st Round	Tue 9/14/04	60 days
17	1.1.1.1.1.4	ROC Prototype 1st Round	Tue 1/4/05	60 days
18	1.1.1.1.1.9	ROC Design 2nd Round	Tue 6/21/05	60 days
19	**1.1.1.1.2**	**ROC Design**	**Mon 2/20/06**	**40 days**
20	1.1.1.1.2.1	ROC Design Pre-production	Mon 2/20/06	40 days
21	**1.1.1.1.3**	**ROC Prototype**	**Mon 10/3/05**	**180 days**
22	1.1.1.1.3.1	ROC Prototype 2nd Round	Mon 10/3/05	60 days
23	1.1.1.1.3.2	ROC Prototype Pre-productic	Mon 4/17/06	40 days
24	**1.1.1.1.4**	**ROC Fabrication**	**Mon 6/12/06**	**200 days**
25	1.1.1.1.4.1	ROC Fabrication - Boards	Mon 6/12/06	1 mon
26	1.1.1.1.4.5	ROC Fabrication - SVX4s	Mon 6/12/06	1 mon
27	1.1.1.1.4.6	ROC Fabrication - Other Part	Mon 6/12/06	5 mons
28	1.1.1.1.4.7	ROC Fabrication - Assembly	Mon 10/30/06	4 mons
29	1.1.1.1.4.8	ROC Fabrication - Test	Mon 1/22/07	2 mons



Si Strip FEE Team

- ORNL
  - Physics:
    - VC (Subsystem Manager), K. Read, D. Silvermyr, C. Zhang, S. Batsouli.
    - Experience with PHENIX FEE, DAQ and testbench development (MuID, Pad Chamber) and with project management.
  - EE:
    - M. Bobrek (Lead Engineer), K. Castleberry, B. Bryan, U. Jagadish, C. Britton.
    - Both digital and analog expertise.
    - Specific experience with many PHENIX subsystems.
- ISU
  - Physics
    - C. Ogilvie, J. Lajoie, postdocs TBD.
    - Experience with PHENIX L1 trigger.
  - EE
    - G. Sleege
    - Experience with PHENIX L1 trigger.