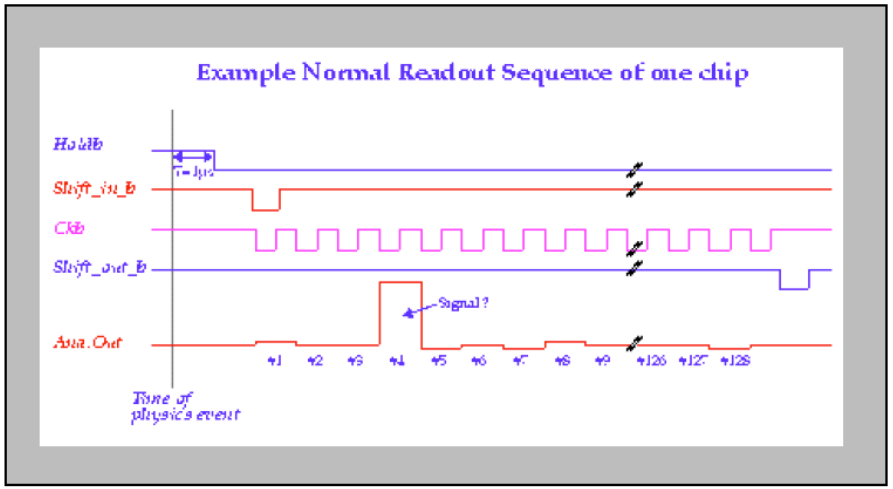
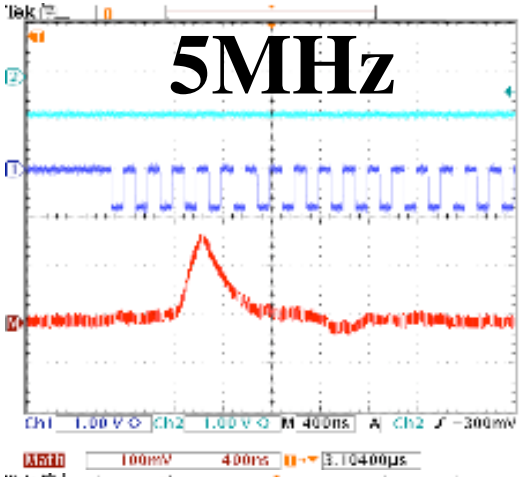
Clock Scan Dependence

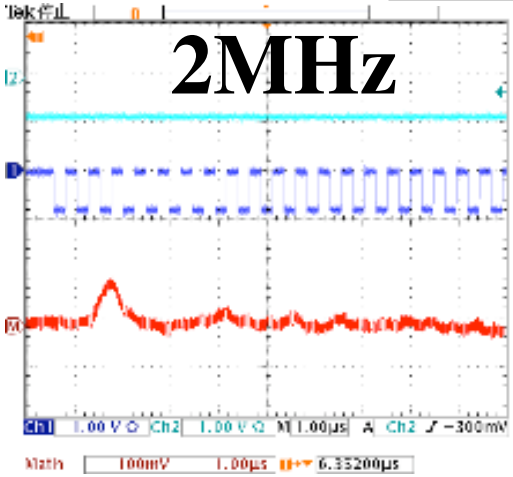


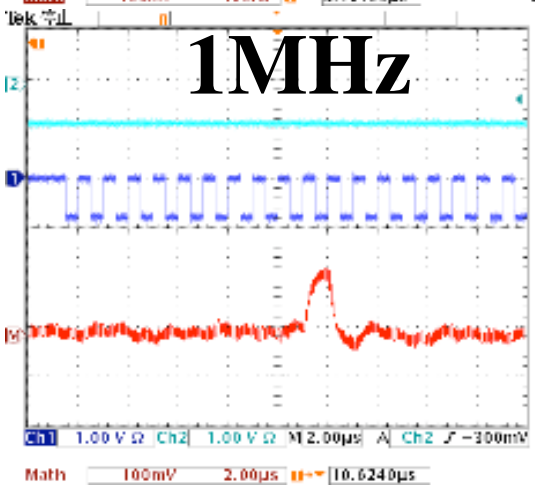
From VA manual

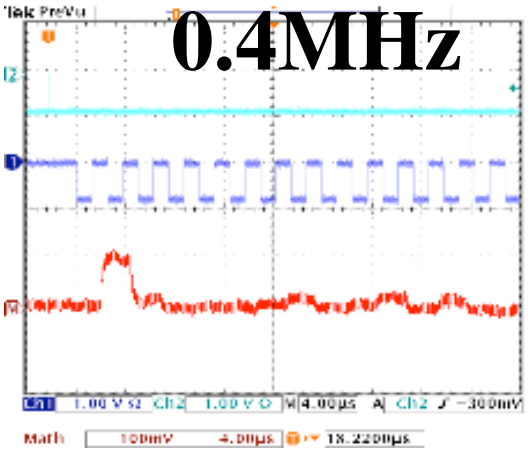
CLOCK (CONVERT)

OUTPUT(差動後)









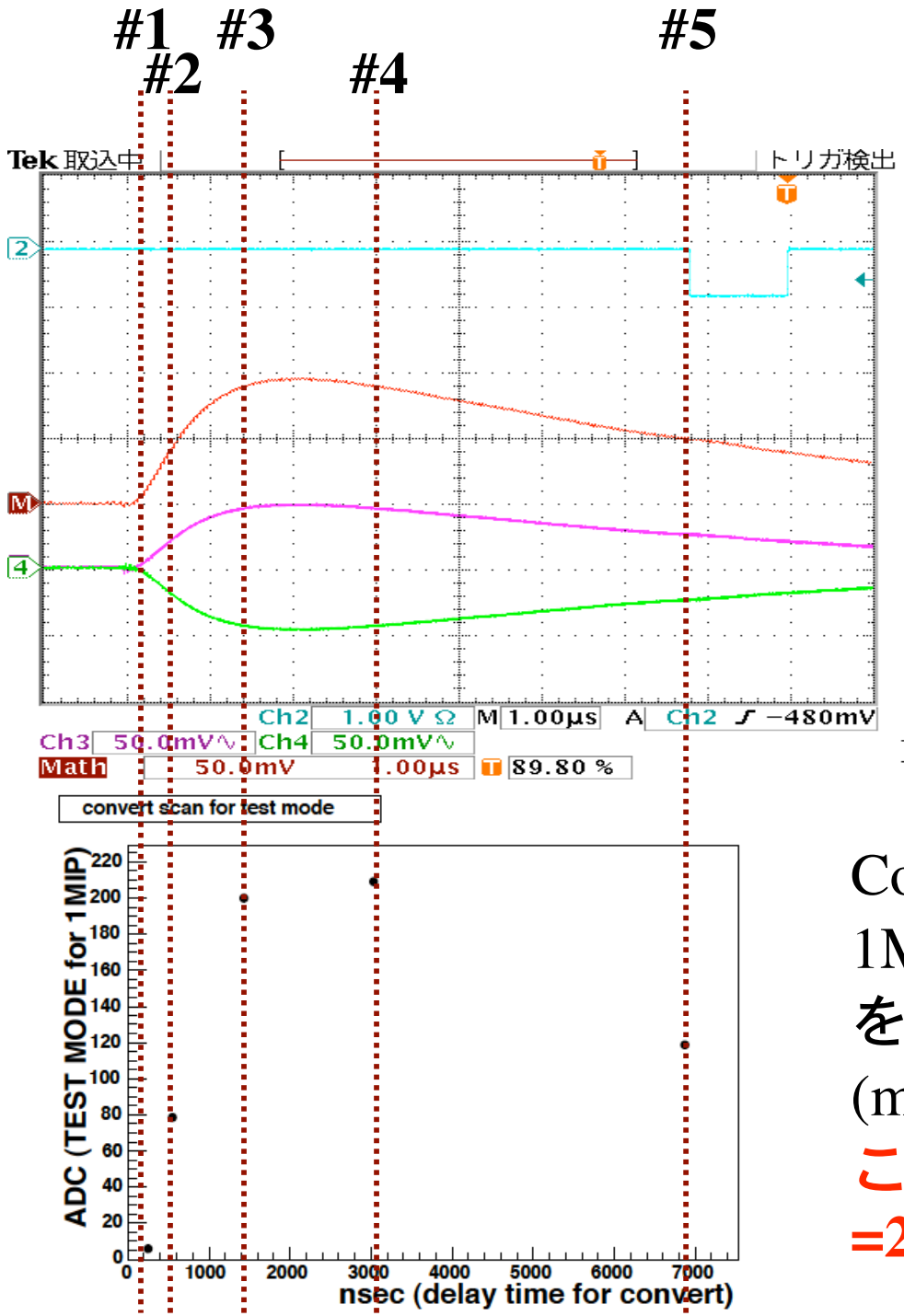
Did effort to reduce noise

A.Taketani,J.Tojo,M.Togawa

- Put bias resister (more higher ~20M)
- Change power supply for VME
  - VME emits noise (~100kHz)
- VMEとインターフェースボードの間のラインを短くした

……..

To understand Test Mode

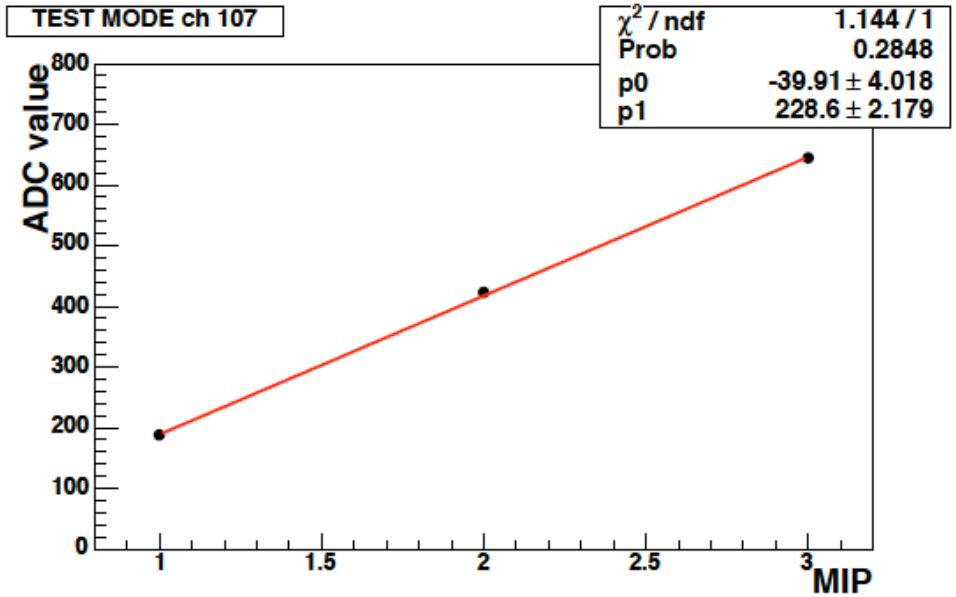


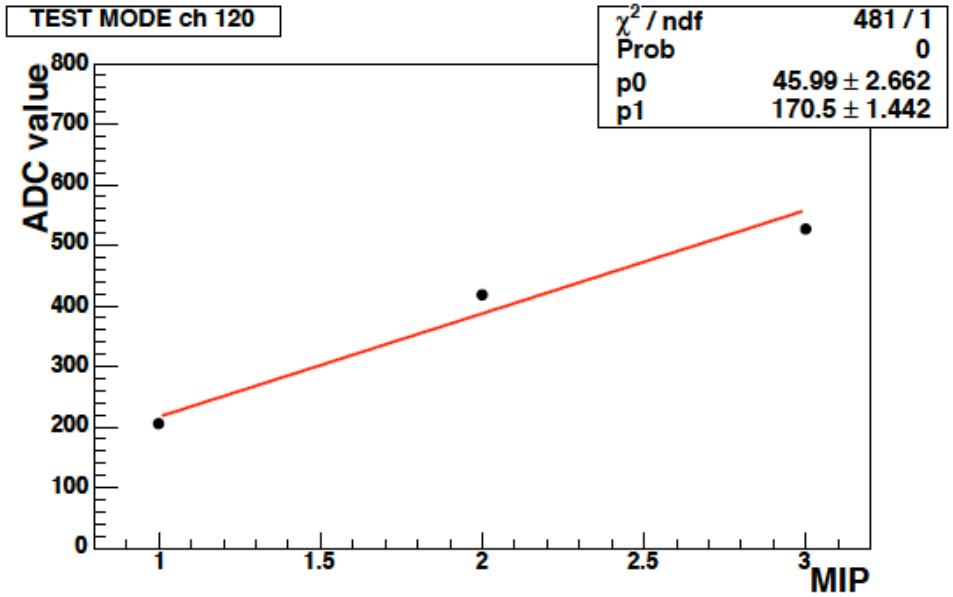
convert

差動アウトプット
ピン:(+) 緑:(-)
赤:(+)-(-)

Convertの立ち下がりを見ている
1MΩターミネーションで見た波形を再現。
(manualではADC inputは50Ω <- ?)
この設定での1MIP(300um,片面)=211ch

Test Mode Linearity





Test Modeのリニアリティーは良いものもあれば悪いものもある

1 MIPは300um、片面読み出しに相当。(22400e^- = 3.6fC)

^{90}Srソーステスト

1VA(xの1~128ch)のみを変えてデータを取った。

・channel/clusterは1~2あたりに分布。(KEKではシグナルは常に2ch以上)

・**1MIPは~120ch。**

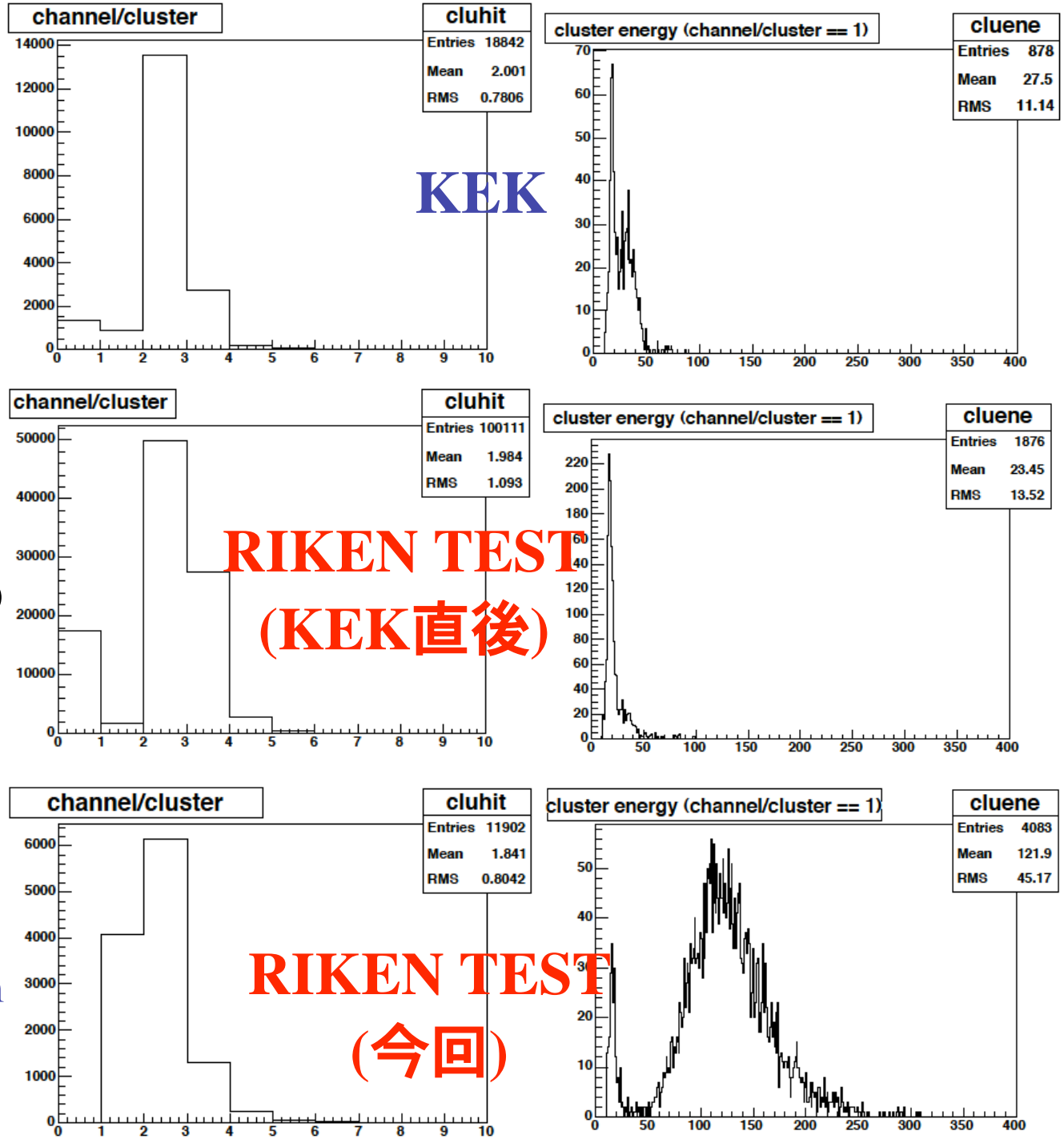
ゲインの違い:

x : u = 75 : 90

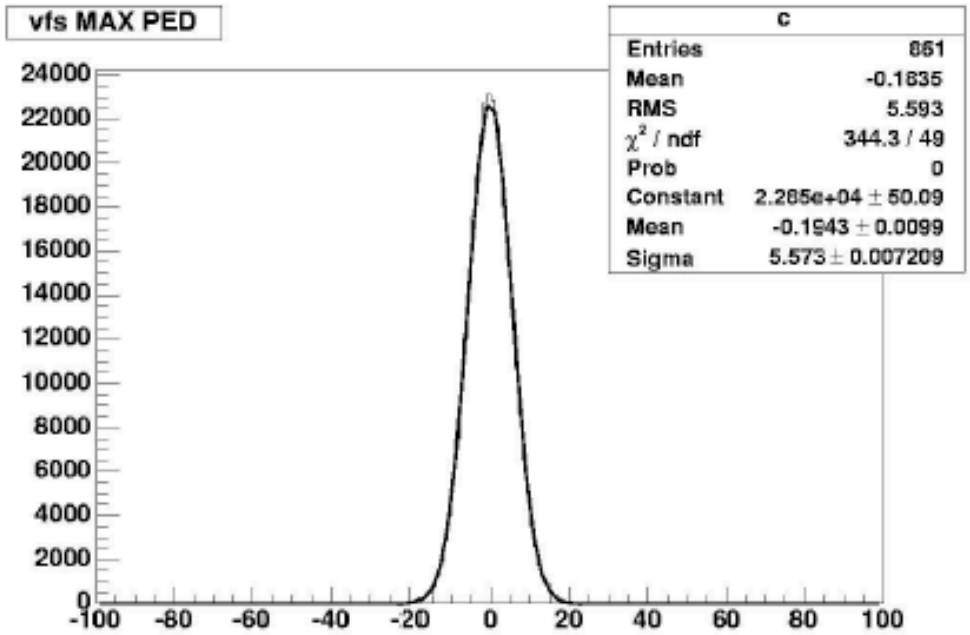
-> x+u ~ 264

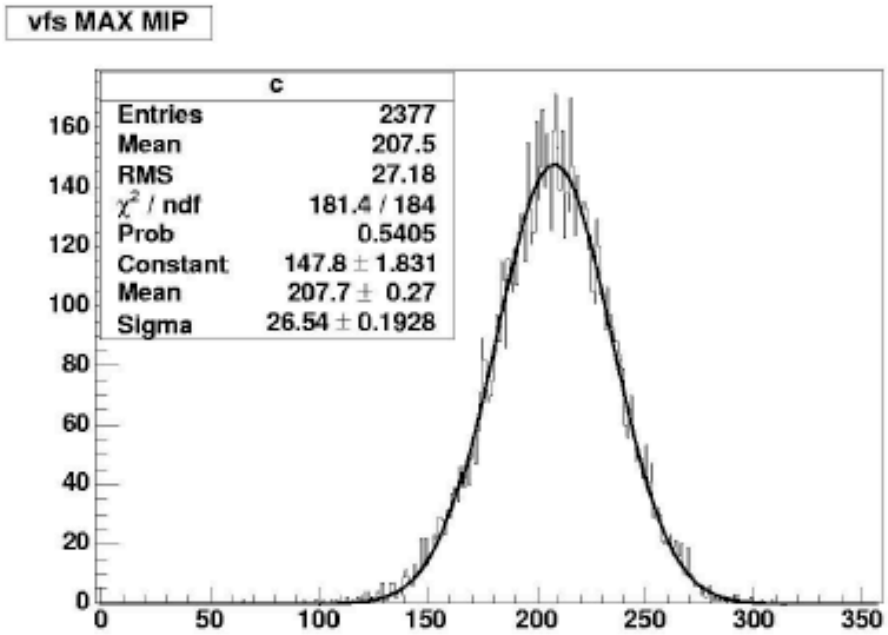
テストモードより400umに直すと、

211*4/3 ~ 281



S/N ratio (from TEST MODE)





S/N = 207.7 / 5.575 ~ 37.3 **37.3 * 4/3 * 1/2 = 24.9**

Noise : 22400/37.3 ~ 600 e

Noise

- **Load Capacitance of our sensor (C_d)**
  - Ver1. : 10pF Ver2. : 15pF
- **Chip specification**
  - VA2 : 80+15/pF e^- rms
  - SVX4 : 675+45/pF e^- rms
- **Expected noise**
  - VA2 : ~230 e^- rms (C_d~10pF), ~305 e^- rms (C_d~15pF)
  - SVX4 : ~1125e^- rms (C_d~10pF), ~1350e^- rms (C_d~15pF)

- **Now Our noise, 600e^-**
  - unknownノイズ sqrt(600^2-230^2) ~ 554e^-
- **SVX4へは(unknownノイズが外来のみとすると)**
  - (Si+SVX4)ノイズ+外来ノイズ : sqrt(1350^2+554^2) ~ 1460
  - S/N : 15000 / 1460 ~ 10.3