

PHENIX Electron Trigger for Heavy Ion Physics

Kenta Shigaki (KEK) at PHENIX Trigger Meeting on February 11, 2000



Presentation Outline

- Needs for Electron Trigger in PHENIX
 - Trigger Needs for Heavy Ion Physics
- Electron Trigger Algorithm
- Simulation Studies
 - Electrons to be Triggered
 - Rejection for Minimum-Bias Events
 - Minimum-Bias Trigger Rates
 - Rejection for Peripheral Au+Au
- Heavy Ion Physics Gain with Electron Trigger
- Summary

Needs for Electron Trigger in PHENIX

- reaction rates (w/ blue book luminosity)
 - 200 A GeV Au+Au
 - 6 barn x 2e26 cm⁻²sec⁻¹ = 1.2 kHz
 - 200 GeV p+p
 - 50 mb x 8e30 cm⁻²sec⁻¹ = 400 kHz (4 MHz later)
 - 500 GeV p+p
 - 60 mb x 2e31 cm⁻²sec⁻¹ = 1.2 MHz (12 MHz later)
- DAQ capability
 - LV1 limit : 25 kHz (6 kHz initially)
 - LV2 limit : 20 Mbyte/sec ~ 100 Hz min.-bias Au+Au

Trigger Needs for Heavy Ion Physics

- p+p and light A+A
 - essential to understand Au+Au data
 - no p+p data at the RHIC energy
 - only limited data at the ISR energy up to $\sqrt{s} = 63 \text{ GeV}$
 - uncertainty in p+p can easily overshadow new phenomena in Au+Au
 - true for basically all physics probes
 - $J/\Psi, \phi, \omega, \rho, charm, \dots$
- peripheral Au+Au ?
 - might be where the QCD phase transition occurs



Electron Trigger Algorithm (1)

- front-end
 - EMCal Ersatz LV1
 - 172 bits from overlapping 4x4 PMT sums
 - *ref.* G.Young at this Trigger Meeting
 - RICH LV1
 - 256 bits from non-overlapping 4x5 PMT sums
 - *ref.* T.Matsumoto at Trigger Meeting in December '99
 - *ref*. T.Matsumoto/K.Oyama at this Trigger Meeting



Electron Trigger Algorithm (2)

- EMCal-RICH look-up
 - was not in original GL1
 - a really simple scheme: 1/2 sector matching
 - EMCal: 3x3 (PbSc) / 4x4 bits (PbGl) OR'ed
 - RICH: 4x4 bits (= 1 readout FEM) OR'ed
 - look-up: simple 1-to-1 AND of 16 bits + 16 bits
 - *ref.* K.Shigaki at Heavy/Light and Spin PWG's in August '99
 - studies to finalize specifications
 - finer segmentation for better rejection power ?
 - overlapping look-up for higher efficiency ?
 - single/double electron trigger ?



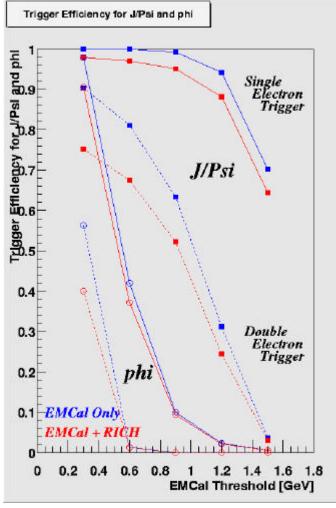
Simulation Studies

- vector meson signals
 - MDC-2 and its follow-up at RCF
 - requested by M.Rosati, K.Barish; processed by I. Ojha et al.
 - 778 J/ Ψ , 700 ϕ from RV generator
- minimum-bias backgrounds
 - MDC-J-2 at PHENIX-CC-J
 - requested by K.Shigaki; processed by N. Hayashi et al.
 - 12,117 Au+Au, 6,120 Ag+Ag, 12,211 Si+Si, 85,203 p+p
- more vector meson signals for systematic study
 - VRDC at PHENIX-CC-J / RCF
 - requested by K.Shigaki; processed by N. Hayashi et al.
 - 60K J/ Ψ , 54K ϕ at fixed p_t

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Electrons to be Triggered (MDC-2)



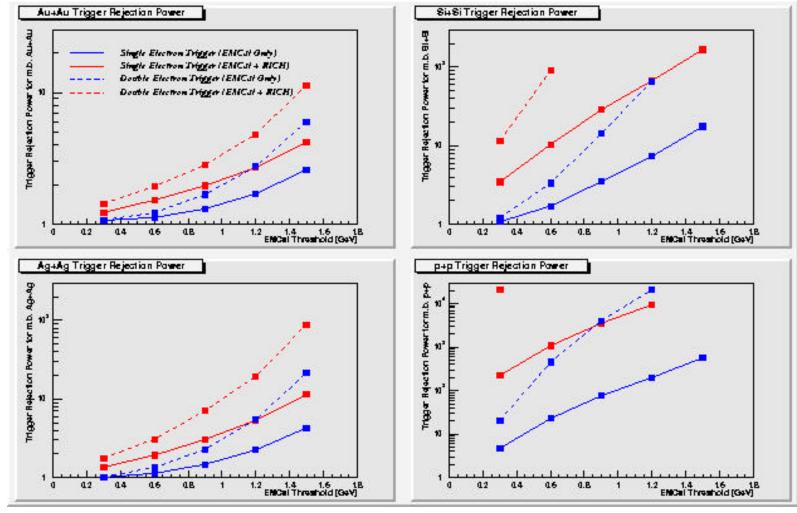
• for J/Ψ

- single electron threshold < 1 GeV
- for
 - single electron threshold < 500 MeV
- for charm
- further study ongoing in VRDC
 - as a function of p_t
 - acceptance cut
 - pair reconstruction

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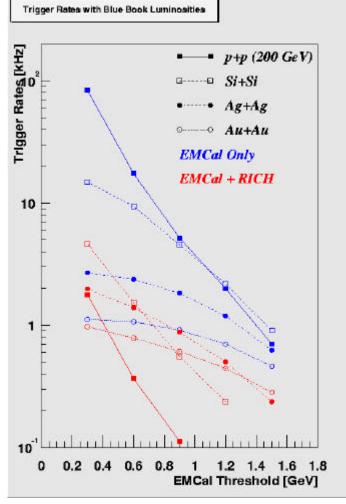
Rejection for M.B. Events (MDC-J-2)



February 11, 2000



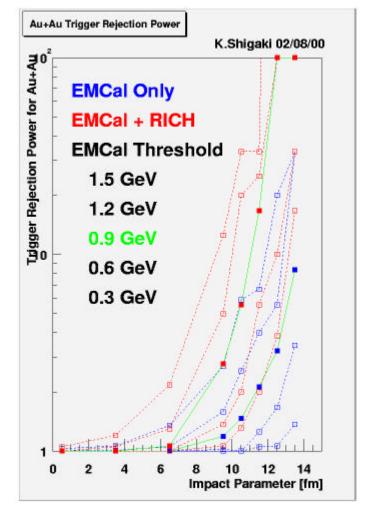
Minimum-Bias Trigger Rates (MDC-J-2)



- plots: single electron trigger rates with blue book luminosity
- EMCal trigger with light collision systems:
 - marginal for J/Ψ
 - insufficient for ϕ (and c?)
 - does not sustain x10 luminosity
- EMCal + RICH trigger:
 - works even for \$\op\$ from x10 luminosity p+p



Rejection for Peripheral Au+Au



- any use of the trigger in Au+Au running ?
 - rejection power exists for peripheral Au+Au events, which might be where the QCD phase transition occurs



HI Physics Gain with Electron Trigger

- high luminosity runs
 - p+p and light A+A
 - at BBL and with future RHIC upgrade
- possible use for peripheral Au+Au
- low electron threshold
 - can go down « 1 GeV
- access to rare probes
 - $J/\Psi, \phi, \omega, \rho$ (di-electron)
 - charm (single electron)
- essential to systematic studies of virtually all single/di- electron channels



Summary

- electron trigger for heavy ion physics
 - essential for systematic studies with light A+A, p+p
 - can be useful to trigger peripheral Au+Au
- simple EMCal-RICH look-up does (EMCal alone does not) cover many physics probes (J/ Ψ , ϕ , ω , ρ , charm, ...)
 - allows electron threshold « 1 GeV with light collision systems
 - required for ϕ and charm (single electron) trigger
 - sustains x10 blue book luminosity
- look-up scheme being studied to finalize hardware specifications