- Single phase cooling is well suited to the endcaps.
- Two adjacent octant panels can be cooled in series thus reducing service connections.
- 2mm cooling tubes and panel thickness are adequate.
- The radiation length of the octant panel exclusive of sensor and electronics is ~ 0.6 %.

The R&D issues consist of refining the calculations, designing attachment points to the main support structure, and prototyping the octant panels.

5 R+D Schedule, Responsibilities and Budget

5.1 R+D Areas

The R&D associated with the endcaps involves modifying the topology of the PHX chip, developing the interface between the PHX chip and the existing PHENIX DCMs, modifying the design of an existing sensor, developing the wedge structure, and developing the bus and flex cable. The data interface is the most involved of the R&D projects. The rest are starting from existing technology or use standard commercial concepts. The R&D for the endcaps will be supported at LANL and BNL. At LANL we will complete the R&D for the interface, the mechanical support and ladder, and the sensor design. BNL will support the R&D for the PHX design and modification.

5.1.1 FPHX

The FPHX chip is a modification of the FPIX 2.1 pixel chip used for the BTeV experiment. The FPHX is a 1 column x 128 channel structure designed for holes rather than electron collection. It has a data push architecture similar to the FPIX2.1 chip and ~ 70 micron channel pitch. The R&D issues involve optimizing the front-end for the mini-strips, designing the digital readout specifically for the PHENIX DAQ and converting the chip to wire bonds. FNAL electronics group(Ray Yarema, head) has completed the conceptual design of FPHX and the next phase will be to do the wafer layout and prototype. We expect that this phase will proceed in early calendar 2007.

5.1.2 Sensor

The sensor will be a standard p on n DC coupled silicon diode. This is a very conventional design that is available from many vendors. The R&D consists of mainly developing the prototype masks and producing prototypes for testing. We have begun the process of identifying vendors and the Czech group have started designing the sensor. We expect to procure a prototype in the spring of 2007.

5.1.3 Interface

The ROC and FEM boards that will connect between the PHX chip and PHENIX DCMs will need to provide the following functions:

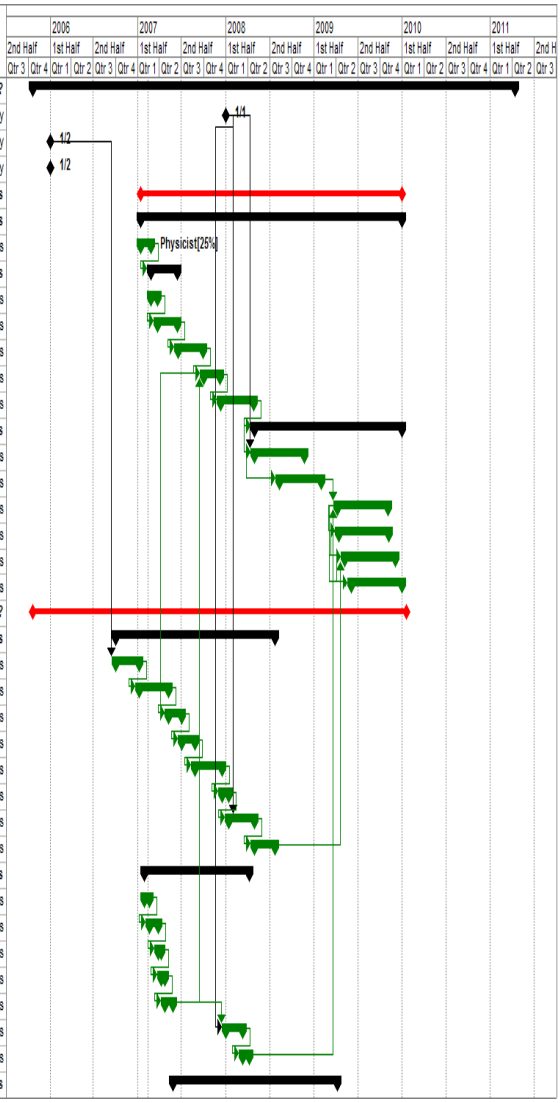
- Strip the sync words out of the data stream, retaining only data words
- Combine the data from several chips into one serial stream which will go via fiber to a FEM
- Provide buffering of the continuously streaming data from the PHX chips for 64 beam clocks, and this buffering must be adequate for everything from pp running to central Au-Au events
- Upon a lvl-1 accept, retrieve the data from the buffer for the appropriate beam clock and package it into a format acceptable by the DCM
- Pass beam clock to the PHX chip, assure sychronization
- Provide an interface to download initialization settings to the PHX chips
- Perhaps provide ability to reset PHX chip(s)

We expect the board designs to be largely completed by our LDRD grant which will put a prototype forward silicon tracker in to PHENIX, and will be using FPIX chips which will have very similar digital output to the FPHX chips. Some details will need to be modified to accept the somewhat different segmentations of the FVTX detector compared to the LDRD detector. A large portion of the designs have already been prototyped via efforts at LANL and Columbia, using FPIX chips and FPGA evaluation boards. The FPIX chips have been successfully read out, with one or more data lines per chip, the data have been buffered into 64 clock buffers, and the correct event from a given chip has been shown to be properly pulled out from the clock buffers upon a trigger. Prototyping will begin in early 2007.

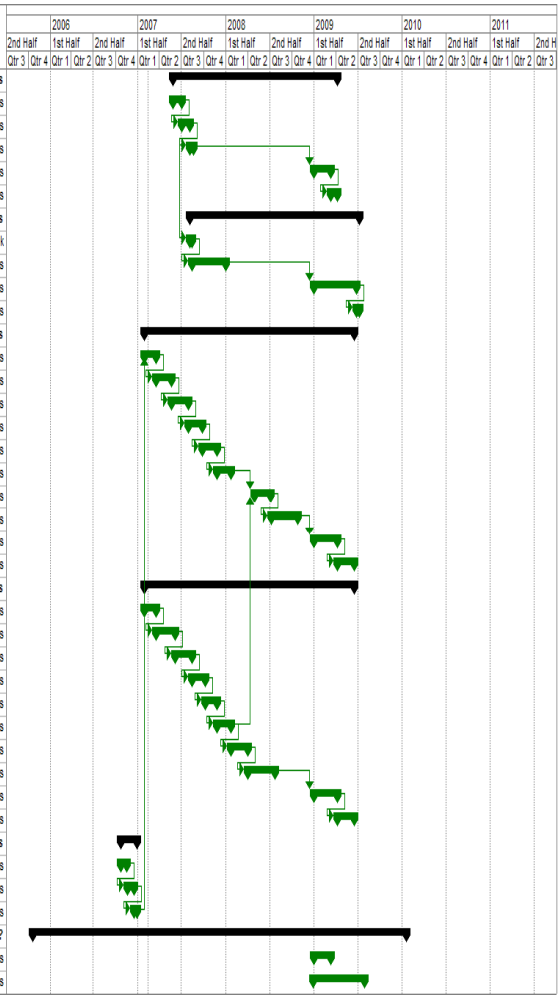
5.2 Schedule

The schedule for the FTVX project is shown in Figure 102. Included in the schedule is the R&D timeline. We have assumed R&D money begins in the second quarter of FY06 and construction funds begin in the second quarter of FY08. Task durations are based on previous experience of the engineering teams and quotes. The total project duration is due primarily to the sensor and PHX R&D and procurement times.

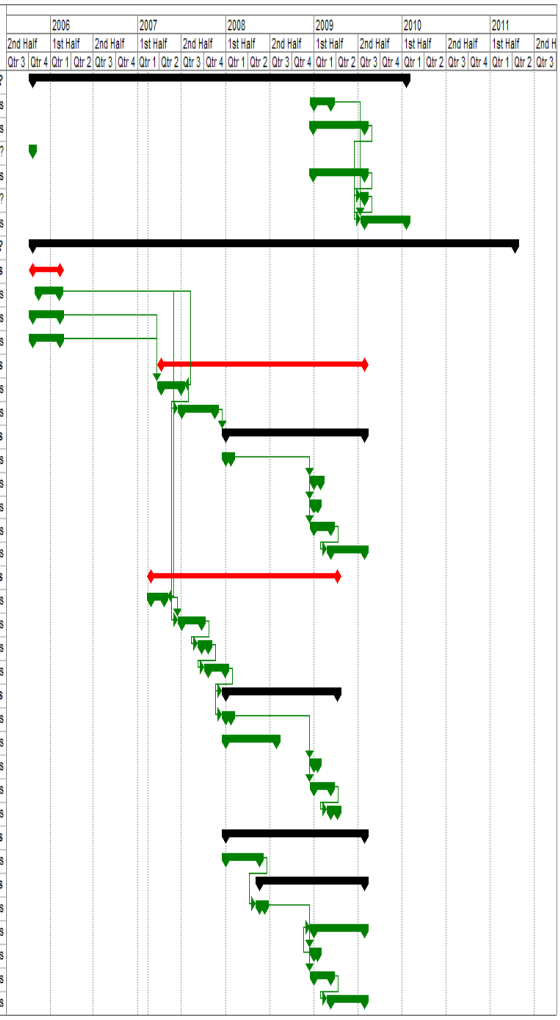
ID	Task Name	Start	Finish	Duration
1	FVTX Project	Fri 10/21/05	Wed 4/13/11	1429 days?
2	Start Construction	Tue 1/1/08	Tue 1/1/08	1 day
3	Start R&D BNL	Mon 1/2/06	Mon 1/2/06	1 day
4	Start R&D LANL	Mon 1/2/06	Mon 1/2/06	1 day
5	Sensors	Mon 1/15/07	Wed 12/30/09	773 days
6	Wedge sensors	Mon 1/15/07	Wed 12/30/09	773 days
7	design sensors	Mon 1/15/07	Fri 2/23/07	6 wks
8	procure prototype sensor	Mon 2/26/07	Fri 6/15/07	80 days
9	mask set	Mon 2/26/07	Fri 3/23/07	4 wks
10	sensor manufacture	Mon 3/26/07	Fri 6/15/07	12 wks
11	test prototype sensor	Mon 6/18/07	Fri 9/28/07	15 wks
12	wire bond FPHX	Mon 10/1/07	Fri 12/7/07	10 wks
13	test FPHX sensor assembly	Mon 12/10/07	Fri 4/25/08	20 wks
14	procure sensors	Mon 4/28/08	Wed 12/30/09	438 days
15	procure sensor	Mon 4/28/08	Fri 11/21/08	30 wks
16	Sensor Q/A	Mon 8/11/08	Fri 1/30/09	25 wks
17	Attach flex cable	Thu 4/9/09	Wed 11/4/09	30 wks
18	Attach sensor	Mon 4/13/09	Fri 11/6/09	30 wks
19	wire bond assembly	Thu 5/7/09	Wed 12/2/09	30 wks
20	test chip,sensor + cable assembles	Thu 6/4/09	Wed 12/30/09	30 wks
21	Ministrip electronics	Fri 10/21/05	Tue 1/19/10	1108 days?
22	FPHX Chip	Tue 10/3/06	Mon 7/21/08	470 days
23	design(FNAL)	Tue 10/3/06	Mon 1/8/07	14 wks
24	submit prototype	Tue 1/9/07	Mon 5/7/07	17 wks
25	test prototype	Tue 5/8/07	Mon 7/2/07	8 wks
26	redesign	Tue 7/3/07	Mon 8/27/07	8 wks
27	resubmit prototype	Tue 8/28/07	Mon 12/17/07	16 wks
28	test 2nd proto	Tue 12/18/07	Mon 1/14/08	4 wks
29	engineering run	Tue 1/15/08	Mon 4/28/08	15 wks
30	test chips(FNAL)	Tue 4/29/08	Mon 7/21/08	12 wks
31	Kapton flex cables HDI	Tue 1/30/07	Tue 4/8/08	311 days
32	design	Tue 1/30/07	Mon 2/19/07	3 wks
33	prototype	Tue 2/20/07	Mon 3/26/07	5 wks
34	test	Tue 3/27/07	Mon 4/9/07	2 wks
35	redesign	Tue 4/10/07	Mon 4/23/07	2 wks
36	prototype	Tue 4/24/07	Mon 5/28/07	5 wks
37	procure	Wed 1/2/08	Tue 3/11/08	10 wks
38	test cable	Wed 3/12/08	Tue 4/8/08	4 wks
39	Kapton HDI to ROC interconnect	Tue 5/29/07	Wed 4/8/09	487 days



ID	Task Name	Start	Finish	Duration
39	**Kapton HDI to ROC interconnect**	**Tue 5/29/07**	**Wed 4/8/09**	**487 days**
40	design	Tue 5/29/07	Mon 7/2/07	5 wks
41	prototype	Tue 7/3/07	Mon 8/6/07	5 wks
42	test prototype	Tue 8/7/07	Mon 8/20/07	2 wks
43	procure	Thu 1/1/09	Wed 3/11/09	10 wks
44	test cable	Thu 3/12/09	Wed 4/8/09	4 wks
45	**Fiber output ROC-FEM**	**Tue 8/7/07**	**Wed 7/8/09**	**502 days**
46	design	Tue 8/7/07	Mon 8/13/07	1 wk
47	prototype	Tue 8/14/07	Mon 12/31/07	20 wks
48	procure	Thu 1/1/09	Wed 6/24/09	25 wks
49	test cable	Thu 6/25/09	Wed 7/8/09	2 wks
50	**ROC Electronics**	**Tue 1/30/07**	**Mon 6/15/09**	**620 days**
51	design	Tue 1/30/07	Mon 3/19/07	7 wks
52	prototype	Tue 3/20/07	Mon 5/21/07	9 wks
53	test prototype	Tue 5/22/07	Mon 7/30/07	10 wks
54	redesign	Tue 7/31/07	Mon 9/24/07	8 wks
55	2nd prototype	Tue 9/25/07	Mon 11/26/07	9 wks
56	test second proto	Tue 11/27/07	Mon 1/21/08	8 wks
57	PHENIX system test	Mon 4/28/08	Fri 7/4/08	10 wks
58	preproduction prototype	Mon 7/7/08	Fri 10/24/08	16 wks
59	production	Thu 1/1/09	Wed 4/8/09	14 wks
60	Q/A - 28 units	Thu 4/9/09	Mon 6/15/09	48 days
61	**FEM Electronics**	**Tue 1/30/07**	**Mon 6/15/09**	**620 days**
62	design	Tue 1/30/07	Mon 3/19/07	7 wks
63	prototype	Tue 3/20/07	Mon 6/4/07	11 wks
64	test prototype	Tue 6/5/07	Mon 8/13/07	10 wks
65	redesign	Tue 8/14/07	Mon 10/8/07	8 wks
66	2nd prototype	Tue 10/9/07	Mon 11/26/07	7 wks
67	test second proto	Tue 11/27/07	Mon 1/21/08	8 wks
68	PHENIX system test	Tue 1/22/08	Mon 3/31/08	10 wks
69	preproduction prototype	Tue 4/1/08	Mon 7/21/08	16 wks
70	production	Thu 1/1/09	Wed 4/8/09	14 wks
71	Q/A - 28	Thu 4/9/09	Mon 6/15/09	48 days
72	**Calibration**	**Mon 10/23/06**	**Fri 12/29/06**	**50 days**
73	Design Pulse injection	Mon 10/23/06	Fri 11/17/06	4 wks
74	prototype	Mon 11/20/06	Fri 12/15/06	4 wks
75	test prototype	Mon 12/18/06	Fri 12/29/06	2 wks
76	**Ancillary**	**Fri 10/21/05**	**Tue 1/19/10**	**1108 days?**
77	Racks	Thu 1/1/09	Wed 3/11/09	10 wks
78	LV,HV,etc	Tue 12/30/08	Mon 7/27/09	30 wks



ID	Task Name	Start	Finish	Duration
76	**Ancillary**	**Fri 10/21/05**	**Tue 1/19/10**	**1108 days?**
77	Racks	Thu 1/1/09	Wed 3/11/09	10 wks
78	LV,HV,etc	Tue 12/30/08	Mon 7/27/09	30 wks
79	DCM-24	Fri 10/21/05	Fri 10/21/05	1 day?
80	Slow controls	Tue 12/30/08	Mon 7/27/09	30 wks
81	Misc lab equip	Tue 7/28/09	Tue 7/28/09	1 day?
82	install	Wed 7/29/09	Tue 1/19/10	25 wks
83	**Mechanics**	**Fri 10/21/05**	**Wed 4/13/11**	**1429 days?**
84	**specifications**	**Fri 10/21/05**	**Thu 2/9/06**	**80 days**
85	endcaps - specify heat load	Tue 11/15/05	Mon 2/6/06	12 wks
86	specify mechanical tolerances/distortions	Fri 10/21/05	Thu 2/9/06	4 mons
87	specify disassembly/configuration options	Fri 10/21/05	Thu 2/9/06	4 mons
88	**Support structure cage**	**Mon 4/9/07**	**Wed 7/29/09**	**603 days**
89	design	Mon 4/9/07	Fri 6/29/07	12 wks
90	prototype	Mon 7/2/07	Fri 11/16/07	20 wks
91	**procure**	**Wed 1/2/08**	**Wed 7/29/09**	**411 days**
92	detail drawings	Wed 1/2/08	Tue 1/22/08	3 wks
93	liason	Thu 1/1/09	Wed 1/28/09	4 wks
94	tooling	Thu 1/1/09	Wed 1/14/09	2 wks
95	material	Thu 1/1/09	Wed 3/11/09	10 wks
96	Fabrication	Thu 3/12/09	Wed 7/29/09	20 wks
97	**ladder wedge**	**Mon 2/26/07**	**Wed 4/8/09**	**553 days**
98	design	Mon 2/26/07	Fri 4/20/07	8 wks
99	prototype	Mon 7/2/07	Fri 9/21/07	12 wks
100	test	Mon 9/24/07	Fri 10/19/07	4 wks
101	final design	Mon 10/22/07	Fri 12/28/07	10 wks
102	**procure**	**Wed 1/2/08**	**Wed 4/8/09**	**331 days**
103	constr drawings	Wed 1/2/08	Tue 1/22/08	3 wks
104	liason	Wed 1/2/08	Tue 7/29/08	30 wks
105	tooling	Thu 1/1/09	Wed 1/14/09	2 wks
106	material	Thu 1/1/09	Wed 3/11/09	10 wks
107	fabrication	Thu 3/12/09	Wed 4/8/09	4 wks
108	**cooling plate**	**Wed 1/2/08**	**Wed 7/29/09**	**411 days**
109	R&D design	Wed 1/2/08	Tue 5/20/08	20 wks
110	**Procure**	**Wed 5/21/08**	**Wed 7/29/09**	**311 days**
111	construction drawings	Wed 5/21/08	Tue 6/10/08	3 wks
112	liason	Thu 1/1/09	Wed 7/29/09	30 wks
113	tooling	Thu 1/1/09	Wed 1/14/09	2 wks
114	material	Thu 1/1/09	Wed 3/11/09	10 wks
115	fabrication	Thu 3/12/09	Wed 7/29/09	20 wks



ID	Task Name	Start	Finish	Duration
115	fabrication	Thu 3/12/09	Wed 7/29/09	20 wks
116	**Alignment and assembly jigs**	**Thu 4/9/09**	**Wed 6/3/09**	**40 days?**
117	design wedge jig	Thu 4/9/09	Thu 4/9/09	1 day?
118	procure wedge jig	Thu 4/9/09	Wed 5/20/09	6 wks
119	design cool plate jig	Thu 4/9/09	Wed 4/22/09	2 wks
120	procure cool plate ass jig	Thu 4/23/09	Wed 6/3/09	6 wks
121	design cage ass jig	Thu 4/9/09	Wed 4/22/09	2 wks
122	procure cage ass jig	Thu 4/23/09	Wed 6/3/09	6 wks
123	**Endcap Assembly**	**Thu 12/31/09**	**Wed 4/13/11**	**335 days**
124	**Assemble ladders onto cooling plate**	**Thu 12/31/09**	**Wed 6/16/10**	**120 days**
125	place wedges on cooling plate	Thu 12/31/09	Wed 3/24/10	12 wks
126	optically survey wedges	Thu 3/25/10	Wed 6/16/10	12 wks
127	**Install into cage enclosure**	**Thu 6/17/10**	**Wed 7/7/10**	**15 days**
128	place cooling plates in cage	Thu 6/17/10	Wed 7/7/10	3 wks
129	optically survey	Thu 6/17/10	Wed 7/7/10	3 wks
130	Install into VTX enclosure	Thu 7/8/10	Wed 9/1/10	2 mons
131	COMMISION	Thu 9/2/10	Wed 4/13/11	8 mons
132	**System Integration**	**Wed 1/2/08**	**Tue 11/16/10**	**750 days**
133	Mechanical egineer	Wed 1/2/08	Tue 11/16/10	150 wks
134	Electrical Engineer	Wed 1/2/08	Tue 11/16/10	150 wks
135	FVTX Management	Wed 1/2/08	Tue 11/16/10	150 wks

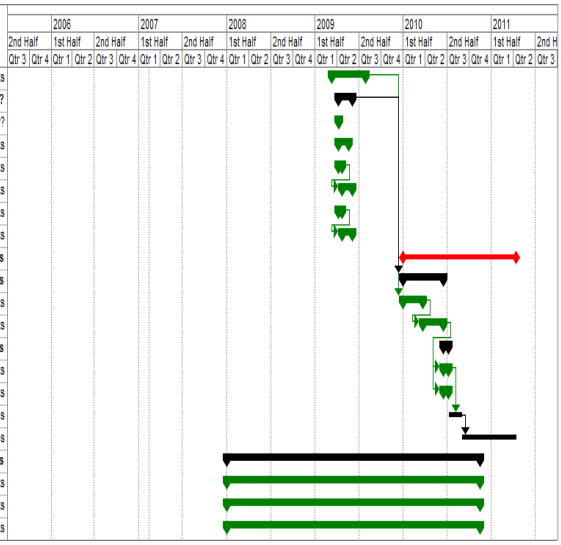


Figure 102 – PHENIX Forward Silicon Vertex (FVTX) project timeline.

5.2.1 Cost

Since the FVTX will be added to the existing barrel vertex detector, VTX, much of the needed infrastructure, cooling, enclosure, cable routing, installation procedures, etc. will already have been done and be in place. In this cost estimate only those items needed for fitting the FVTX into the VTX enclosure are considered. The costs in Table 12 are generally obtained from cost estimates by the engineering team who will be doing the work and from cost estimates for work already done by those teams. For example, the cost estimate for the PHX chip came from the FNAL engineers who designed the FPIX2 chip. The HYTEC engineering team previously designed the ATLAS pixel mechanical structures and that forms the basis for the mechanical cost estimates. The cost basis for the sensors are from quotes from ON Semiconductor Inc. in Prague, Czech Republic and CIS Semiconductor obtained in Nov. 2005 and on drawings of the wafers with the FVTX wedges. The contingency analysis method is listed in Appendix A (Section 6).

Forward Endcap Cost Estimate - FVTX

FY2007 dollars

2 endcaps	R&D BNL(k$)	R&D LANL(K$)	Construction(k$)	comments	total contin	Cost with Contingency	2008	2009	2010
Mechanical ladder and support structure		100	400	HYTEC Estimate	0.25	499.00		499	
Alignment and Assembly jigs			90	engineering estimate	0.26	113.40		113.6	
Silicon Sensor		50							
purchase			410	CIS and ON quotes, 10% spare, 80% yiel	0.26	516.60	516.6		
setup and masks		30		CIS and ON quotes					
sensor Q/A and testing			50	University students + engineer	0.16	58.00	58		
PHX chip, tested	175								
engineering run			240	FNAL estimate	0.36	326.40	326.4		
testing			50	FNAL tech	0.16	58.00	58		
attach HDI to backplane			30	engineering estimate	0.22	36.60		36.6	
attach sensor			30	engineering estimate	0.22	36.60		36.6	
wire bond assembly		55	188	Promex quote	0.26	236.88		236.9	
test wedge assembly			40	engineering estimate	0.22	48.80		48.8	
ROC electronics		261							
preproduction proto			73.3	engineering estimate	0.36	99.69	99.7		
production			443	engineering estimate	0.36	602.70		602.5	
Q/A			20	engineering estimate	0.14	22.80			
FEM electronics		223							
preproduction			93	engineering estimate	0.36	126.48		126.5	
production			323	engineering estimate	0.36	439.28		439.3	
Q/A			20	engineering estimate	0.14	22.80		22.8	
Racks,LV,HV,DCM,install			81	existing designs	0.12	90.72			90.72
slow controls			5	existing designs	0.12	5.60			5.6
calibration system		22							
Assemble endcap			90	techs and students	0.26	113.40			113.4
Electronics Integration			250	Engineer	0.14	285.00	95	95	95
Mechanical Integration			250	Engineer	0.14	285.00	95	95	95
HDI bus		40	106	422 HDI, 10% spares, $250 ea.	0.25	132.50	132.5		
flex cables, sensor to ROC		25	51	784 flex, 2% spares, $42 ea.	0.13	57.43		57.43	
fibercables, ROC-FEM		3	31	56ea. -12 and 8 channel units	0.15	35.59		35.6	
lab equipment			100	probe, test equipment	0.1	110.00	110		
Management			200		0.14	228.00	76	76	76
total	175	809	3664.3			4587.26	1567.2	2521.63	475.72
				Inflation adjusted(.035 per year)		4850.29	1622.052	2700.666	527.5735

BNL overhead 18%
LANL overhead and GRT 19.5%
All labor fully burdened

Table 12 – Cost estimate for the FVTX endcaps with contingency. The methodology used for contingency is in Appendix A (Section 6).

5.2.2 Project Management and Responsibilities

The LANL Group will work together with HYTEC inc. to develop the design for the Endcap mechanical ladder and cooling. LANL has formed collaboration with FNAL to design, prototype and test the PHX readout chip. An MOU with PHENIX, BNL physics department and FNAL for R&D of the PHX chip was signed in 2004.

The organizational chart for the FVTX project is shown in Figure 103.

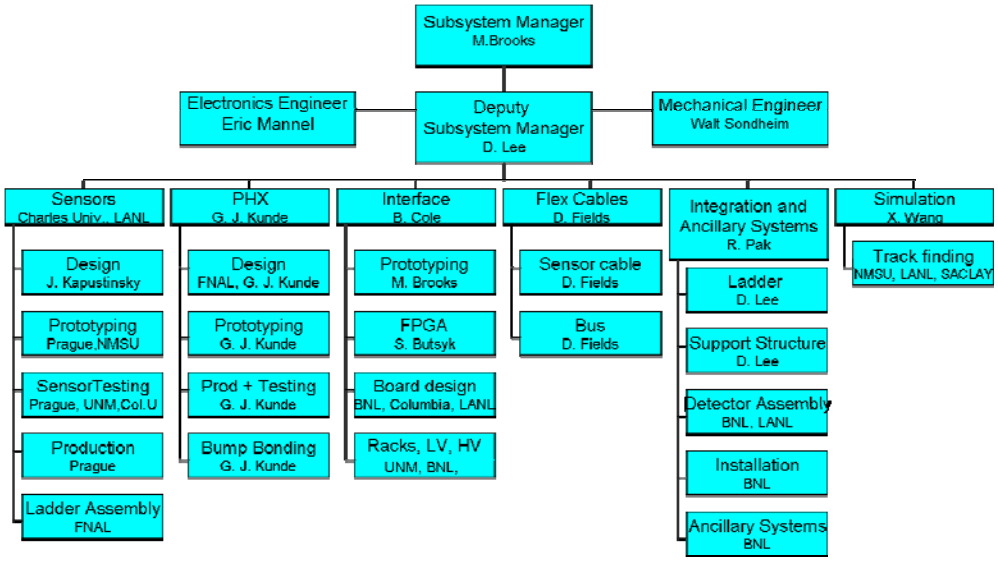


Figure 103 - Organizational Chart for the FVTX project.

Institutional Responsibilities

Los Alamos National Laboratory

LANL coordinate work to procure the silicon sensors, work with FNAL on the development of the PHX chip, with Columbia on development of the interface to PHENIX DAQ, and on the simulation effort with NMSU. Los Alamos is currently leading the mechanical engineering and the integration effort for the barrel detector, and will continue those efforts for the FVTX.

Columbia University

Columbia University is an acknowledged expert on the PHENIX DAQ system. They will work on the interface between the PHX chip and the PHENIX DAQ. The lead electronics engineer also comes from Columbia.

Iowa State University

Iowa State University is currently working on management details with the barrel detector and working on an (funded) SBIR effort addressing the level 1 trigger capabilities of the FVTX. They are also involved with the interface module.

Charles University, Czech Technical University, Institute of Physics, Academy of Sciences, Prague, Czech Republic

Charles University has been active in the development, testing, assembly, and commissioning of the ATLAS pixel sensors. They will do the same for the FVTX effort and additionally participate in software development.

New Mexico State University

NMSU will work on comprehensive simulations for the FVTX effort.

University of New Mexico

UNM has experience in testing, Q/A and a laboratory for characterization of sensors. They are currently working on the barrel strip sensors and will do the same for the FVTX effort.

Saclay

Saclay will work on software.

Yonsei University, Seoul, Korea

The Yonsei group has worked on electronics and software for the muon system. They have not defined their scope of work.

6 Appendix A – Contingency Analysis

6.1 Contingency Analysis

The average contingency for the FVTX is 25.2 %.

This section describes how the contingency for a given WBS element was calculated. Risk is a function of the following factors: the sophistication of the technology, the maturity of the design effort, the accuracy of the cost sources and the impact of delays in the schedule. Risk analysis is performed for each WBS element at the lowest level estimated. Results of this analysis are related to a contingency, which is listed for each WBS element. The goal is to make the method of contingency determination uniform for all project WBS elements.

Definitions

Base Cost Estimate – The estimated cost of doing things correctly the first time. Contingency is not included in the base cost.

Cost Contingency – The amount of money, above and beyond the base cost, that is required to ensure the project's success. This money is used only for omissions and unexpected difficulties that may arise. Contingency funds are held by the Project Manager.

Risk Factors

Technical Risk – Based on the technical content or technology required to complete the element, the technical risk indicates how common the technology is that is required to accomplish the task or fabricate the component. If the technology is so common that the element can be bought "off-the-shelf", i.e., there are several vendors that stock and sell the item, it has very low technical risk, therefore a risk factor of 1 is appropriate. On the opposite end of the scale are elements that extend the current "state-of-the-art" in this technology. These are elements that carry technical risk factors of 10 or 15. Between these are: making modifications to existing designs (risk factor 2-3), creating a new design which does not require state-of-the-art technology (risk factor 4 & 6), and creating a design which requires R&D, and advances the state-of-the-art slightly (risk factor 8 & 10).

Cost Risk – Cost risk is based on the data available at the time of the cost estimate. It is subdivided into 4 categories.

The first category is for elements for which there is a recent price quote from a vendor or a recent catalog price. If the price of the complete element, or the sum of its parts, can be found in a catalog, the appropriate risk factor to be applied is 1. If there is an engineering drawing or specification for the element, and a reliable vendor has recently quoted a price based on these, the cost risk factor to be applied is 2. Similarly, if a vendor has quoted a price based on a sketch that represents the element, and the element's design will not change prior to its fabrication, the appropriate cost risk factor would be 3.

The second category is for elements for which there exists some relevant experience. If the element is similar to something done previously with a known cost, the cost risk factor is 4. If the element is something for which there is no recent experience, but the capability exists, the cost risk is 6. If the element is not necessarily similar to something done before, and is not similar to in-house capabilities, but is something that can be comfortably estimated, the risk factor is 8.

The third category is for elements for which there is information that, when scaled, can give insight into the cost of an element or series of elements. The cost risk factor for this category is 10.

The fourth category is for elements for which there is an educated guess, using the judgment of engineers or physicists. If there is experience of a similar nature, but not necessarily designing, fabricating or installing another device, and the labor type and quantity necessary to perform this function can be estimated comfortably, a cost risk factor of 15 is appropriate.

Schedule Risk – If a delay in the completion of the element could lead to a delay in a critical path or near critical path component, the schedule risk is 8. If a delay in the completion of the element could cause a schedule slip in a subsystem which is

not on the critical path, the schedule risk is 4. Only elements where a delay in their completion would not affect the completion of any other item have schedule risks of 2.

Design Risk – is directly related to the maturity of the design effort. When the element design is nearly complete, quantity counts and parts lists finished, the risk associated with design is nearly zero; therefore a risk factor of 0 is applied. This is also the case when the element is an "off-the-shelf" item and the parts counts and quantities are finalized. When the element is still just an idea or concept, with crude sketches the only justification for the cost estimate, the risk associated with design state is high or 15. Between these two extremes are the stages of conceptual design and preliminary design. In conceptual design, when layout drawings of the entire element are approaching completion, some preliminary scoping analyses have been completed, and parts counts are preliminary, the design risk factor is 8. During preliminary design, when there are complete layout drawings, some details worked out, complete parts counts, and some analysis for sizing and showing design feasibility, the appropriate design risk is 4.

Weighting Factors

The weight applied to the risk factors depends on whether there are multiple or single risks involved in completing an element.

The weights applied to technical risk depend upon whether the element requires pushing the current state-of-the-art in design, manufacturing, or both. If the element requires pushing both, the weight to be applied is high, or 4; if either the design or manufacturing are commonplace, the weighting factor is 2.

For weights applied to cost risk, the two factors are material costs and labor costs. If either of these are in doubt, but not both, the weight to be applied to cost risk is 1. If they are both in doubt, the weight applied is 2.

The weight factor given to schedule risk is always 1.

The weight factor given to design risk is always 1 and so is not shown explicitly.

Procedure

The following procedure is used for estimating contingency.

Step 1 – The conceptual state of the element is compared with Table 4 to determine risk factors. A technical risk factor is assigned based on the technology level of the design. A design risk factor is assigned based upon the current state (maturity) of the design. A cost risk factor is assigned based on the estimating methodology used to arrive at a cost estimate for that element. Similarly, a schedule risk factor is identified based on that element's criticality to the overall schedule.

Step 2 – The potential risk within an element is compared with Table 5 to determine the appropriate weighting factors.

Step 3 – The individual risk factors are multiplied by the appropriate weighting factors and then summed to determine the composite contingency percentage.

Step 4 – This calculation is performed for each element at its lowest level.

Step 5 – The dollar amount of contingency for an element is calculated by multiplying the base cost by the composite contingency percentage.

Risk Factor	Technical	Cost	Schedule	Design
0	Not used	Not used	Not used	Detail design > 50% done
1	Existing design and off-the-shelf H/W	Off-the-shelf or catalog item	Not used	Not used
2	Minor modifications to an existing design	Vendor quote from established drawings	No schedule impact on any other item	Not used
3	Extensive modifications to an existing design	Vendor quote with some design sketches	Not used	Not used
4	New design; nothing exotic	In-house estimate based on previous similar experience	Delays completion of non-critical subsystem item	Preliminary design >50% done; some analysis done
6	New design; different from established designs or existing technology	In-house estimate for item with minimal experience but related to existing capabilities	Not used	Not used
8	New design; requires some R&D but does not advance the state-of-the-art	In-house estimate for item with minimal experience and minimal in-house capability	Delays completion of critical path subsystem item	Conceptual design phase; some drawings; many sketches
10	New design of new technology; advances state-of-the-art	Top-down estimate from analogous programs	Not used	Not used
15	New design; well beyond current state-of-the-art	Engineering judgment	Not used	Concept only

Table 13 - Technical, cost and schedule risk factors.

Risk Factor	Condition	Weighting Factor
Technical	Design OR Manufacturing	2
	Design AND Manufacturing	4
Cost	Material Cost OR Labor Rate	1

	Material Cost AND Labor Rate	2
Schedule	Same for all	1
Design	Same for all	1

Table 14 - Technical, cost, schedule and design weighting factors.

7 Appendix B – The FVTX Level-1 Trigger System

7.1 Introduction

In this Appendix we present the current status of a conceptual design for a Level-1 trigger system utilizing the FVTX detector. While many of the details remain to be worked out, the design outlined here is a powerful, flexible trigger system that exploits synergies between many PHENIX upgrades and can address a wide array of physics observables.

We begin by summarizing the additional required event rejection for single and di-muon physics with the PHENIX detector beyond that currently available with the existing Muon Identifier Local Level-1 (MuID LL1). We outline a trigger strategy starting with an FVTX LL1 system for the identification of tracks from both the primary and displaced vertices. This trigger strategy requires combining the FVTX LL1 output with additional information from the PHENIX Muon Trigger Upgrade, which we describe in detail. We then report on the current hardware research and development effort, and conclude with a cost estimate for the FVTX LL1

7.2 Required Event Rejection

The required event rejection for heavy flavor physics with the PHENIX muon arms in future RHIC and RHIC-II running can be divided into two classes of trigger signals – single muons and muon pairs.

The existing trigger option for single muons is to trigger on at least one deep muon road in the Muon Identifier (MuID). A deep road is defined as a track in LL1 that penetrates all layers of the MuID. The achieved rejection factors for the 1-Deep MuID LL1 trigger in both p+p and Au+Au are shown in Table 15 (taken from Table 30 in this proposal). Also shown are the required rejections for the end of RHIC-I running as well as for RHIC-II. The required rejections are what are needed to ensure that the triggers are not prescaled (Table 31 this proposal). Prescaling means that valid triggers are not written to disk because the rate exceeds a bandwidth limit at Level-1 (1kHz). For convenience the required rejections are factorized into the current rejection and the required improvement.

Table 15 - Event rejection required beyond the MuID LL1 for RHIC-I (2008) and RHIC-II running for single muon triggers.

Existing Trigger MuID 1-Deep	Achieved Rejection	Rejection needed 2008	Rejection needed RHIC-II
p+p	478	478*21	478*71
Au+Au	5	5*15	5*116